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HIGH-ORDER CASCADE MULTIBIT ΣΔ MODULATORS FOR xDSL APPLICATIONS

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ABSTRACT

This paper explores the use of ΣΔ modulators for A/D conversion in xDSL applications. Two high-order multibit architectures, the 2-1-1*mb* modulator [7] and a novel 2-1-1-1*mb* cascade (MASH), are proposed to achieve 14bit dynamic range @ 4.4MS/s using low oversampling ratio. They show very low sensitivity to the internal DAC linearity error, with no calibration required. Simulations show this performance can be achieved in presence of circuit imperfections, using submicron digital CMOS processes.

1. INTRODUCTION

ΣΔModulators (ΣΔMs) have been successfully employed in the past for low-, medium-frequency A/D conversion [1]. The use of oversampling and noise-shaping techniques in these converters avoids the need of extremely accurate analog building blocks, what makes them very suitable in the context of poor-analog-performance submicron CMOS processes. Such advantages have encouraged designers to widen the bandwidth of ΣΔ converters up to the data acquisition and communication ranges [2]-[8], demanding high-resolution and high-speed operation.

Considering only quantization noise, the dynamic range *DR* of a ΣΔM can be roughly estimated as follows:

$$DR(\text{dB}) = 10\log\left[\frac{3(2^B-1)^2(2L+1)M^{2L+1}}{\pi^{2L}}\right] \quad (1)$$

where L stands for the modulator order, M for its oversampling ratio, and B for the internal quantizer resolution in bits.

In high-speed applications, increasing the signal bandwidth f_x while maintaining an achievable sampling frequency f_s implies the use of a moderate M, since $M = f_s/(2f_x)$. In this scenario, the natural way to increase *DR* in order to cope with high-resolution specifications is to resort to high-order (increasing L), multibit (increasing B) ΣΔMs. However, two important drawbacks arise:

- On the one hand, unlike 1st- and 2nd-order loops, high-order loops are not unconditionally stable.
- On the other, the linearity of the multibit ΣΔM is ultimately limited by that of the multibit DAC in the feedback path.

Both problems have been partially overcome; actually, high-order ΣΔMs have been stabilized through several techniques [1]: i.e., proper choice of the scaling factors, use of multipath feedforward structures, or resetting of the internal variables if unstable operation is detected. On the other hand, a common strategy to palliate the strong dependence on the internal DAC linearity is using calibration either in the analog or in the digital domain [1].

Nevertheless, cascade multibit architectures overcome these problems with neither calibration nor resetting required by:

- performing the high-order filtering by cascading low-order (1st- and 2nd-) ΣΔMs to guarantee unconditional stability, and
- using multibit quantization only at the last stage of the cascade to attenuate the influence of the DAC non-linearity [2].

This paper explores the use of such architectures to obtain 14bit@4.4MS/s – specifications in the range of xDSL requirements. In Section 2, two cascade multibit architectures are considered: a 4th-order 3-stage cascade (with the structure 2-1-1) and a 5th-order 4-stage cascade (2-1-1-1), both including multibit quantization. Section 3 is dedicated to analyze the impact of circuit imperfections degrading the modulators performance.

2. CASCADE MULTIBIT ΣΔMs

Fig.1 shows a generic Lth-order N-stage cascade multibit ΣΔM. It includes single-bit quantizers in all stages except the last one which has a multibit quantizer. In cascade ΣΔMs, the quantization error induced in each stage is remodulated by the following one in the cascade. Once in the digital domain, by properly combining the outputs of the stages, it is possible to cancel out the quantization error in all stages except that in the last one, which appears at the modulator output attenuated by a shaping function of order equal to the summation of the order of all stages. Thus, ideally, the following is obtained for the Z-domain output:

$$Y(z) = z^{-L}X(z) + d(1-z^{-1})^{L}E_N(z) - d(1-z^{-1})^{(L-L_N)}E_D(z) \quad (2)$$

where $X(z)$ is the Z-transform of the modulator input, d is an scalar larger than unity resulting from proper scaling of the transferred signal to prevent overloading of the stages, $E_N(z)$ is the last-stage quantization error, $E_D(z)$ is the error induced in the last-stage DAC,

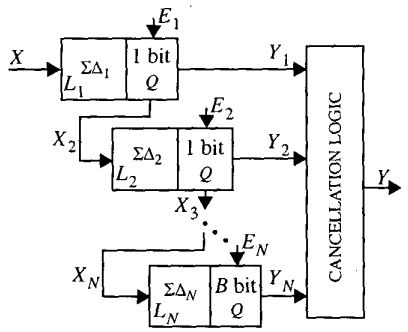

Fig. 1: Generic Lth-order N-stage cascade multibit ΣΔM.

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and $L = L_1 + \ldots + L_N$. Note that $E_D(z)$ is $(L - L_N)$th -order shaped, what significantly relaxes the DAC linearity specifications, with neither correction nor calibration required.

Several cascade multibit ΣΔMs have been reported: a 3rd-order 2-1 cascade (2-1*mb*) [2], a 4th-order 2-2 cascade (2-2*mb*) [3], and a 4th-order 2-1-1 cascade (2-1^2*mb*) [7]. According to eq.(2), DAC-induced error is 2nd-order shaped in the first two modulators and 3rd-order shaped in the last one. Thus, while in the 2-1*mb* and 2-2*mb* architectures the in-band power of such error is attenuated by M^5, it is attenuated by M^7 in the 2-1^2*mb*. This considerably reduces the sensitivity of the latter to the DAC *INL*, simplifying therefore its design. Fig.2 illustrates the 2-1^2*mb* cascade ΣΔM.

A 5th-order 4-stage 2-1-1-1 cascade using multibit quantization in the last stage (2-1^3*mb*), Fig.3, has been developed as an extension of the former to one more order, while preserving its properties. Ideally, the following Z-domain output is obtained for both modulators:

$$\begin{aligned} Y(z)|_{2\text{-}1^2mb} &= z^{-4}X(z) + d_3(1-z^{-1})^4E_3(z) - d_3(1-z^{-1})^3E_D(z) \\ Y(z)|_{2\text{-}1^3mb} &= z^{-5}X(z) + d_5(1-z^{-1})^5E_4(z) - d_5(1-z^{-1})^4E_D(z) \end{aligned} \quad (3)$$

where it has been assumed that the relationships among digital and analog coefficients and the values of the digital filters $H_k(z)$, $k = 1, \ldots, 6$ are those in Table 1 and 2, respectively. Therefore, the in-band error power at both modulator outputs is

$$\begin{aligned} P_{2\text{-}1^2mb} &= d_3^2\left(\sigma_Q^2\,\frac{\pi^8}{9M^9} + \sigma_D^2\frac{\pi^6}{7M^7}\right) \\ P_{2\text{-}1^3mb} &= d_5^2\left(\sigma_Q^2\,\frac{\pi^{10}}{11M^{11}} + \sigma_D^2\frac{\pi^8}{9M^9}\right) \end{aligned} \quad (4)$$

where $\sigma_Q^2 = [\Delta/(2^B - 1)]^2/12$ is the power of the last-stage quantization error (Δ stands for the last-stage quantizer full-scale) and σ_D^2 represents the DAC-induced error power. Note that this error is attenuated by M^9 in the 2-1^3*mb*.

2.1 Integrator weight optimization

Whatever set of coefficients (integrator weights in Fig.2 and 3) fulfilling the relationships in Table 1 and 2 leads to the expressions in eq.(3). Nevertheless, the following considerations must be taken into account in actual implementations:

- The level of the signal transferred from one stage to the next in the cascade must be low enough to avoid overloading the latter.

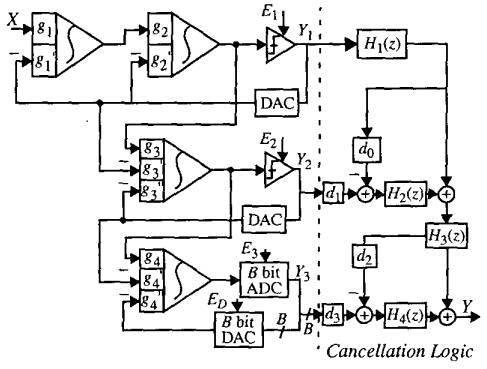

Fig. 2: 4th-order 2-1-1 cascade multibit ΣΔM (2-1^2*mb*).

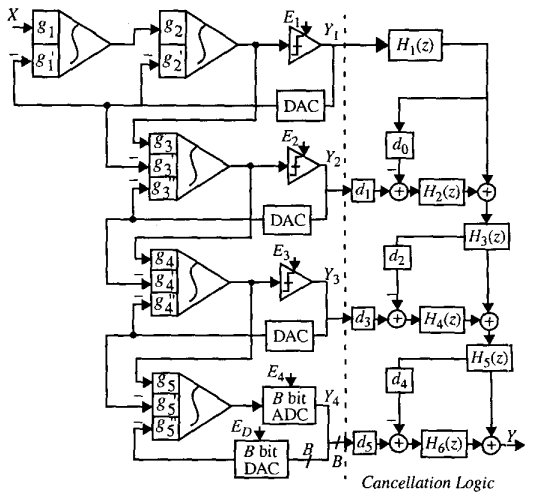

Fig. 3: 5th-order 2-1-1-1 cascade multibit ΣΔM (2-1^3*mb*).

TABLE 1: Digital transfer functions and relationships for the 2-1^2 ΣΔM.

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - \frac{g_3'}{g_1g_2g_3}$	$g_1' = g_1$
$H_2(z) = (1-z^{-1})^2$	$d_1 = \frac{g_3''}{g_1g_2g_3}$	$g_2' = 2g_1'g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3''g_4$
$H_4(z) = (1-z^{-1})^3$	$d_3 = \frac{g_4''}{g_1g_2g_3g_4}$	

TABLE 2: Digital transfer functions and relationships for the 2-1^3 ΣΔM.

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - \frac{g_3'}{g_1g_2g_3}$	$g_1' = g_1$
$H_2(z) = (1-z^{-1})^2$	$d_1 = \frac{g_3''}{g_1g_2g_3}$	$g_2' = 2g_1'g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3''g_4$
$H_4(z) = (1-z^{-1})^3$	$d_3 = \frac{g_4''}{g_1g_2g_3g_4}$	$g_5' = g_4''g_5$
$H_5(z) = z^{-1}$	$d_4 = 0$	
$H_6(z) = (1-z^{-1})^4$	$d_5 = \frac{g_5''}{g_1g_2g_3g_4g_5}$	

- The output swing required for the integrators, which depends on their weights as well as on the input level, must be physically achievable. In SC implementations this limit is determined by the supply voltages.
- Digital coefficients d_3 and d_5, which amplify the last-stage quantization error in eq.(3), should be as small as possible.

Additional considerations in order to simplify the design are:

- Digital coefficients should be 0, ±1 or multiple of 2.
- Multibit quantizer gain must be such that the loop gain of the last stage equals unity. Moreover, it should not be too large in order

to simplify the design of the multibit quantizer.

Table 3 presents good selections of the integrator weights of the 2-1^2*mb* and 2-1^3*mb*, for which the output swing requirement is reduced to only the reference voltages. In addition, in both cases the last-stage quantization error is amplified only by 2, $d_3 = d_5 = 2$ in eq.(3). This means a systematic loss of resolution of 6dB (1bit) respect to the ideal case given in eq.(1). However, this loss is small when compared to that caused by stabilization and non-linearity correction mechanisms used in other approaches [1]. Another 5th-order multibit cascade we initially considered, a 2-2-1*mb* ΣΔM, was discarded at this point because the set of coefficients required to avoid overloading lead to $d_5 = 8$ (3bit systematic loss).

TABLE 3: Analog and digital coefficients in Fig.2 and 3. Shaded cells correspond to the 2-1^3*mb* modulator.

g_1	0.25	0.25	g_4	2	0.5	d_0	-1
g_1'	0.25	0.25	g_4'	1	0.5	d_1	2
g_2	1	1	g_4''	1	0.5	d_2	0
g_2'	0.5	0.5	g_5	-	2	d_3	2
g_3	1	2	g_5'	-	1	d_4	0
g_3'	0.5	1	g_5''	-	1	d_5	2
g_3''	0.5	1					

These coefficients present two additional advantages:

- Because the largest weight in all three-weight integrators can be easily obtained as a combination of the others, an SC implementation will only require two-branch integrators. Note that only one branch is needed for the first integrator.
- The total number of unitary capacitors is only 16 for the 2-1^2*mb* and 19 for the 2-1^3*mb* modulator, smaller than in other cascade ΣΔMs – 29 unitaries in [5] and [8], and 44 in [6].

3. CIRCUIT NON-IDEALITIES

Except for the DAC-induced errors, the architectural study in Section 2 assumes ideal conditions. Nevertheless, circuit imperfections degrading the ΣΔM performance must be taken into account in practice. These non-idealities can be grouped in two categories:

- those affecting the quantization noise transfer function, whose effect strongly depends on the architecture considered, for instance integrator leakage and weight mismatching, and
- those that can be modeled as an error source at the first integrator; such approximation is justified by the fact that the contribution of remaining integrators is attenuated by increasing powers of the oversampling ratio. This is the case of thermal noise, defective settling in integrators, etc.

3.1 Integrator leakage and weight mismatching

The ideal study developed in Section 2 assumes that the relationships of Table 1 and 2 are fulfilled and that the transfer function of the integrators is exactly $z^{-1}/(1-z^{-1})$. However, these assumptions are not valid in practice:

- On the one hand, actual values of integrator weights differ from nominal ones due to mismatch in capacitors ratios.
- On the other, the integrator transfer function above is modified by the finite DC-gain of the amplifiers.

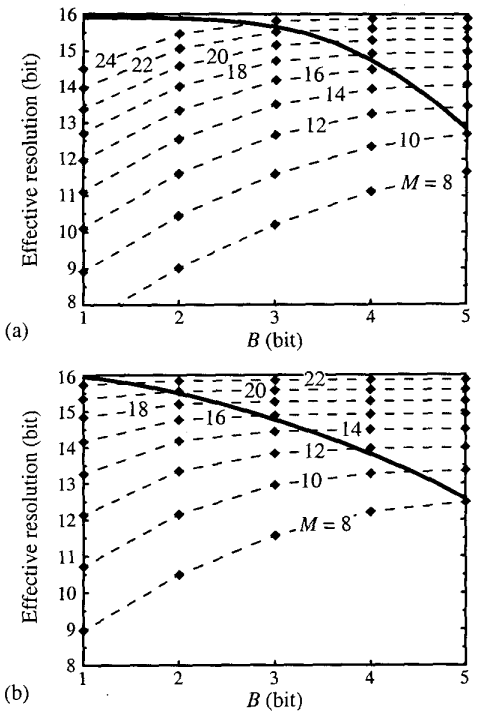

Fig. 4: Modulator resolution vs. last-quantizer resolution for: (a) 2-1^2*mb* ΣΔM and (b) 2-1^3*mb* ΣΔM.
(A_v = 2500, weight mismatch σ = 0.1%, and DAC *INL* = 0.4% FS)

Both non-idealities result in an incomplete cancellation of the quantization error of the former stages and degrade the modulator *DR* [9]. Analysis shows that the extra in-band error power due to these non-idealities is:

$$\Delta P \approx \sigma_C^2 \left[\frac{(g_1 + g_2 + g_2')^2}{A_v^2} \frac{\pi^2}{3M^3} + \varepsilon_1^2 \frac{\pi^4}{5M^5} \right] \qquad (5)$$

where A_v stands for the opamp DC-gain, ε_1 refers to mismatching in weights g_1, g_2, g_3 and g_3'', and $\sigma_C^2 = \Delta^2/12$ is the quantization error power of a single-bit quantizer.

Note that these extra error contributions can in practice mask those in eq.(4), since they are only attenuated by M^3 and M^5. Fig.4 shows simulation results for the effective resolution of the 2-1^2*mb* and 2-1^3*mb* modulators when varying the last-stage quantizer resolution *B*, with *M* acting as a parameter (depicted over each curve). Note that curves saturate in the presence of these non-idealities, leading to a practical limit for the use of multibit quantization – grossly estimated by the thick solid line. Increasing *B* over this limit would not further improve the modulator *DR*. Nevertheless, resolutions below this limit are enough to significantly relax the circuit requirements with respect to single-bit approaches.

3.2 Other circuits imperfections

Different [*M*, *B*] pairs can be a priori selected from Fig.4 for the 2-1^2*mb* and the 2-1^3*mb* modulators, in order to fulfil specifications of 14bit@4.4MS/s. Nevertheless, as operation frequencies increase

in ΣΔMs, the defective settling of SC integrators becomes one of the dominant errors limiting the modulators performance. Thus, the final choice among possible [*M*, *B*] pairs must be done in practice considering the opamp dynamic requirements involved. Table 4 shows an estimation of the required opamp bandwidth (*GBW*) for the different [*M*, *B*] pairs obtaining >13bit for both modulators. $M = 16$, $B = 4$ for the 2-1^2*mb* modulator and $M = 14$, $B = 3$ for the 2-1^3*mb* are the less demanding pairs for 14bit resolution.

Note that multibit quantization significantly relaxes the dynamic requirements with respect to a single-bit approach. For instance, a 2-1^2 modulator with single-bit quantization would require $M = 22$ to obtain 14bit resolution. This higher *M* would lead to an increase of ~35% on the power consumption per opamp.

TABLE 4: Estimated opamp *GBW* for operation at 4.4MS/s.

	2-1^2*mb*		2-1^3*mb*	
~13bit	$M = 12, B = 4$	225MHz	$M = 12, B = 2$	225MHz
	$M = 16, B = 2$	300MHz	$M = 14, B = 1$	275MHz
~14bit	**$M = 16, B = 4$**	**300MHz**	**$M = 14, B = 3$**	**275MHz**
	$M = 22, B = 1$	425MHz	$M = 16, B = 1$	300MHz
~15bit	$M = 20, B = 3$	400MHz	$M = 18, B = 2$	350MHz
	$M = 24, B = 2$	475MHz	$M = 20, B = 1$	400MHz

The overall influence of circuit imperfections on the modulator performance has been evaluated using SDOPT [9], a sizing tool for SC ΣΔMs. This tool combines accurate analytical expressions for each error contribution and statistical optimization, what allows us to find optimized, non-oversized specifications for the building blocks. Table 5 summarizes the circuit requirements providing 14bit@4.4MS/s for both architectures, taking into account the different error contributions (e.g., quantization and thermal noise, settling error, capacitor mismatching, finite opamp DC-gain).

Fig.5 shows behavioral simulation results using ASIDES [9] for the signal-to-(noise+distortion) ratio *SNDR* of both modulators in the presence of the circuits imperfections in Table 5. The maximum *SNDR*, obtained for a -5dB input level, is 80.5dB for the 2-1^2*mb* and 79dB for the 2-1^3*mb*. The *DR* is 86dB and 84.5dB, respectively.

These results present both architectures as good candidates to obtain high-resolution, high-speed operation in xDSL applications, with a moderate power consumption. In fact, with the explored modulators, DAC non-linearities up to 0.4%FS can be tolerated with moderate requirements for the building blocks.

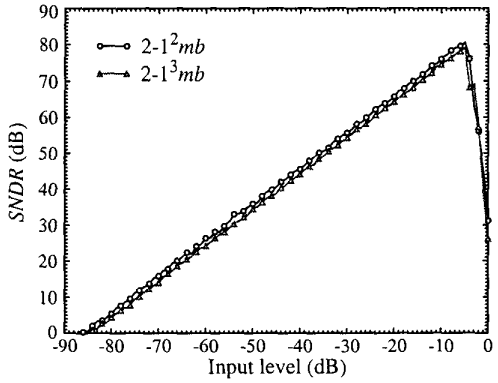

Fig. 5: *SNDR* as a function of the input level.

TABLE 5: Modulator sizing results.

SPECS: 14bit@4.4MS/s		2-1^2*mb*	2-1^3*mb*	Unit
MODULATOR	Oversampling ratio	16	14	
	Sampling frequency	70.4	61.6	MHz
	Reference voltages	±1	±1	V
INTEGRATORS	Sampling capacitor	0.5	0.5	pF
	Unitary capacitor	0.5	0.5	pF
	Sigma	0.1	0.1	%
	Capacitor non-linearity ≤	25	25	ppm/V
	Bottom parasitic capacitor	20	20	%
	Switch ON resistance ≤	0.2	0.2	kΩ
OPAMPS	DC-gain ≥	68	68	dB
	DC-gain non-linearity ≤	20%	20%	V^{-2}
	Transconductance ≥	3.0	2.25	mA/V
	Maximum output current ≥	1.1	0.9	mA
	Differential output swing ≥	±1	±1/±2*	V
COMPARATORS	Hysteresis ≤	20	20	mV
A/D/A CONVERTER	Resolution	4	3	bit
	Non-linearity (*INL*) ≤	0.4%FS	0.4%FS	
Dynamic range		87.7dB (14.3bit)	86.4dB (14.1bit)	
Quantization noise		-93.5dB	-91.5dB	
Thermal noise		-95.9dB	-95.5dB	
Incomplete settling noise		-102.3dB	-102.4dB	
Harmonic distortion		-101.1dB	-101.1dB	

*. Only third integrator needs ±2V output swing

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