IC design for spread spectrum communication exploiting chaos

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Abstract - This paper presents a 2.4μm CMOS IC prototype which includes a programmable chaotic generator and some interface circuitry for chaotic encryption. It realizes a member of the family of the canonical Chua's state equation. It exhibits several bifurcation parameters by changing a few external bias currents and can be used for the chaotic encryption of audio signals.

I.Introduction

This paper follows a previous paper of the authors in [1]. There the fundamentals to design chaotic oscillators using *Gm-C* techniques were established and a IC prototype of the Chua's circuit built. It was able to generate a number of chaotic oscillators by the first time using a fully monolithic continuous time IC. However, its controllability was rather tricky. Hence, it was neither convenient for experimental demonstration of chaotic phenomena nor for chaotic encryption.

This paper presents a new chaotic CMOS chip also in 2.4μm technology. The new chip has much better controllability than the previous. We present its architecture and a number of measurements to illustrate its performance.

II.Chip Architecture

Fig.1 shows the chip architecture which comprises the following blocks:

- A core *Gm-C* chaotic oscillator.
- A *Gm-C* reference integrator.
- Three voltage buffers.

As Fig.1 illustrates, the chip has 14 pins grouped as follows:

- 2 supply voltages.
- 1 analog ground.
- 3 control inputs (low impedance).
- 2 tuning pins.
- 3 unbuffered output pins (one per state variable).
- 3 buffered output pins (one per state variable).

As stated in [1], the design of the monolithic Chua's oscillator is reduced to transistor level implementation of one single transconductance amplifier of g_{mu} gain and a nonlinear transconductor. The transconductor unit has a folded-cascode structure,

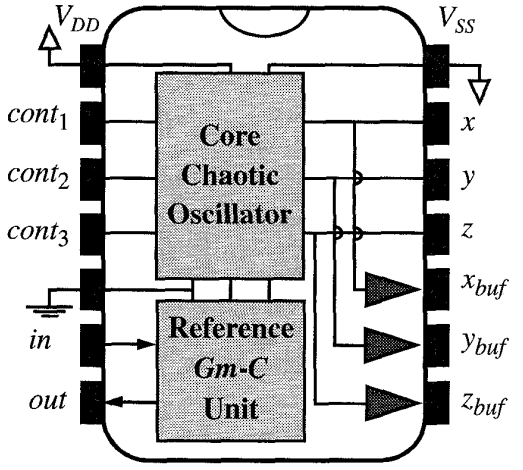

FIGURE 1. Chip architecture.

whose input stage presents a linearization scheme through source degeneration [2] characterized by an ample range of linearity in the voltage-current conversion, low systematic offset, and very high output resistance. The transconductance value is controlled by the biasing current I_{cont1} applied to pin $cont_1$. The nonlinearity of the characteristics is less than 1.0% error in the input voltage ranging from −1.5v to 1.5v, assuming a symmetrical biasing of ± 2.5v. Obviously, proper operation of the circuit implies that the chaotic attractor be comprised inside this range.

The nonlinear transconductor has been implemented via the cascaded connection of a unit transconductor and a current-mode PWL block, as explained in [1] and [3]. Fig.2(a) and (b) show the variation of the nonlinear characteristics for different slopes s_0 and s_1 of the central and outer pieces, respectively. They can be externally controlled through biasing currents I_{cont2} and I_{cont3} applied to pins $cont_2$ and $cont_3$. The values of these currents can be regarded as the cryptographic key for the secure communication scheme.

III.Chip Measurements

Figs.6 and 7 show a biffurcation sequence obtained by changing the biasing current I_{cont2}. A double scroll is obtained through a period-doubling route to chaos. A Rossler-like chaotic attractor and several periodic windows are observed as well.

Fig.3 and Fig.4 demonstrate the feasibility of

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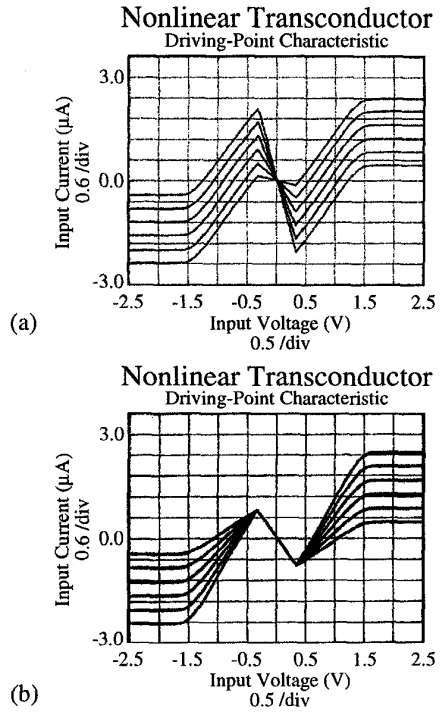
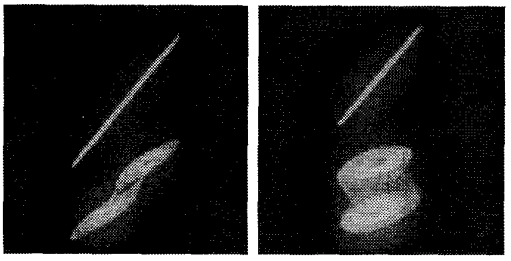


FIGURE 2. Nonlinear Transconductor. Variation of the PWL characteristics with: (a) the central slope, s_0 (control variable I_{cont2}); and (b) the outer slopes, s_1 (control variable I_{cont3}).

chaotic synchronization between two of the manufactured IC prototypes. Fig.3(a) considers a linear diffusion coupling between equivalent state variables of the two chaotic oscillators [4]. It shows the phase plots obtained from a y-coupled experimental set-up, built in practice by inserting an R_y linear resistor between the y terminals of both prototypes (see Fig.1). It was found that whenever the coupling resistance is $R_y < 27k\Omega$, the (x_1, x_2) phase plot follows a nearly perfect straight line, thus confirming synchronization in spite of the chaotic behavior exhibited by the oscillators, as the (x_1, z_1) phase plot illustrates. A similar set-up was built by inserting an R_x linear resistor between the x terminals of the oscillators, thus leading to an x-coupled system. In this case, trajectories of both circuits approach each other asymptotically if $R_x < 745k\Omega$, for the same internal configurations as before. A z-coupled configuration was also built in the laboratory, but, in this case, the system exhibits sporadic losses of synchronization.

Fig.3(b) considers a drive-response scheme as originally proposed by Pecora and Carroll [4]. It shows the phase plots obtained from a x-drive experimental set-up, built by inserting a voltage buffer from the x terminal of the driving prototype to the same terminal at the receiving system. As can be seen from the (y_1, y_2) phase plot, nearly ideal synchronization is obtained. The same conclusion also applies when considering a y-drive scheme, but not for a z-



(a) (b)

FIGURE 3. (a) y-coupled synchronization results. Hor. axis: x_1. Vert. axis: x_2 at the top, z_1 at the bottom. (b) x-drive synchronization results. Hor. axis: y_1. Vert. axis: y_2 at the top, x_1 at the bottom.

drive configuration as predicted by theory [4]. Fig.4 illustrates the performance of the whole secure communication scheme. Input signal (Fig.4(a)) consists of a segment of speech. The worst-case signal to noise ratio of the recovered signal (Fig.4(b)) is greater than +40dB (this occurs at very low frequencies) with less than -0.2dB loss of the input signal power. At higher frequencies, the signal-to-noise ratio rises up to +60dB, while retaining similar losses at the receiver. As can be seen from Fig.4, the transmitted signal (Fig.4(c)) keeps no resemblance to the information content.

IV.References

[1] A. Rodríguez-Vázquez and M. Delgado-Restituto: "CMOS Design of Chaotic Oscillators Using State Variables: A Monolithic Chua's Circuit". *IEEE Transactions on Circuits and Systems* II, Vol.40, N.10, pp. 596-613, Oct. 1993.

[2] F. Krummenacher and N. Joehl: "A 4MHz CMOS Continuous-Time Filter with On-Chip Automatic Tunings". *IEEE J. Solid-State Circuits,* SC-23, pp. 750-758, 1988.

[3] M. Delgado-Restituto and A. Rodríguez-Vázquez: "Switched-Current Chaotic Neurons". *Electronics Letters*, Vol.30, N.5, pp. 429-430.

[4] M. Ogorzalek: "Taming Chaos--Part I: Synchronization". *IEEE Transactions on Circuits and Systems* I, Vol. 40, N.10, pp. 693-699, Oct. 1993.

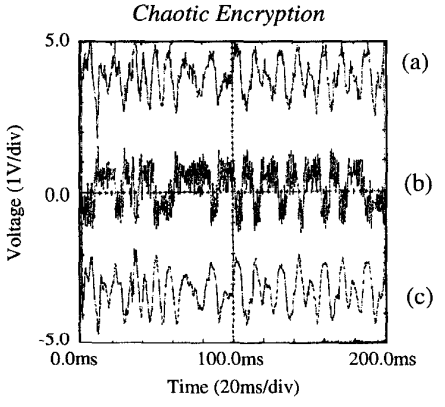
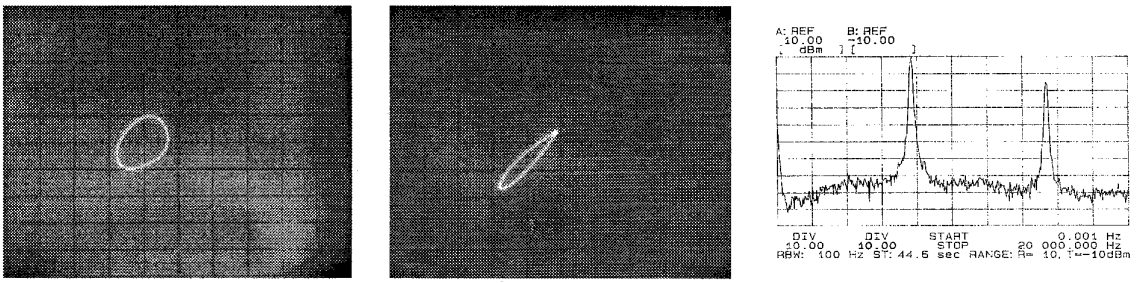
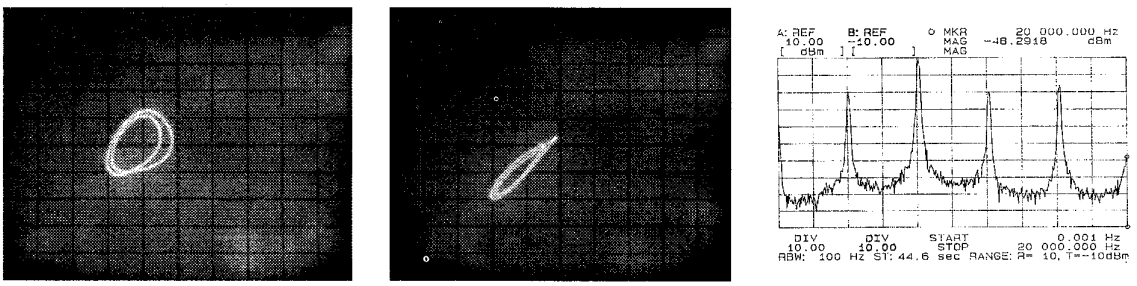


FIGURE 4. Audio Transmission System.



(a)



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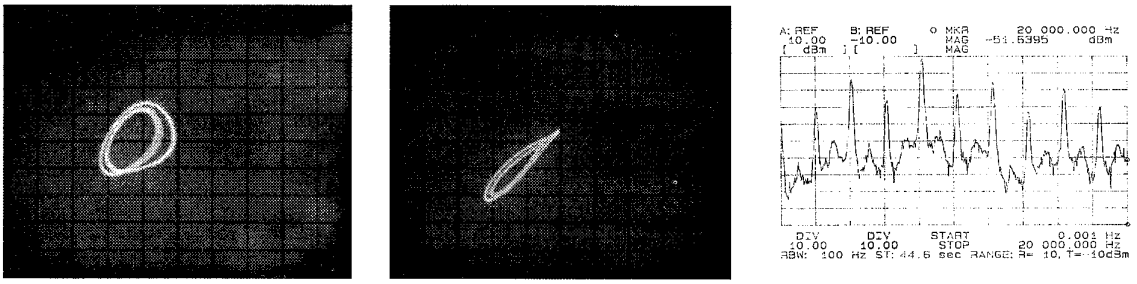
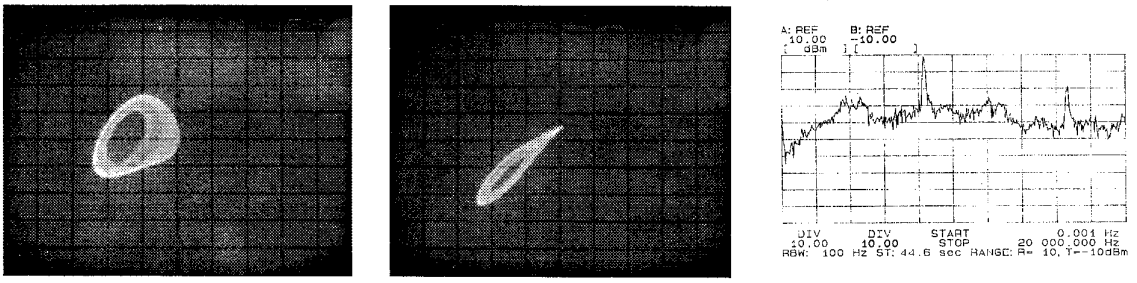
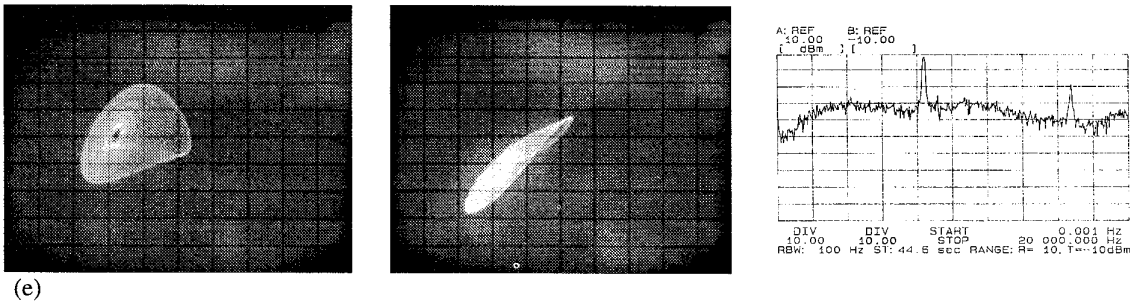


(c)

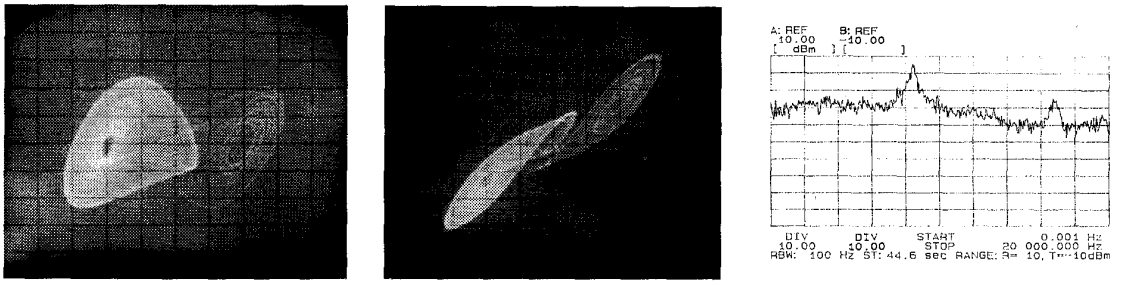


(d)



(e)

FIGURE 5. Experimental Lissajous figures (projections onto the (x, y) and (x,z) planes), and power spectra for:
(a) $I_{cont2} = 1.0\ \mu A$; **(b)** $I_{cont2} = 1.05\ \mu A$; **(c)** $I_{cont2} = 1.125\ \mu A$; **(d)** $I_{cont2} = 1.2\ \mu A$; **(e)** $I_{cont2} = 1.35\ \mu A$.



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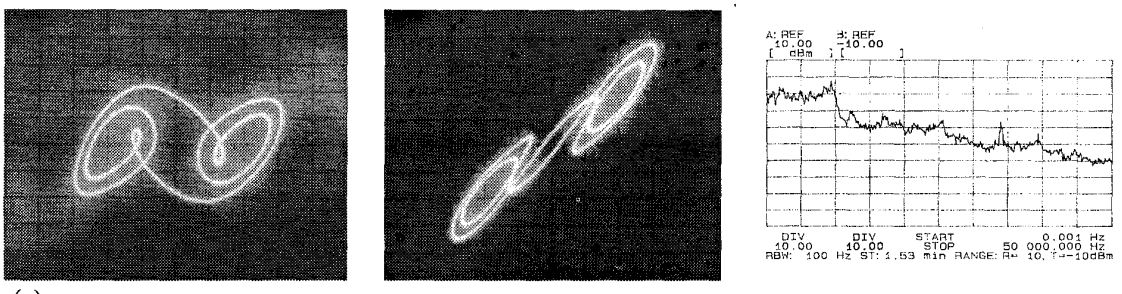

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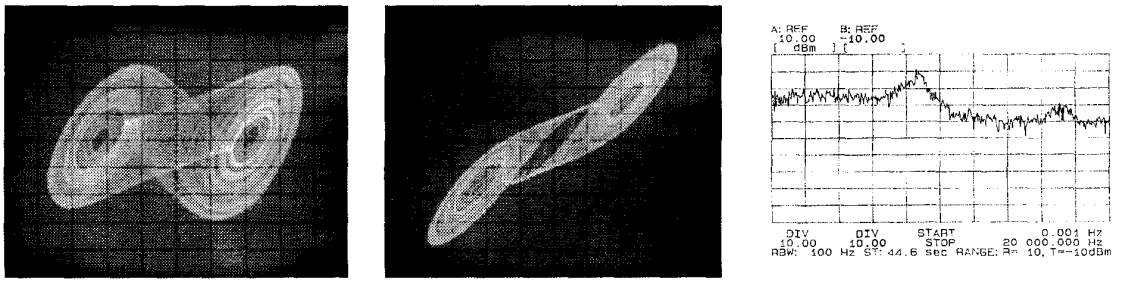

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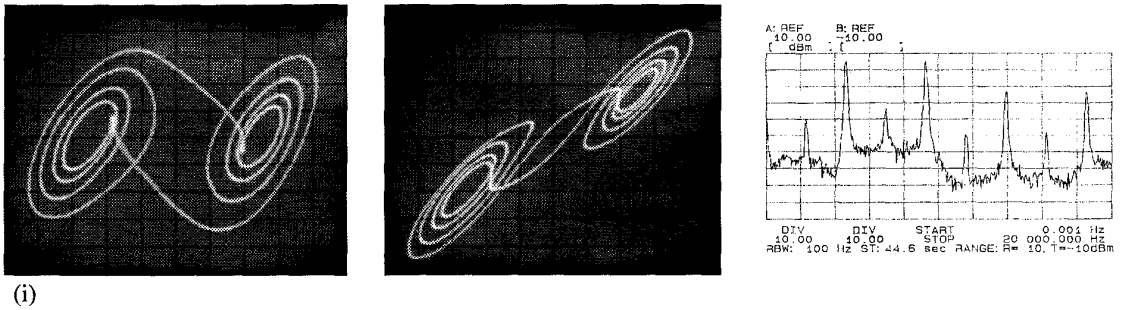
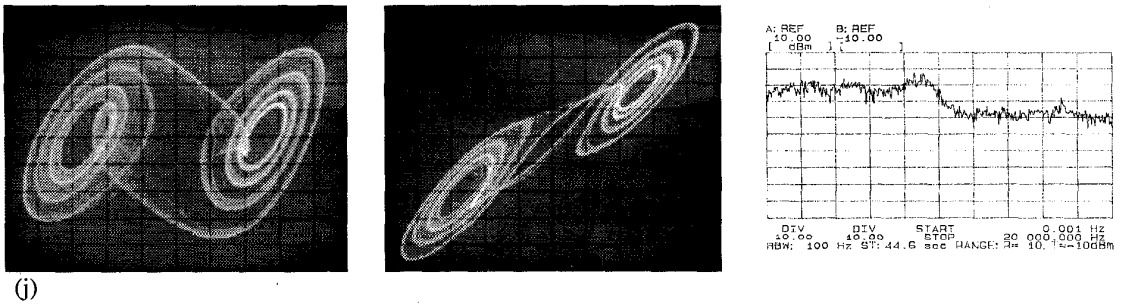


(i)



(j)

FIGURE 6. Experimental Lissajous figures (projections onto the (x, y) and (x,z) planes), and power spectra for:
(f) $I_{cont2} = 1.52\ \mu A$; **(g)** $I_{cont2} = 1.67\ \mu A$; **(h)** $I_{cont2} = 1.7\ \mu A$; **(i)** $I_{cont2} = 1.912\ \mu A$; **(j)** $I_{cont2} = 1.97\ \mu A$.