Self-calibration of Neural Recording Sensors

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***Abstract*—This paper reports a calibration system for automatically adjusting the bandpass and gain characteristics of programmable ExG sensors. The calibration mechanism of the bandpass characteristic is based on a mixed-signal tuning loop which uses as feedback signal the output of the data converter following the signal conditioning of the ExG sensor. Intended high-pass and low-pass frequency poles of the transfer function are injected into the loop by means of a direct frequency synthesizer followed by a smoothing atenuator.**

I. Introduction

The analog front-end (AFE) of modern biopotential ExG is typically composed of a signal acquisition stage and a signal conditioning circuit (see Fig. 1). The signal acquisition stage consists of a low noise amplifier (LNA) which boosts the captured biopotential and compensate for the imperfections of the tissue-electrode interface, including dc drifts and gain errors as of the variable contact impedance. The signal conditioning circuitry, formed by a bandpass filter and a programmable gain amplifier (PGA), adjusts the spectral band and amplification level of the sensor so that the conditioned signal fits in the dynamic range of subsequent processing stages. The proper setting of these parameters is particularly relevant in neural recording interfaces in order to improve the selectivity and specificity of the measurements and, thereof, the performance of the therapeutic device or the brain-machine interface that make use of the sensor. However, due to its circuit implementation, they usually rely on circuit components that are process dependent, which introduces uncertainty about the final value. This is the case, for example, of those circuit solutions that implement large feedback resistors by means of parasitic transistors structures [1], and where the final value can differ up to 400% from the nominal one.

In most commercial devices, the adjustment of the bandpass characteristics and gain of the signal conditioning circuit is done during sensor fabrication and involves the use of high precision off-the-shelves components or the application of trimming techniques [2]. This, however, increases production costs and lacks adaptability against changing environmental conditions (like tissue-electrode interface degradation or electrode displacement, for example). In other realizations, the implementation of the analog conditioning circuit is relaxed and the frequency selection task is translated to digital domain [3]. In this case, high resolution data converters with input ranges and bandwidths much wider than the signal of interest are usually required, thus leading to bulky digital processors and increased complexity and power in the conversion stage,

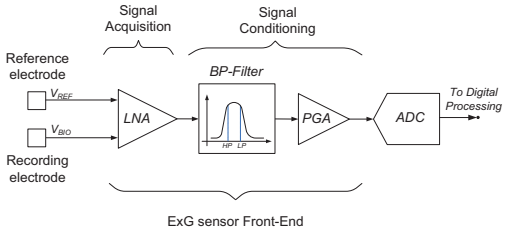

Fig. 1. Front end of a biopotential ExG sensor.

which are potentially unsuitable for large sensor arrays and low power solutions. In a third approach, the analog signal conditioning circuit is endowed with programming capabilities so that both signal filtering and amplification can be independently adjusted [1], [4], [5]. This favors to keep the resolution of the following data converter low and reduce the area and power consumption of the sensor. However, no automatic mechanism has been proposed so far for the setting of the programming variables and, in practice, the definition of the sensor front-end transfer characteristic has to be defined by inspection. For large sensor arrays, this may be a painful and difficult task, particularly, if they are implanted.

To solve this issue, this paper proposes a calibration system for automatically adjusting the bandpass and gain characteristics of programmable ExG sensors. After defining the target frequencies of the transfer function poles, the system runs an automatic foreground calibration procedure which seeks for the filter programming settings that, taking into account technology deviations of circuit components, better approximate the desired passband. Additionally, the system offers a background procedure for the calibration of the voltage gain of the sensor. The purpose is to amplify the acquired biopotential so as to maximally cover the input range of the following data converter. This feature grants dynamic adaptation against variations in the tissue-electrode interface and makes the sensor essentially patient-independent.

The paper is organized as follows. Section II shows the architecture of the proposed calibration system and presents the procedures for adjusting the passband and gain characteristic of a programmable ExG sensor. After describing in Section II-B the circuit implementation details, IV presents a silicon implementation of a neural recording channel which employs the proposed calibration system. The calibration procedure is illustrated by showing the adjustment of the channel configured for the detection and characterization of action potentials. Finally, Section V concludes the paper.

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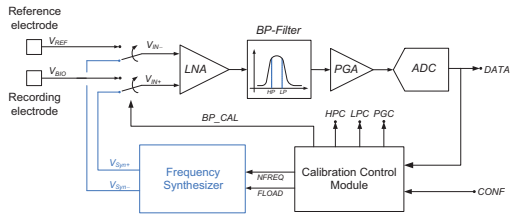

Fig. 2. Calibration system in a sensor AFE.

II. Calibration System and Procedures

Fig. 2 shows the architecture of the proposed calibration system for tuning the analog front-end of a biopotential ExG sensor. It is based on a mixed-signal control loop which uses as feedback signal the output of the data converter following the signal conditioning circuit. Controlled signals are digital words which define the positions of the high-pass (HP) and low-pass (LP) corners of the bandpass filter (vectors *HPC* and *LPC*, respectively) and the amplification of the PGA (vector *PGC*). The calibration system is composed of a digital module, a frequency synthesizer and a switch arrangement at the input of the AFE controlled by the logic signal *BP_CAL*. The frequency of the tones generated by the synthesizer is defined by a control word, *NFREQ*, provided by the control module at instances of a loading pulse *FLOAD*. As the bandpass filter depend mainly on process variations, it can be calibrated only once at the beginning. Therefore, the frequency synthesizer can be shared between different recording sensors to reduce the area overhead and the calibration would be done switching the input among the channels sharing the synthetsizer.

A. Bandpass calibration

In the case of the bandpass filter, the foreground automatic tuning of the HP and LP poles encompasses three steps, illustrated in Fig. 3. Along the whole process, signal *BP_CAL* is set to '1' and the inputs of the LNA are connected to the output terminals of the frequency synthesizer. For simplicity, in the following description it is assumed that no overlap exists between the tuning ranges of the HP and LP poles.

In the first step, control words *HPC* and *LPC* are initially set to the widest passband possible and the calibration module sends to the frequency synthesizer a *NFREQ* value corresponding to an arbitrary frequency within the target bandpass characteristic. After a PGA calibration process (to maximize the ADC input swing), that will be described later on, the module defines a transient and a measurement period. Once the transient period is over, the module stores the digital peak amplitude V_a detected at the ADC output during the measurement phase.

In the next step, the frequency of the tone generated by the synthesizer is made to coincide to the intended HP pole by setting the proper *NFREQ* value. Initially, the control word *HPC* sets the HP pole to the highest frequency possible and the *LPC* word remains unaltered. Then, the calibration module measures, after a transient phase, the peak amplitude $V_{a,HP}$ detected at the ADC output and compares this value to $\alpha \cdot V_a$, where α is a scaling factor (it amounts $3/4$ in the presented design). If $V_{a,HP}$ is lower than such scaled value, which means

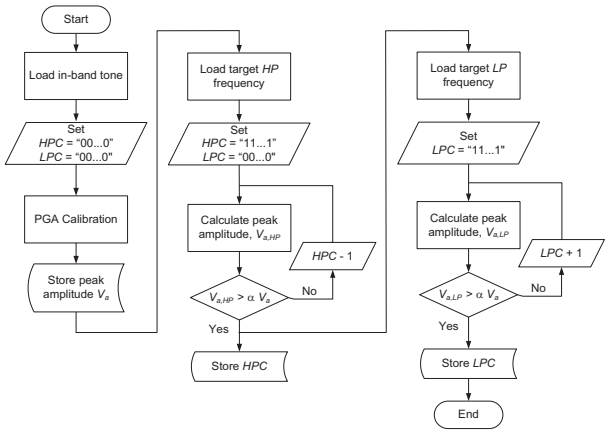

Fig. 3. BP-filter calibration process

that the configured HP pole is above the desired one, the calibration module reduces the *HPC* code by one and starts a new peak amplitude detection process. Otherwise, if $V_{a,HP}$ is higher than $\alpha \cdot V_a$, the calibration module stores the *HPC* value and stops the tuning of the HP pole.

The final step of the passband tuning aims to obtain the *LPC* code that more closely approximates the intended LP pole. In this case, the initial *HPC* code is the one stored in the previous step and the control word *LPC* sets the LP pole to the lowest frequency possible. The procedure is similar to the adjustment of the *HPC* code and it is described in Fig. 3.

B. Programmable gain amplifier calibration

Two cases can be distinguished depending on the state of the logic signal *BP_CAL*. In both configurations, the objective of the calibration process is to adjust the PGA so as its output signal maximally covers the input range of the ADC avoiding saturation. If the signal *BP_CAL* is set to '1', corresponding to the first step of the bandpass calibration procedure, the control word *PGC* is initially set to its mid value "10...0" and a binary search algorithm is run in order to calculate the required peak amplitude V_a. Decisions along the binary search are based on the detection or not of ADC saturation.

In a second case, the signal *BP_CAL* is set to '0' and the PGA operates in background with the inputs of the LNA connected to the electrodes. The calibration process is illustrated in Fig. 4. It starts by setting the PGA to its maximum gain value and calculating the maximum and minimum amplitudes at the output of the ADC during a time interval specified by the user. If any of these amplitudes exceeds given threshold values defined as $\beta \cdot V_{FS}$, for the upper bound, and $\gamma \cdot V_{FS}$, for the lower bound, where V_{FS} is the full-scale of the ADC, the gain of the PGA is reduced by one. This process repeats until no exceeding values are detected. At this point, the last control word *PGC* is stored.

Contrary to the first case in which the input signal to the AFE is a sinusoid generated by the frequency synthesizer, when the calibration procedure operates in background mode the input signal is essentially unpredictable. It is likely peak amplitudes coincide with the presence of action potentials in the neural signal. However, as these signals may have long-

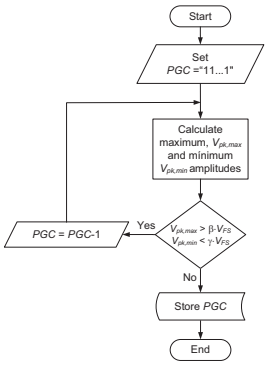

Fig. 4. Functional flow of the PGA calibration with external monitoring process

time silent periods without firing activities, the outcome of the calibration has to be validated by an external user. Anyhow, although the process is not totally unsupervised, the approach still is extremely useful for saving programming tasks in particular for large sensor arrays.

III. Circuit Design

The circuit details of the AFE used as demonstration vehicle of the proposed calibration scheme were presented in detail in [6]. The LNA is implemented by means of a capacitive feedback network where the HP pole is defined by the feedback resistor and feedback capacitor and the LP pole by the transconductance of the OTA and the load capacitance. Both the feedback resistor and the capacitive load are made digitally controllable by means of binarily weighted selectable series and parallel ladders, respectively. The PGA is implemented by a switched-capacitor amplifier placed before the data conversion stage. The amplification of the PGA is defined by the ratio of two capacitors. By implementing the input capacitor as a digitally-controlled capacitive array, this ratio can be made electrically tunable.

Fig. 5 shows the block diagram of the frequency synthesizer used for bandpass calibration. It uses a direct digital synthesis (DDS) approach and consists of a programmable frequency divider which obtains a periodical pulse trail *CLKDIV* from a master clock signal *CLK*; a phase to amplitude converter which generates quantized discrete-time samples of a sinusoidal signal; a digital to analog converter (DAC) which brings this digital waveform to analog domain and builds up a quantized tone; and an adaptation circuit which smooths and attenuates the output of the DAC. The digital implementation shows more robustness against process variations that would not have been guaranteed by an analog-based oscillator solution. The operation of the frequency synthesizer is enabled by a positive pulse *FLOAD* sent by the calibration control module of Fig. 2. The programmable frequency divider essentially consists in a phase accumulator which uses the user-defined digital word *NFREQ* as phase increment. The phase to amplitude converter uses a ROM which stores K equally distributed samples of sine function in the phase interval [0, π/2]. The bit length of these sine samples, P, coincides with the resolution of the DAC. By sequentially reading the ROM upside down at the

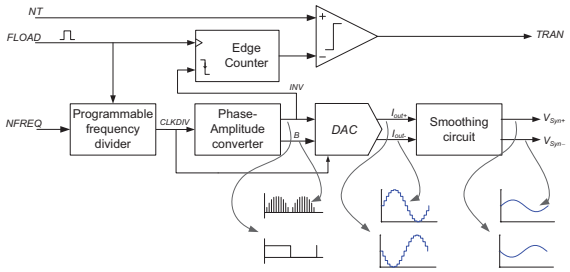

Fig. 5. Schematic of the direct digital synthesizer and representative waveforms along the chain.

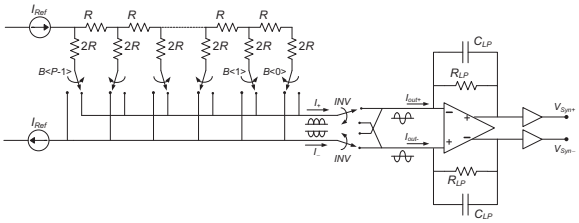

Fig. 6. Schematic of DAC and the smoothing filter used in the DDS architecture.

rate defined by the clock *CLKDIV*, a semiperiod of a digital sine waveform with frequency $f_{DIV}/4 \cdot K$ is generated, where f_{DIV} is the frequency of *CLKDIV*. At every transition between semiperiods, the signal *INV* changes its logic state. When the number of these transitions, as determined by an edge counter, exceeds a user-defined value *NT*, the logic signal *TRAN* turns low. This *NT* value is used as an estimation of the transient period required by the calibration control loop to settle after a change in the *NFREQ* value. Once the transient period is over, the calibration module of Fig. 2 defines a measurement period, which occupies *NM* period of the synthesized tone, to calculate the peak amplitude V_a detected at the ADC output.

Fig. 6 shows the schematic of the DAC and the smoothing filter placed after the phase to amplitude converter. The DAC uses a R-2R ladder structure which is implemented in practice by means of pMOS transistors. Supply currents are obtained by means of unity-gain current mirrors from a single current reference, I_{Ref}. Depending on the sample words $\mathbf{B} < 0, P-1 >$ stored in the ROM, positive and negative currents with identical amplitude are respectively routed to the branches $I_+$and I_-. By means of a quad switch arrangement controlled by the logic signal *INV*, a fully-differential current is generated at the input of a first-order lowpass smoothing filter. This filter, formed by a fully-differential folded-cascode OTA with resistors R_{LP} and capacitors C_{LP} in the feedback loop, converts the input currents into voltages with peak amplitudes given by $R_{LP} \cdot I_{Ref}$. Simple voltage followers take the outputs of the smoothing filter to the inputs $V_{Syn+}$and $V_{Syn-}$of the AFE, as shown in Fig. 2..

IV. Experimental Results

Fig. 7 shows the microphotograph of the proposed calibration system composed by the control module (embedded in the digital section of a recording channel) and the programmable frequency synthesizer. The system, which is part of a 64 channel neural interface for intracortical recordings, has been

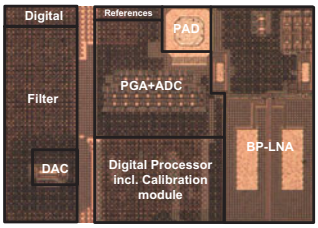

Fig. 7. Microphotograph of the channel and the frequency synthesizer.

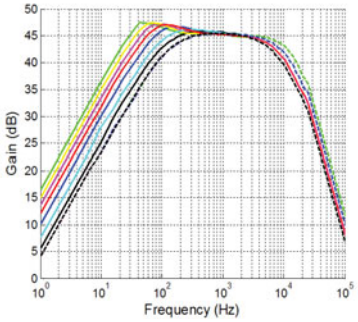

Fig. 8. Experimental frequency response of the neural channel under the different poles configurations.

integrated in a 6M2P 0.13µm standard CMOS technology. The frequency synthesizer is indeed shared by 8 channels in the array (only one shown in Fig. 7) which are sequentially calibrated one after the other. Digital data transfer between the frequency synthesizer and the calibration module is realized by means of buffers tri-state. The input/output terminals of the channels which are not running the calibration procedure are in high impedance.

Every channel has 3-bit for the calibration of the HP pole, 2-bit for the LP pole and 3-bit for the adjustment of the PGA. Fig. 8 shows the frequency response of the AFE under all possible configurations of the control words *HPC* and *LPC*. Measurements show a tuning range for the HP pole from 15 to 232 Hz, while the LP pole can be tuned between 5.2kHz and 10.15 kHz.

Most of the area of the frequency synthesizer is occupied by the smoothing filter, whose lowpass corner can be set either to 1kHz, or to 12 kHz. Only 5 samples of sine information are stored in the ROM of the phase to amplitude converter. The length of the samples and, accordingly, the resolution of the DAC is 6-bit. The biasing current of the DAC, as provided by built-in current reference block, is nominally 50 nA.

Fig. 9 shows the measured ADC output code, as well as the evolution of the control words *HPC* and *LPC*, along the calibration of the channel bandpass characteristic. Seeking for neural spike recordings, the target frequencies for the HP and LP poles are 200 Hz and 7 kHz, respectively. As can be seen, three iterations are needed to identify the code (*HPC* = '101') that better approximates the desired HP pole, whereas two iterations suffice for the LP pole (*LPC* = '10') . In both calculations, the transient and measurement phases per iteration long $NT = NM = 2000$ samples of the synthesized tone.

Fig. 10 shows the measured ADC output code and the value of the *PGC* code along the calibration of the PGA (*BP_CAL* is

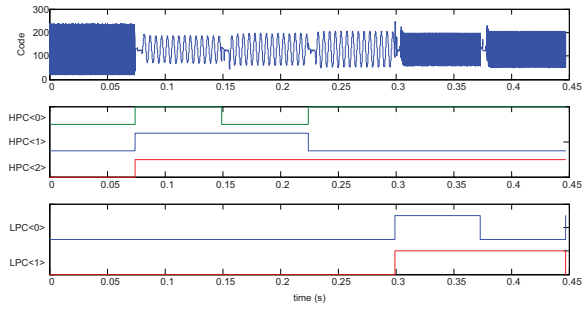

Fig. 9. Temporal evolution during BP-LNA calibration.

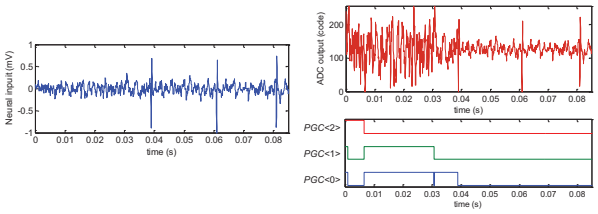

Fig. 10. Temporal evolution during PGA calibration.

set to '0'). The PGA is initially set to its maximum gain value and the algorithm decreases *PGC* every time a saturation is detected at the output of the ADC. A synthetic neural signal provided by a Tektronix AFG3102 arbitrary function generator has been used in this experiment.

V. Conclusions

This paper reports a calibration system for automatically adjusting the bandpass and gain characteristics of programmable ExG sensors. The calibration mechanism of the bandpass characteristic is based on a mixed-signal tuning loop which uses as feedback signal the output of the data converter following the signal conditioning of the ExG sensor. Intended high-pass and low-pass frequency poles of the transfer function are injected into the loop by means of a direct frequency synthesizer followed by a smoothing atenuator.

Acknowledgments

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