A HIGH-PERFORMANCE SIGMA-DELTA ADC FOR ADSL APPLICATIONS IN 0.35μm CMOS DIGITAL TECHNOLOGY

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ABSTRACT: We present a Sigma-Delta modulator designed for ADSL applications in a 0.35μm CMOS pure digital technology. It employs a 4th-order 3-stage cascade architecture including both single-bit and multi-bit quantizers with programmable resolution, which allows us to use only 16 oversampling ratio. Especial emphasis is placed on technology issues, namely: poor analog performance and substrate coupling. The measured performances are 13-bit dynamic range operating at 2MS/s and 12-bit dynamic range operating at 4MS/s. The modulator consumes 77mW from a 3.3-V supply and occupies 1.32 mm^2.

1. INTRODUCTION

The connection in cascade of low-order ΣΔ modulators (ΣΔMs) to build high-order, unconditionally stable architectures, often in combination with robust, calibration-free, multi-bit quantization, has been proven to be a good alternative to achieve the requirements of the xDSL ADCs [1]-[6]. A claimed drawback of these architectures is that they are suitable only in moderate sub-micron analog technologies where the good matching of passive devices, chiefly capacitors, and the obtainable performance of the analog cells, make them power-efficient in comparison with other ΣΔ-based architectures or other types of ADCs. In this context, this paper demonstrates that, through a careful design, the above topologies can also be efficiently implemented in a 0.35μm pure digital CMOS technology. The ΣΔM presented here uses a 4th-order 3-stage cascade multi-bit architecture – the 2-1^2*mb* modulator [1] shown in Fig.1. A detailed discussion on the benefits of the selected topology, as well as on the selection of integrator weights (summarized in Table 1) can be found in [7].

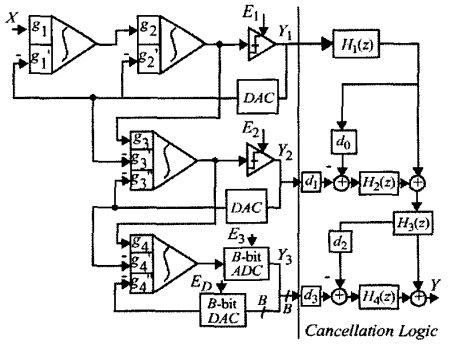

Fig. 1. Block diagram of the 2-1^2mb ΣΔM.

The paper is organized as follows. Section 2 covers the synthesis of the 2-1^2*mb* modulator. Sections 3 describes the design of the modulator building blocks. Finally, Section 4 is dedicated to layout and measurement results.

2. MODULATOR SIZING

The evaluation of the circuit requirements for the 2-1^2*mb* ΣΔM has been done using SDOPT [8], a sizing tool for SC ΣΔMs. This tool combines accurate analytical expressions for each error contribution degrading the modulator performance and statistical optimization, which allows us to find optimized, non-oversized specifications for the building blocks. Table 2 summarizes the circuit requirements providing 14bit@4MS/s. Most significant error contributions are also shown. Note that quantization noise is the main in-band error source (-85dB). The requirements in Table 2 for the integrator and the amplifier apply only to the first integrator in the cascade. However, some specifications, as amplifier DC-gain, transconductance and output current, can be relaxed for the second, third, and fourth integrator, because their in-band error power contributions are attenuated by increasing powers of the oversampling ratio. The same applies for thermal noise, which allows reduction of the unitary capacitor from 0.5pF to 0.25pF for these integrators.

Fig.2 shows the fully differential SC implementation of the 2-1^2*mb* ΣΔM. The first stage is formed by two SC integrators, with one and two input branches, respectively. A single-bit quantizer (comparator) at the end of the first stage, together with two AND gates, provides the feedback signals A_1,B_1 to switch the integrator sampling capacitors to either V_r+ = +1V or V_r- = -1V. Since the circuit is fully differential, the resulting reference voltages are ±2V. The second stage has a two-branch integrator. Although three different weights are needed in this integrator – g_3, g_3', and g_3'' – weight values in Table 1 allow splitting g_3 between the two branches. The same applies for weight g_4 in the fourth integrator. This integrator drives a programmable ADC, whose resolution can be switched between 2 and 4bit for exploration purposes. The third-stage loop is closed through the DAC. The 1-of-16 (4-bit) output code of the last-stage ADC (alternatively 1-of-8 in the 3-bit mode or 1-of-4 in the 2-bit mode) is converted to binary code using a ROM memory, providing outputs $Y_{3,0\text{-}3}$ (alternatively $Y_{3,0\text{-}2}$ or $Y_{3,0\text{-}1}$).

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Table 1. Integrator weights for the 2-1^{2}mb ΣΔM.

g_1	0.25	g_3	1	g_4	2
g_1'	0.25	g_3'	0.5	g_4'	1
g_2	1	g_3''	0.5	g_4''	1
g_2'	0.5				

Table 2. Modulator sizing results.

SPECS: 14bit@4MS/s@1.1V$_p$		2-1^2*mb*
Modulator	Oversampling ratio	16
	Sampling frequency	64MHz
	Reference voltages	±±2V
Integrators	Sampling capacitor	0.5pF
	Unitary capacitor	0.5pF
	Sigma	0.12%
	Capacitor non-linearity ≤	25ppm/V
	Bottom parasitic capacitor	20%
	Switch ON-resistance ≤	250Ω
Opamps	DC-gain	68dB
	DC-gain non-linearity ≤	20%V^{-2}
	Transconductance ≥	2.5mA/V
	Maximum output current ≥	±0.95mA
	Output swing ≥	±2V
Comparators	Hysteresis ≤	30mV
A/D/A Converter	Resolution	4bit
	Non-linearity (*INL*) ≤	0.4%FS
Dynamic range		87.2dB 14.2bit
Quantization noise		-85.0dB
Thermal noise		-94.8dB
Incomplete settling noise		-96.9dB
Harmonic distortion		-99.4dB

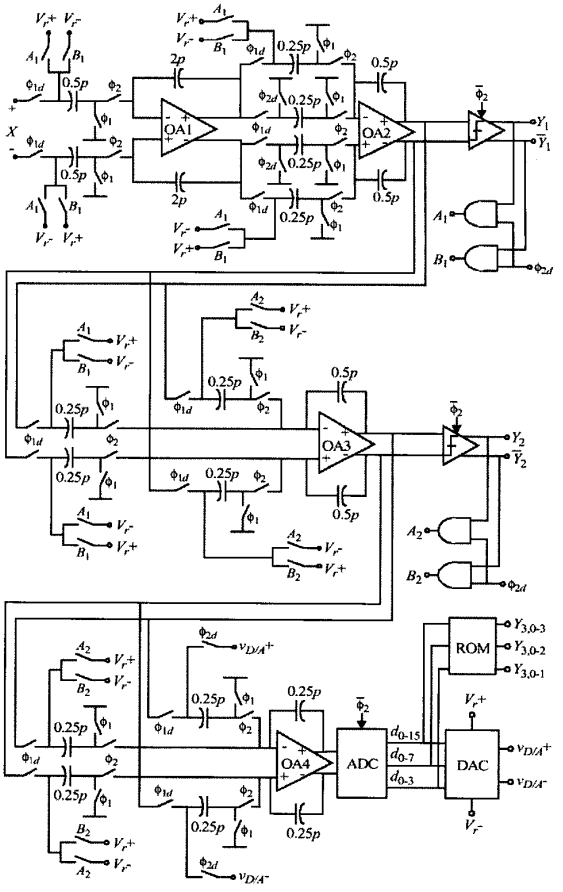

Fig. 2. SC implementation of the 2-1^{2}mb ΣΔM.

The modulator is controlled by two non-overlapped clock-phases. The integrator input signals are sampled during phase ϕ_1 and the algebraic operations are performed during ϕ_2. The comparators and the ADC are activated at the end of ϕ_2 – using its complementary phase as strobe – to avoid any possible interference at the beginning of ϕ_1. In order to attenuate the signal-dependent clock charge injection, delayed versions of the phases, ϕ_{1d} and ϕ_{2d}, are also provided.

The modulator has been extensively evaluated in ASIDES [8], a behavioural simulation tool for ΣΔMs. Fig.3*(a)* shows the signal-to-(noise+distortion)-ratio *SNDR* of the modulator as a function of the input level, when operating with different values of the oversampling ratio (*M*) and the last-stage quantizer resolution (*B*). The maximum dynamic range *DR* is 85.5dB. Fig.3*(b)* shows its output spectrum for a -6dBV@250kHz input tone.

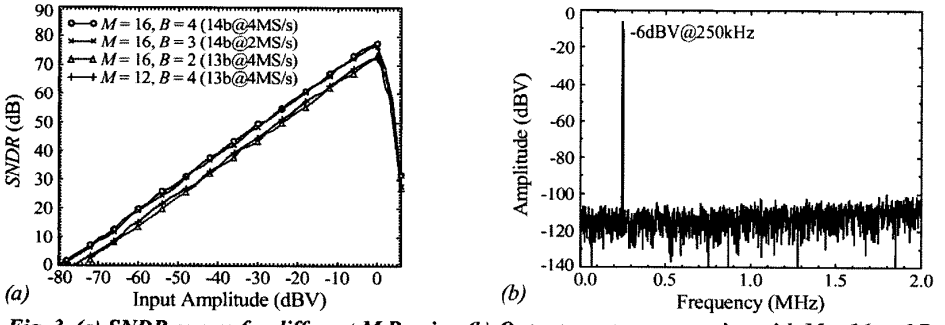

Fig. 3. (a) SNDR curves for different M,B pairs, (b) Output spectrum operating with M = 16 and B = 4.

3. CIRCUIT DESIGN

3.1 Amplifiers

Most important amplifier design aspects are [9]: (a) *Required output swing* which, with the weights in Table 1, is reduced to only the reference voltages. (b) *Open-loop DC-gain*: Simulations with ASIDES show that the 68dB requirement can be relaxed for amplifiers in the second, third and fourth integrator to 62dB, 54dB, and 54dB, respectively. (c) *Dynamics,* influenced by the equivalent capacitive load which is different for each integrator and clock phase.

A two-stage architecture, shown in Fig.4*(a),* was selected for OA1 in order to fulfil its DC-gain requirement. It uses a telescopic first stage and Miller compensation. A single-stage folded-cascode OTA, shown in Fig.4*(b),* has been used in OA2, OA3, and OA4 – enough to accomplish their medium-, low-DC-gain requirements. Although these amplifiers use the same structure, different sizings have been obtained for each of them, in order to fulfil their specifications with a reduced power consumption. The common-mode feedback nets (not shown) are dynamic – neither static consumption nor voltage range problems. The main features of the four amplifiers, sized using FRIDGE [8], are summarized in Table 3.

Table 3. Summarized amplifier performance

	OA1	OA2	OA3	OA4
DC-gain (dB)	80.0	62.8	55.7	62
GB (MHz)	250	311	261	167
PM (Degree)	67	65	71	79
Output swing (V)	±2.5	±3.1	±2.9	±3.1
Transc. (mA/V)		4.2	2.6	5.4
Output current (A)		±0.57	±0.45	±0.84
Slew rate (V/μs)	450	895	706	632
Power cons. (mW)	38.5	4.5	4.0	6.6

3.2 Capacitors and switches

Unitary capacitors have been implemented with a multi-metal sandwich structure, using the five metal layers available in the intended technology. According to previous measurements, the standard deviation of the matching error is 0.12%. The bottom-plate parasitic capacitor, especially important for dynamic requirements, is between 20% - 40% of the nominal capacitance. Due to the high-speed operation of the ΣΔM, finite switch ON-resistance R_{on} is mainly constricted by dynamic considerations. In our case, R_{on} in the range of 250Ω - 300Ω can be tolerated, with a minor degradation of the modulator performance. This value is not too demanding for a CMOS transfer gate in the 3.3-V supply intended technology, so that clock-boosting stages or similar techniques can be avoided.

3.3 Quantization Blocks

Since comparators have to be very fast, although not very precise, a regenerative latch, without pre-amplifying stage is enough to meet the requirements. The same block has been used as the comparator block of the last-stage 4-bit flash ADC, which uses a fully differential SC front-end to compute the difference between the last integrator output signal and the reference signals generated in a resistive ladder. The latter consists of a simple resistor string of 30 unitaries (R = 50Ω) connected between the reference voltages V_r+ = +1V and V_r- = -1V. The same string has been used for the DAC. The value selected for R ensures that settling errors are small enough. Note that we can afford this simple, calibration-free design because cascade multi-bit ΣΔMs show low sensitivity to the non-idealities of the last-stage quantization blocks [8].

4. EXPERIMENTAL RESULTS

Fig.5 shows the layout of the prototype fabricated in a 0.35μm CMOS digital technology with epi conductive substrate. It includes centroid techniques in matched devices, separate analog, digital and substrate biasing, and an extra supply dedicated to the digital output buffers, in order to be able to reduce this supply without affecting the rest of the circuitry during the test phase, thus lowering the power of the switching noise. The modulator occupies 1.32mm^2 without pads and consumes 78.3mW: 60.2mW for the analog blocks, 4.5mW for the digital part, and 13.6mW for the output drivers.

The modulator samples were soldered (without socket) on a two-layer PCB, Fig.6, including separate analog and digital planes, de-coupling capacitors in the supply lines and reference voltages, termination resistors for impedance coupling at the digital output lines and ESD protec-

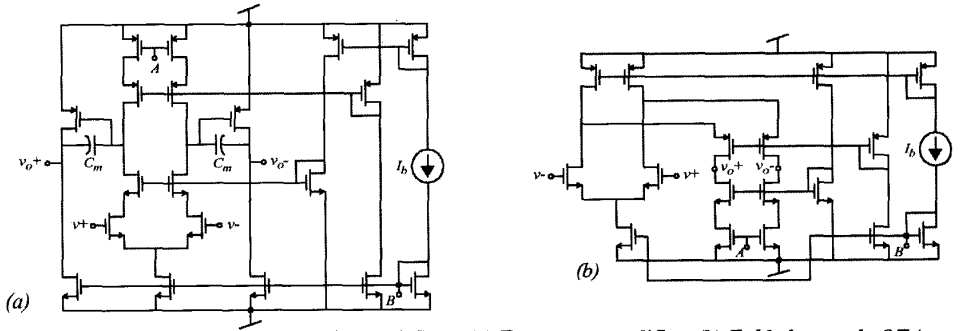

Fig. 4. Schematics of the amplifiers: (a) Two-stage amplifier, (b) Folded-cascode OTA.

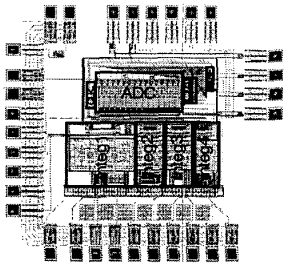

Fig. 5. Layout of the 2-1²mb ΣΔM

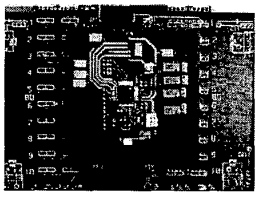

Fig. 6. Two-layer PCB

tions. An external 1st-order low-pass anti-aliasing filter was placed at the modulator input.

Fig.7 shows the measured output spectrum of the complete modulator and those corresponding to the first stage (2nd-order) and to the combination of the first and second stages (3rd-order). Note the increase in the order of the shaping of the quantization noise.

The measured *SNDR* vs. input level are shown in Fig.8 for two different clock frequencies: 35.2MHz and 64MHz, and constant oversampling ratio = 16. Note that the achieved dynamic range is 81dB in the first case and it is 6dB smaller in the second. Our measurements show that this degradation is larger the larger the sampling frequency and that the performance improves when the biasing of the output buffers is lowered. Because of that, such degradation could be due to the switching noise coupled through the highly conductive substrate of the epi technology [10]. Further results in this respect will be presented at the conference. Nevertheless, with the achieved performance, the modulator here compares favorably with the state-of-the-art modulators in Fig.9, especially because previous results have been achieved in analog technologies.

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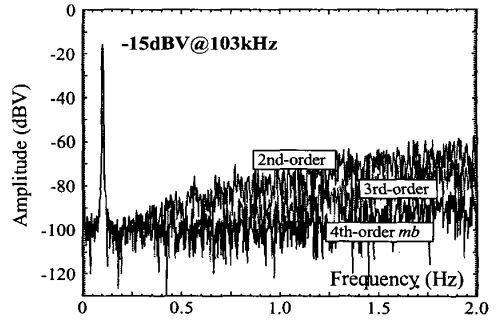

Fig. 7. Measured spectra

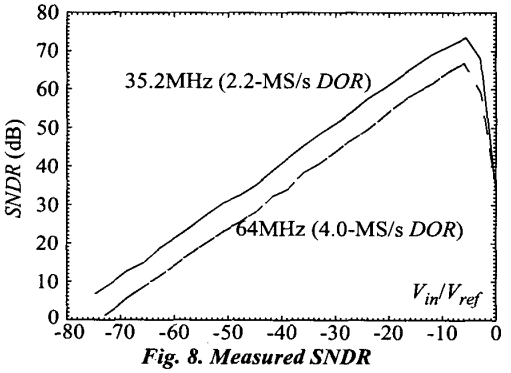

Fig. 8. Measured SNDR

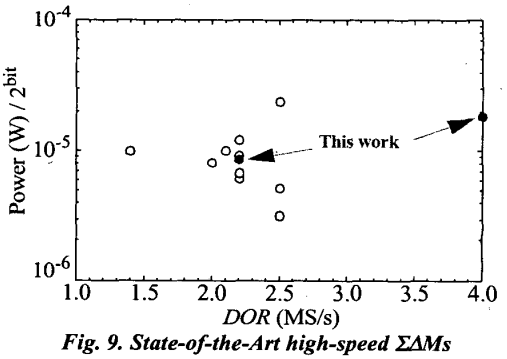

Fig. 9. State-of-the-Art high-speed ΣΔMs

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