# Chapter 11

# Bandpass Sigma-Delta A/D Converters: Fundamentals, Architectures and Circuits

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## 11.1 INTRODUCTION

In last years we have witnessed a growth of the wireless communication market as never before, introducing in our daily live a great number of digital portable gadgets such as cellular phones, digital radio receivers, Global Positioning System (GPS) handheld units, Personal Digital Assistants (PDAs), etc. It is expected that this evolution will continue to do so in the first decade of this century, with the proliferation of new technologies and applications such as Bluetooth, Software-Defined Radios (SDRs), Wireless Local Area Networks (WLANs), etc.

The *wireless revolution* has been partially prompted by the 'vertiginous' scaling-down of microelectronic technologies, which has exponentially increased the capabilities of digital VLSI circuits, making it possible the integration of entire communication systems on the same silicon substrate. Together with reduced priced, size and power consumption, the so-called *Systems-on-Chips (SoCs)* tend to realize more and more functions by a Digital Signal Processor (DSP), thus facilitating the *programmability* and adaptability of these functions to many different radio interface standards [1] – preferably reconfigurable with software [2][3]. For this purpose it would be desirable to place the analog-digital interface as closer to the antenna as possible.

In this scenario, Analog-to-Digital Converters (ADCs) based on BandPass ΣΔ Modulators (BPΣΔMs) are very well suited for the implementation of the front-end of such digital wireless communication SoCs. One of the main advantages of BPΣΔMs as compared to other architectures comes from the fact that they do not need to digitize the whole Nyquist band (from DC to one half of the sampling frequency); instead they digitize just the signal band, thereby requiring much less power consumption to obtain similar dynamic range.

The principle of ΣΔ Modulation (ΣΔM) [4] is extended in BPΣΔMs to bandpass signals, especially but not only, with a narrow bandwidth [5]. Thus, BPΣΔMs have much in common with their lowpass counterparts – whose properties have been covered in previous Chapters of this book. However, there are some issues which are peculiar to BPΣΔ-ADCs. This Chapter is devoted to the description of these issues. In Section 11.2, digital radio receivers are revised, pointing out the necessity for an ADC at the IF location. Section 11.3 and Section 11.4 explain the basic concepts and architectural issues of BPΣΔ-ADCs. The problems derived from circuit implementation are treated in Section 11.5. Finally, Section 11.6 summarizes the performance of state-of-the-art BPΣΔ-ADCs.

## 11.2 THE DIGITAL WIRELESS COMMUNICATIONS UNIVERSE

Since the invention of the cellular concept by Bell Laboratories and the later introduction of the 1st-Generation (1G) (analog) mobile phones in the early 80's, a multitude of wireless communication systems have appeared. As an illustration, Table 12.1 summarizes some significant wireless systems including the 2G and 3G cellular standards as well as others like Bluetooth and WLAN [6]. The table shows the main characteristics of these systems, namely: frequency range, channel spacing, multiple access technique and modulation type. Among other 2G standards, Global System for Mobile communications (GSM) is the most used worldwide. In the case of 3G systems, as they are in their final stage of standardization, there is still an uncertainty about what protocols will dominate the market.

This *wireless communications universe* calls for the need of developing digital transceiver chips capable of operating at different modes with multi-standard support features. The final goal is to allow software-based radios to simultaneously

**Table 12.1:** Summary of digital wireless communication standards.

| Wireless Standard | Type | Access | Modulation Type | Frequency Range (Tx) (MHz) | Frequency Range (Rx) (MHz) | Channel Spacing (kHz) | Data Rate (kb/s) | Peak Power (W) |
|---|---|---|---|---|---|---|---|---|
| AMPS | Cellular1G | FDD | FM | 824-849 | 869-894 | 30 | N/A | 3 |
| GSM | Cellular2G | TD,FDMA /FDD | GMSK | 890-915 | 935-960 | 200 | 270.8 | 0.8-8 |
| IS-54 | | TDMA /FDD | π/4-QPSK | 824-849 | 869-894 | 30 | 48 | 0.8-3 |
| IS-95 | | CDMA | OQPSK | 824-849 | 869-894 | 1250 | 1228 | N/A |
| UMTS | Cellular3G | CDMA | QPSK | 1920-1980 | 2110-2170 | 5000 | 3840 | 0.125-2 |
| DCS-1800 | Cordless | TDMA | GMSK | 1710-1785 | 1805-1850 | 200 | 270.8 | 0.8-8 |
| DECT | | TDMA /TDD | GFSK | 1881-1897 | 1881-1897 | 1728 | 1152 | 0.25 |
| PCS-1900 | Wireless Digital | TDMA | GMSK | 1880-1910 | 1930-1955 | 200 | 270.8 | 0.8-8 |
| DSSS | | CDMA | QPSK | 2400-2483 | 2400-2483 | N/A | 1211 | 1 |
| Bluetooth | | CDMA/FH | GFSK | 2400-2483 | 2400-2483 | 1000 | 1000 | 20dBm |

carry voice, video and data, using a variety of telecommunication systems [3].

### 11.2.1 The ideal digital wireless transceiver

Fig. 12.1 shows the generic block diagram of an ideal digital RF transceiver intended for SDRs. In the receive side, the RF signal coming from the antenna is directly digitized by an ADC. Hence, many functions like frequency tunning and translation, filtering, channel selection and demodulation can be implemented by running software on a general-purpose DSP. A similar reasoning holds in the transmit side. Unfortunately, the transceiver of Fig. 12.1 is unrealizable because the required specifications for both the ADC and the DAC are prohibitively stringent. For instance, the receiver would require realizing the A/D conversion of a signal at 800MHz-2.5GHz (see Table 12.1) with an accuracy of 14-18bit [7]. Hence, a more realistic digital radio transceiver would contain an Analog Signal Processing (ASP) section including signal conditioning, i.e: frequency translation, amplification and filtering. The implementation of these analog functions can be realized in different manners resulting in several Radio Frequency (RF) transceiver architectures. In this Chapter, we are interested in the receiver architectures – analyzed in the following section.

### 11.2.2 Overview of wireless digital radio receiver architectures

Fig. 12.2 shows the simplified block diagram of the most significant digital radio receiver architectures [8]. Fig. 12.2(a) is a *digital superheterodyne* receiver, where the signal is first down-translated to an Intermediate Frequency (IF) – for example 10.7MHz in GSM systems – and then to baseband where it is digitized and demodulated. This is the most conventional architecture. However, it is not appropriate for fully-integrated RF receivers because external narrowband filters with high selectivity, such as ceramic or SAW filters (in both the RF and the IF sections) are required. This problem can be partially solved by using a sufficiently low IF – typically $< 1$MHz – referred to as *low-IF superheterodyne receivers*. In this case the channel-select filters can be implemented using established circuit

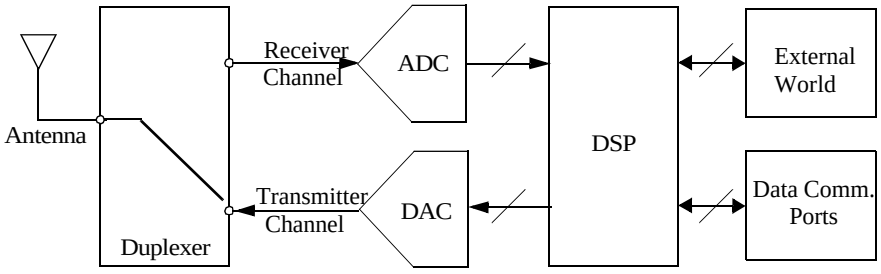



**Figure 12.1:** Ideal wireless transceiver intended for software-defined radios.

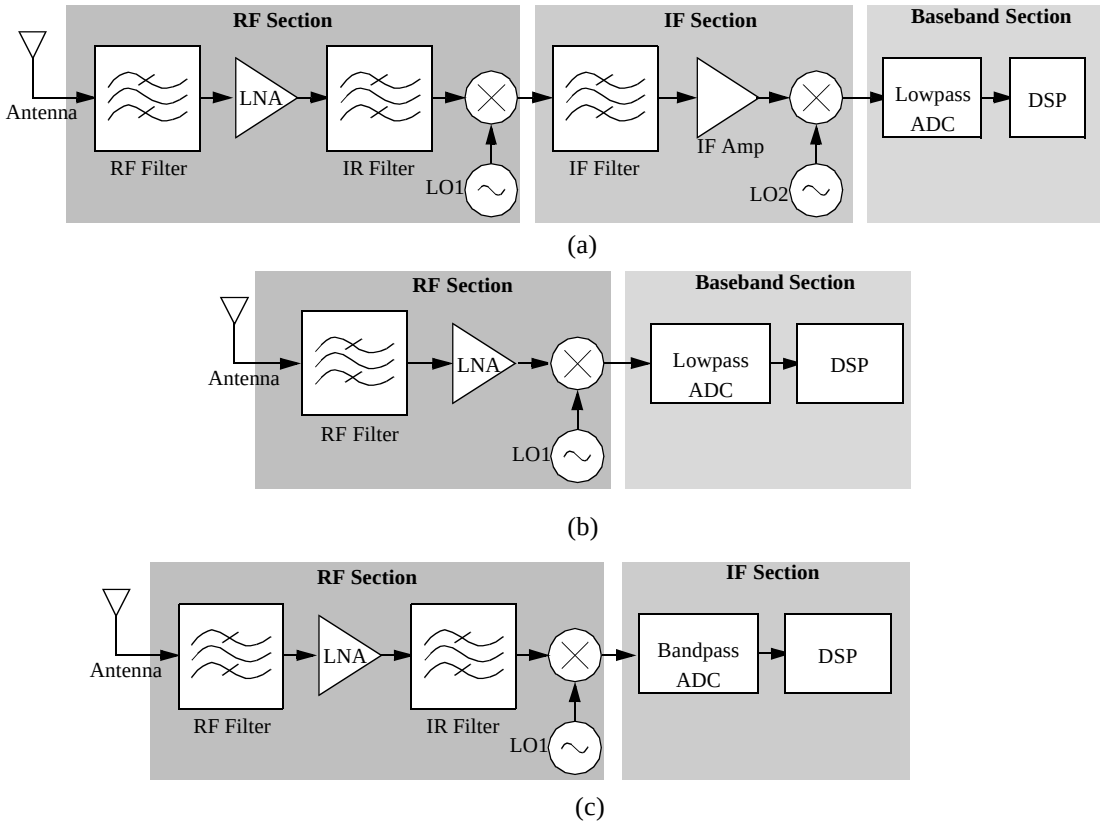



**Figure 12.2:** Digital RF receivers. (a) Superheterodyne. (b) Direct conversion. (c) IF conversion.

techniques such as $g_m - C$ or Switched-Capacitor (SC). However, the use of a low IF imposes very demanding requirements for the Image-Reject (IR) filter[†1].

In order to *relax* the IR filter requirements, an analog quadrature mixer can be used in both the RF and the IF sections [9]. As an illustration, Fig. 12.3(a) shows the IF section of a superheterodyne receiver including a quadrature mixer. Note

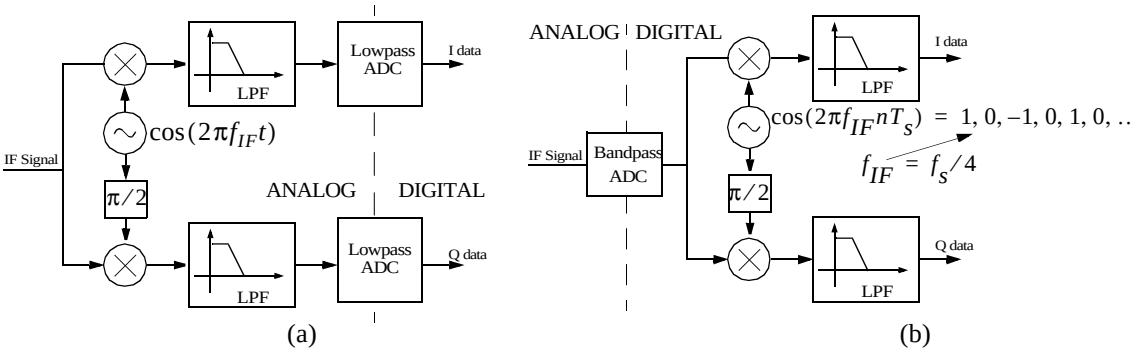



**Figure 12.3:** Using quadrature mixers in: (a) Superheterodyne receivers. (b) IF-conversion receivers.

1 . The problem of suppressing signals in the image band will be discussed later.

that two lowpass ADCs are needed to digitize the resulting In-phase (I) and Quadrature (Q) components. These quadrature signals are complex combined in order to cancel the image power in the downconverted signal band. In practice, however, there is not a complete cancellation of the image due to gain and phase mismatch between quadrature paths in Fig. 12.3(a).

For that reason, other alternatives have been explored in last years to improve the IR problem in *low-IF superheterodyne receivers*. One of them is based on the integration of an IF quadrature mixer with a lowpass ΣΔM, usually referred to as IF-to-Baseband ΣΔMs [10][11]. In these architectures, the mixer errors are shaped so that they are reduced in the desired band. In practical circuit realizations, the IR feature is limited by I/Q path mismatches, which requires the use of additional compensation strategies like dynamic element matching algorithms [10].

The IR problem can be completely eliminated by using the receiver shown in Fig. 12.2(b), known as *direct conversion, zero-IF* or *homodyne* receiver. In this architecture, the RF signal is mixed-down directly to DC where is digitized. This approach is more suited to integration than the *superheterodyne* because it eliminates the IF section. Hence, only off-chip RF filters are required since, as the image and the desired signal are the same, the IR filter can be removed. However, the offset and flicker noise of the mixer are present in the middle of the signal band and can severely degrade the performance of this type of receivers.

Many of the problems arising in the above mentioned receiver architectures can be eliminated using the *IF-conversion receiver*, shown in Fig. 12.2(c). In this architecture the in-coming signal at the antenna is first mixed-down to IF where it is digitized. Thus, the signal is first translated to the digital domain by one ADC, referred to as *bandpass* or *IF ADC*, and then mixed to the baseband as shown in Fig. 12.3(b). This is advantageous for several reasons. On the one hand, as quadrature mixing is done in the digital domain, the problems associated with the analog mixer in the receiver shown in Fig. 12.3(a) are avoided [12]. Another advantage of the *IF-conversion receiver* is that it allows channel-select filtering, gain control and demodulation to be handled in the digital domain [13][14]. This results in robust RF receivers with a high degree of programmability, thus allowing a single software-controlled RF receiver to be employed for multi-standard receivers [15].

### 11.2.3 IF A/D Conversion - Bandpass ΣΔ modulators

Digitization in IF-conversion receivers can be accomplished either with a wideband Nyquist-rate ADC or a BPΣΔ-ADC. The use of the latter is the optimum solution since the bandwidth of IF signals is typically much smaller than the carrier frequency, and hence, reducing the quantization noise in the entire Nyquist

band becomes superfluous. Instead, by using BPΣΔ-ADCs the quantization noise power is reduced only in a narrowband around the IF location, thus taking advantage of the higher *oversampling ratio*[†2] and hence yielding to a high resolution.

BandPass ΣΔ Modulators (BPΣΔMs) extend the noise-shaping concept from the *conventional* LowPass ΣΔMs (LPΣΔMs) – in which the quantization noise is suppressed around DC – to a more general case where the quantization noise is reduced in a narrow passband centred at an IF location [5][17]. Thus, the design and analysis of BPΣΔMs share much in common with LPΣΔMs [12].

The rest of the chapter is devoted to the study of BPΣΔ-ADCs, surveying the different design issues, from architectures to circuit implementation.

## 11.3 BASIC CONCEPTS OF BANDPASS ΣΔ A/D CONVERTERS

A BPΣΔ ADC[†3] is a particular class of ΣΔ–ADC that places the zeroes of the quantization noise transfer function in a narrow band around an IF location, usually named *notch* frequency, and represented by the parameter $f_n$.

Fig. 12.4 shows the conceptual block diagram of a BPΣΔM. It is composed of a BandPass Filter (BPF), an $N$-bit quantizer and a Digital-to-Analog Converter (DAC) connected in a loop. The BPF can be synthesized by cascading two or more second-order biquadratic filters or *resonators*, which must have a sharp transfer function and well-defined resonance at $f_n$. These resonators may be implemented as a Discrete-Time (DT) filter using either SC [13][14] or *SwItched-current* (SI) [18] techniques or they may be implemented as a Continuous-Time (CT) filter [19][20].

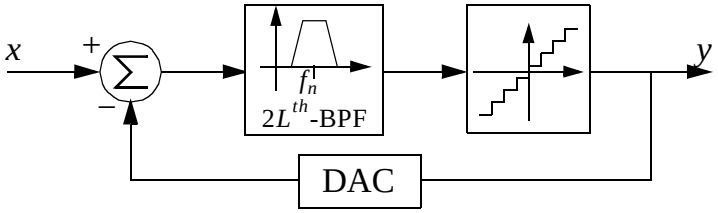



**Figure 12.4:** Conceptual block diagram of a BPΣΔM.

2. In the case of bandpass signals, the oversampling ratio is defined as [16] $M = f_S\lfloor (f_n + B_w/2)/B_w \rfloor / [2(f_n + B_w/2)]$, where $B_w$ is the signal bandwidth, $f_S$ is the sampling frequency, $f_n$ is the centre frequency and $\lfloor x \rfloor$ stands for the largest integer not exceeding $x$.
3. A BPΣΔ ADC is composed of three basic blocks: an anti-aliasing filtering, a BPΣΔM and a digital decimator. As in the lowpass case, the modulator is the hardest to design since oversampling simplifies the anti-aliasing filter requirements and the decimator is a pure digital block whose design can be highly structured and automated [12]. For that reason, we will focus on the modulator design issues.

Let us consider that the BPF is a $2L^{th}$-order filter composed of a cascade of $L$ resonators with a DT[†4] transfer function given by:

$$H_R(z) = \frac{N_R(z)}{(1-z^{-1}z_n)(1-z^{-1}z_n^*)} \tag{12.1}$$

where $z_n$ and $z_n^*$ are the conjugate-complex poles of $H_R(z)$. Assuming that the quantization error can be modelled as an additive, white noise source, the $z$-transform of the modulator output in Fig. 12.4 can be written as:

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E_q(z) \tag{12.2}$$

where the signal transfer function and the noise transfer function are respectively:

$$S_{TF}(z) = \frac{[N_R(z)]^L}{[N_R(z) + (1-z^{-1}z_n)(1-z^{-1}z_n^*)]^L} \tag{12.3}$$

$$N_{TF}(z) = \frac{[(1-z^{-1}z_n)(1-z^{-1}z_n^*)]^L}{[N_R(z) + (1-z^{-1}z_n)(1-z^{-1}z_n^*)]^L} \tag{12.4}$$

Note that $N_{TF}(z)$ has $L$ zeroes at $z = z_n$ and $z = z_n^*$. In most practical cases, $z_n$ and $z_n^*$ are placed in the unit circle, i.e, $z_n = \exp[j(2\pi f_n T_S)]$, with $T_S$ being the sampling period. In some BPΣΔMs the value of $f_n$ can be either digitally [21] or continuously [22] programmable, thus allowing $f_n$ to be changed without changing $f_S$. This is especially useful in radio applications, where the use of a tunable BPΣΔM eliminates the necessity of a channel-selection function in RF receivers.

Assuming that $N_R(z)$ is synthesized in such a way that

$$N_R(z) + (1-z^{-1}z_n)(1-z^{-1}z_n^*) = 1 \tag{12.5}$$

yields:

4. A similar discussion can be held for CT-BPΣΔMs. This class of modulators are internally DT systems as will be discussed in Section 11.4.5.

$$N_{TF}(z) = [1 - 2\cos(2\pi f_n T_S)z^{-1} + z^{-2}]^L \tag{12.6}$$

and the Power Spectral Density (PSD) of the *shaped* quantization noise is:

$$S_Q(f) = \frac{\Delta^2}{12 f_S}\left|N_{TF}(f)\right|^2 = \frac{\Delta^2}{12 f_S}\left|4\sin[\pi(f - f_n)T_S]\sin[\pi(f + f_n)T_S]\right|^{2L} \tag{12.7}$$

where $\Delta$ is the quantization step, defined as $\Delta \equiv X_{FS}/(2^N - 1)$, with $X_{FS}$ being the full-scale range of the quantizer.

The quantization noise in-band power can be calculated as follows:

$$P_Q = \int_{f_n - B_w/2}^{f_n + B_w/2} 2S_Q(f)df \cong \frac{(\sin[2\pi f_n T_S])^{2L}\pi^{2L}X_{FS}^2}{12(2^N - 1)^2(2L + 1)M^{(2L+1)}} \tag{12.8}$$

where $B_w$ is the signal bandwidth and $B_w \ll f_n$ has been assumed. An important conclusion is that, although the BPΣΔM of Fig. 12.4 is a $2L^{th}$-order modulator, the quantization noise is suppressed with $L^{th}$-order bandstop filtering. In other words, the quantization noise shaping of a $2L^{th}$-order BPΣΔM is equal to that of an $L^{th}$-order LPΣΔM. As an illustration, Fig. 12.5(a) plots several simulated output spectra of the modulator in Fig. 12.4 for $N = 1$, $f_n = f_S/4$ and different values of $L$. The input is a sinusoidal signal of a frequency close to $f_n$ and an amplitude $A = A_{REF}/2$, with $A_{REF}$ being the output level of the DAC. As Fig. 12.5(a) shows, the output spectrum of the modulator can be seen as the sum of two components: the input signal spectrum (a vertical line) and the quantization noise spectrum. The form of the shaped quantization noise is like a valley with its

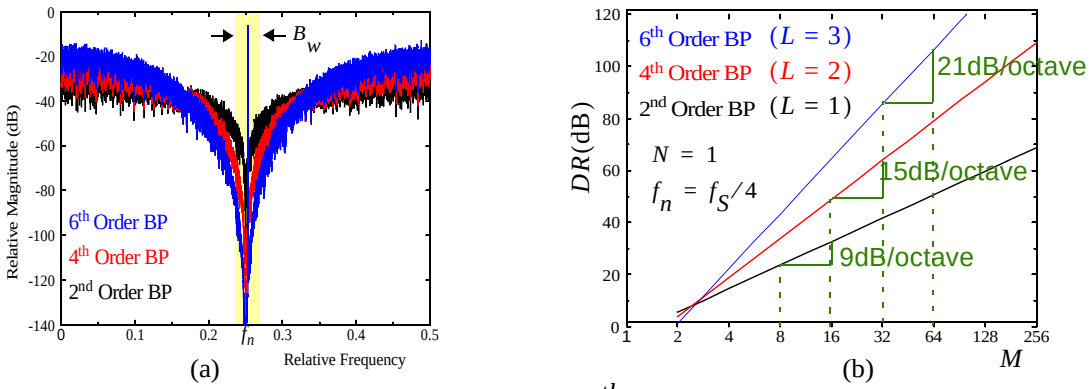



**Figure 12.5:** (a) Ideal output spectra of a $2L^{th}$-order BPΣΔM. (b) $DR$ vs. $M$.

minimum value at $f_n$.

The Signal-to-Noise Ratio ($SNR$) and the Dynamic Range ($DR$) for the modulator of Fig. 12.4, are given respectively by:

$$SNR \equiv \frac{A^2/2}{P_Q} = \frac{3(2^N-1)^2(2L+1)M^{2L+1}}{2\pi^{2L}(\sin[2\pi f_n T_s])^{2L}}\left(\frac{2A}{X_{FS}}\right)^2 \tag{12.9}$$

$$DR \equiv \frac{(X_{FS}/2)^2}{2P_Q} = \frac{3(2^N-1)^2(2L+1)M^{2L+1}}{2\pi^{2L}(\sin[2\pi f_n T_s])^{2L}} \tag{12.10}$$

Note that for a $2L^{th}$-order BPΣΔM, the quantization noise increases at a rate of $[(2L+1)\log(2)]\text{dB/octave}$, which is equivalent to a $L^{th}$-order LPΣΔM. This is shown in Fig. 12.5(b) by plotting $DR$ vs. $M$, computed from the spectra in Fig. 12.5(a).

### 11.3.1 Signal passband location

In theory, the passband of a BPΣΔM can be placed at any frequency from DC to $f_S/2$. Thus, for a given input signal centre frequency, $f_{IF}$ (the IF location in a wireless receiver) and bandwidth, $B_w$, the choice of the ratio $f_n/f_S$ is a trade-off among sampling frequency (directly related to the speed of the whole system), anti-aliasing filter requirements, and oversampling ratio. As illustrated in Fig. 12.6(a), the transition band, $B_{tr}$, of the anti-aliasing filter becomes sharper as $f_n$ approaches $f_S/2$. Thus, the lower $f_n(=f_{IF})$ the higher $B_{tr_{max}}$. However, the use of low $f_{IF}$ complicates the problem of suppressing image-band signals when the RF signal is mixed down to an IF location. This is illustrated in Fig. 12.6(b), where the incoming RF signal is centered at $f_{RF}$. Note that, an IR filtering must be performed preceding the mixer to avoid image-band signals centered at $f_{RF}-2f_{IF}$ to corrupt the desired signal [1][8].

In order to cope with both IR and anti-aliasing filter requirements, $f_n$ must be located at an intermediate location in the Nyquist band. An optimum solution to this problem is to place $f_n$ at one-quarter of the sampling frequency. This notch frequency location, in addition to relaxing the mentioned filter specifications, offers several advantages. First, the forward path loop (analog) filter realization

can be relatively simplified. Secondly, it makes simpler the synthesis of bandpass architectures, which can be easily derived from lowpass prototypes with a simple variable transformation (for instance $z^{-1} \rightarrow -z^{-2}$) as will be described in the next section. Last but not least, the design of the digital mixing to baseband (see Fig. 12.3(b)) is obviously simplified because the digital cosine and sine signals are equal to the data series $(1, 0, -1, 0, \ldots)$ and $(0, 1, 0, -1, \ldots)$, respectively.

In addition to the mentioned advantages, making $f_n = f_S/4$ also offers the possibility of centering the IF signal at $3f_S/4$ as demonstrated in [23] – the spectrum is symmetrical with respect to $f_S/2$. This approach offers several advantages. On the one hand, making $f_{IF} = 3f_S/4$ the anti-aliasing filter requirements are the same as for $f_{IF} = f_S/4$, but the IR filter specifications are relaxed. On the other hand, it allows for either the clock rate to be reduced to one-third or processing signals to be three times higher in frequency. The only drawback is that the oversampling ratio is also reduced by a factor of three. For example, in the case of a $4^{th}$-order BPΣΔM, this means a $DR$ loss of $3.7\text{bit}$.

## 11.3.2 Decimation for bandpass ΣΔ ADCs

The decimator filter is the last stage of a ΣΔ ADC. This block realizes two operations on the modulator output bit stream: filtering the out-of-band quantization noise and reducing the sampling rate to the Nyquist rate [12].

Fig. 12.7 illustrates the decimation process in BPΣΔ-ADCs. The modulator

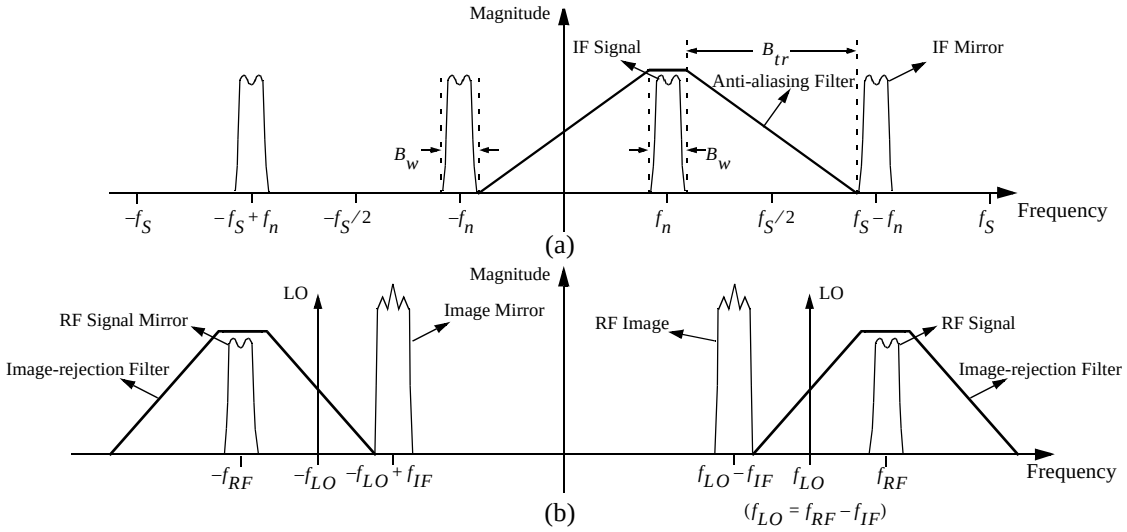



**Figure 12.6:** Choice of the signal passband location. (a) Trade-off among anti-aliasing filter requirements and high values of $f_{IF}$. (b) Trade-off among IR filter requirements and low values of $f_{IF}$.

output, $y$, is first filtered by a bandpass filter with a digital cut-off frequency at $B_w = f_S/(2M)$. This filter removes all out-of-band components in order to avoid aliasing in the subsequent *compressor* stage. Thus, the band-limited signal resulting from the filtering, $w$, is *downsampled* by discarding $M-1$ out of every $M$ samples to produce the decimated signal, $y_d$, at the Nyquist rate.

Note that the scheme of Fig. 12.7 requires a high-Q narrow-band BPF with a high passband center frequency. This yields an increase of cost, in terms of power consumption and silicon area, as compared to the lowpass case. This problem can be avoided by using the scheme shown in Fig. 12.8, composed of a complex mixer and a complex lowpass filter [24]. The modulator output is mixed down to baseband through the multiplication of $\exp(-j2\pi f_n n T_S)$. This scheme can be notably simplified if $f_n = f_S/4$ because the multiplying signal is a sum of two periodic data series containing 0's and ±1's as illustrated in Fig. 12.8.

Note that, as the inputs to the lowpass filters are zeros in alternate clock cycles, the two lowpass filters can be simplified by only one multiplexed in time.

## 11.4 SYNTHESIS OF BANDPASS ΣΔ MODULATOR ARCHITECTURES

The basic structure of a BPΣΔM is analogous to that of an LPΣΔM except for the type of loop filter. Thus, the operation of both types of ΣΔMs is based on the same strategy to attenuate the quantization noise. Hence, although most of the design art developed for LPΣΔMs can be used to develop BPΣΔMs, there are some aspects of the modulator design which are peculiar to BPΣΔMs. This fact has motivated the development of several methods for synthesizing BPΣΔM architectures. This section summarizes the most important of these methods.

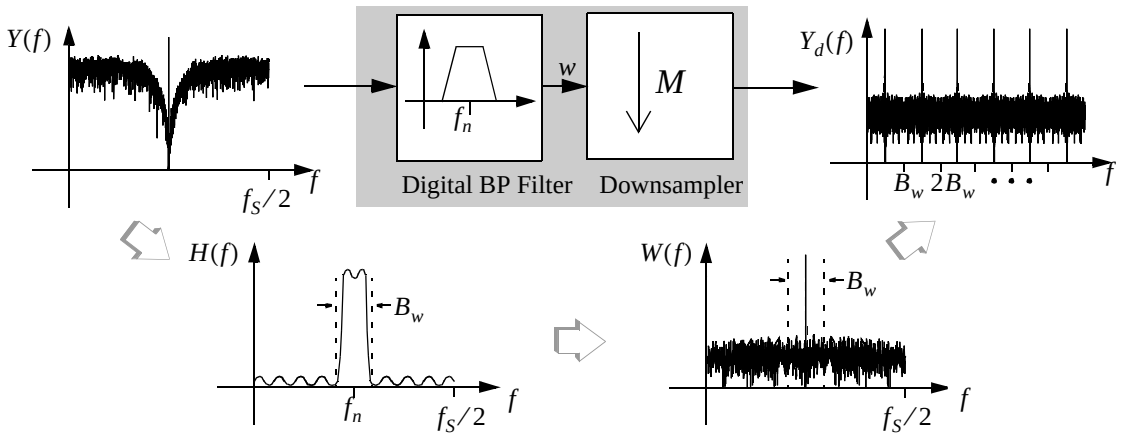



**Figure 12.7:** Decimation process in BPΣΔ-ADCs.

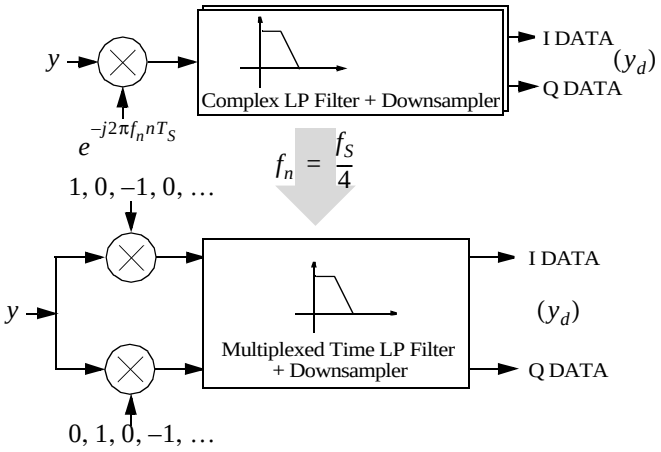



**Figure 12.8:** Efficient decimator for BPΣΔMs.

### 11.4.1 The lowpass-to-bandpass transformation method: LP-to-BP

As shown in Section 11.3, an $L^{th}$-order LPΣΔM and a $2L^{th}$-order BPΣΔM, present identical figures of merit: $SNR$ and $DR$. Consequently, a simple way to synthesize any BPΣΔM architecture is to apply a Lowpass-to-Bandpass (LP-to-BP) transformation to an LPΣΔM that meets a given specification. The LP-to-BP transformation most extensively used in BPΣΔM Integrated Circuits (ICs) is:

$$z^{-1} \rightarrow -z^{-2} \tag{12.11}$$

Applying the above transformation to the $L^{th}$-order LPΣΔM of Fig. 12.9(b), the $2L^{th}$-order BPΣΔM of the Fig. 12.9(a) is obtained. Assuming a linear model

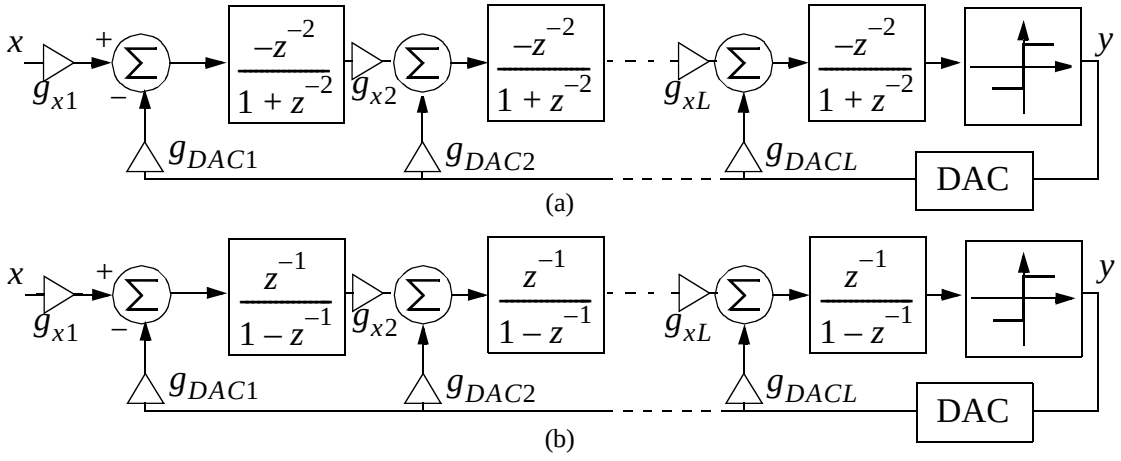



**Figure 12.9:** (a) Block diagram of the $2L^{th}$-order BPΣΔM derived by applying $z^{-1} \rightarrow -z^{-2}$ to the $L^{th}$-order LPΣΔM shown in (b).

for the quantizer, the $Z$-transform of the BPΣΔM output is given by:

$$Y(z) = (-z^{-2})^{L} X(z) + (1 + z^{-2})^{L} E_q(z) \tag{12.12}$$

As illustrated in Fig. 12.10, the zeroes of the $N_{TF}$ are mapped from DC (in the original LPΣΔM) to $f_S/4$ (in the resulting BPΣΔM), which corresponds to $z_n = \exp[j(\pi/2)]$ in Fig. 12.10.

Note that, as a consequence of the transformation in eq.(12.11), the integrators of the original LPΣΔM become resonators in the resulting BPΣΔM, which have the transfer function in eq.(12.1) with $z_n = \exp[j(\pi/2)]$ and $N_R(z) = -z^{-2}$.

The shaped quantization noise power, $P_Q$, of the modulator in Fig. 12.9, can be obtained by substituting $f_n = f_S/4$ in eq.(12.8), yielding to an identical expression to that of an $L^{th}$-order LPΣΔM. In an analogous way, the $SNR$ and the $DR$ are identical to that obtained in a $L^{th}$-order LPΣΔM [25].

In general, any $2L^{th}$-order, $N$-bit BPΣΔM can be obtained by applying the transformation in eq.(12.11) to an $L^{th}$-order, $N$-bit LPΣΔM. As an illustration, Fig. 12.11 shows several BPΣΔMs obtained by using that transformation. Fig. 12.11(a) is a $2^{nd}$-order BPΣΔM, Fig. 12.11(b) is a $4^{th}$-order, and Fig. 12.11(c) is a $8^{th}$-order 4-4 cascade obtained from a $1^{st}$-order LPΣΔM, a $2^{nd}$-order LPΣΔM and a $4^{th}$-order 2-2 cascade LPΣΔM, respectively.

The transformation in eq.(12.11) preserves all features of the original modulator: $P_Q$, $SNR$, $DR$, etc.... In addition to these characteristics, eq.(12.11) keeps the stability properties of the original LPΣΔMs. In fact, the resulting BPΣΔM will be

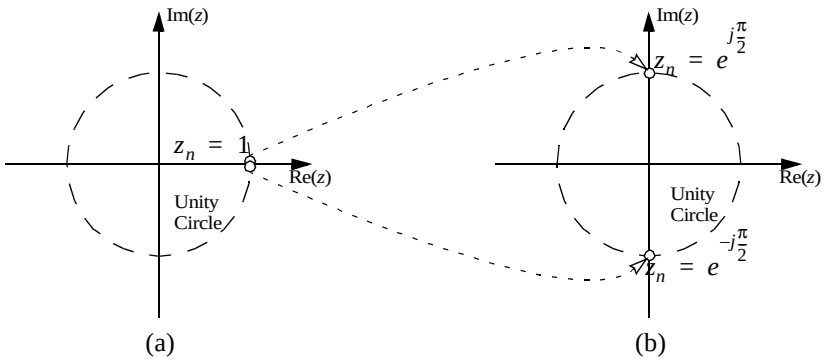



**Figure 12.10:** Zero location of $N_{TF}$ for: (a) LPΣΔM. (b) BPΣΔM.

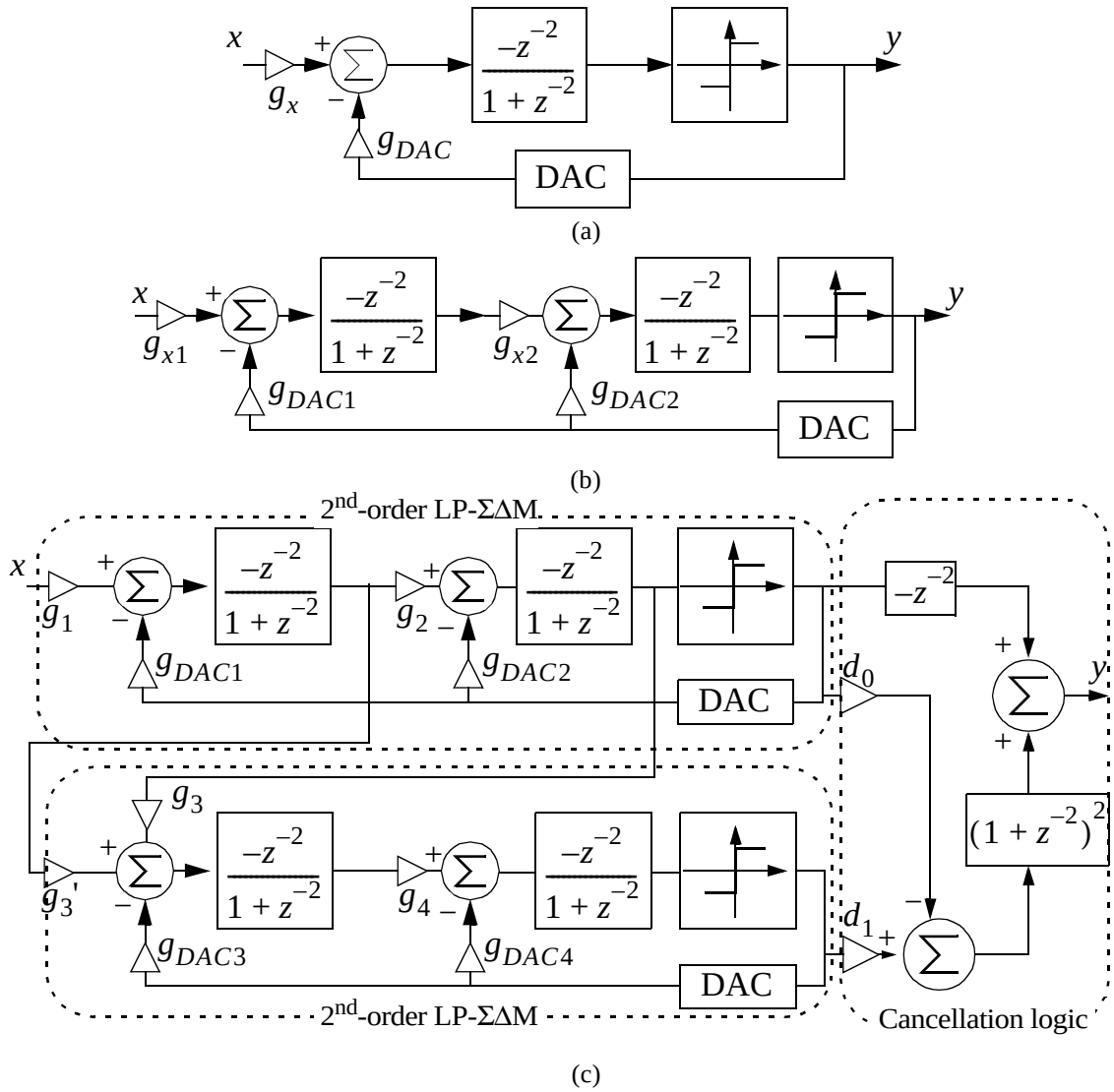



**Figure 12.11:** BPΣΔMs obtained by using $z^{-1} \rightarrow -z^{-2}$. a) $2^{th}$-order BPΣΔM. b) $4^{th}$-order BPΣΔM. c) 8th-order 4-4.

stable if and only if the original LPΣΔM is stable. As for the lowpass case, the use of cascade BPΣΔMs guarantees the stability for high-order modulators ($L > 2$).

### 11.4.1.1 *Pattern noise of second-order BPSDMs*

An important property that is translated from LPΣΔMs to BPΣΔMs is the non-linear behaviour of the quantization error. This phenomenon is much more significant as the number of internal levels of the quantizer and/or the order of the ΣΔM decreases, the worst case corresponding to a 1-bit $1^{st}$-order LPΣΔM [26]. In the

bandpass case, a 1-bit $2^{nd}$-order BPΣΔM presents a *noise pattern* similar to that of its lowpass counterpart. To demonstrate this, the modulator of Fig. 12.11(a) is simulated for a single-tone input signal with a frequency equal to $f_S/4$. The signal amplitude was varied in the range $[-\Delta/2, \Delta/2]$. Fig. 12.12 (a) shows the quantization error in-band power as a function of the input signal amplitude for $M = 64$, showing a behaviour similar to that shown in $1^{st}$-order LPΣΔMs with DC signals [26], reproduced in Fig. 12.12(b).

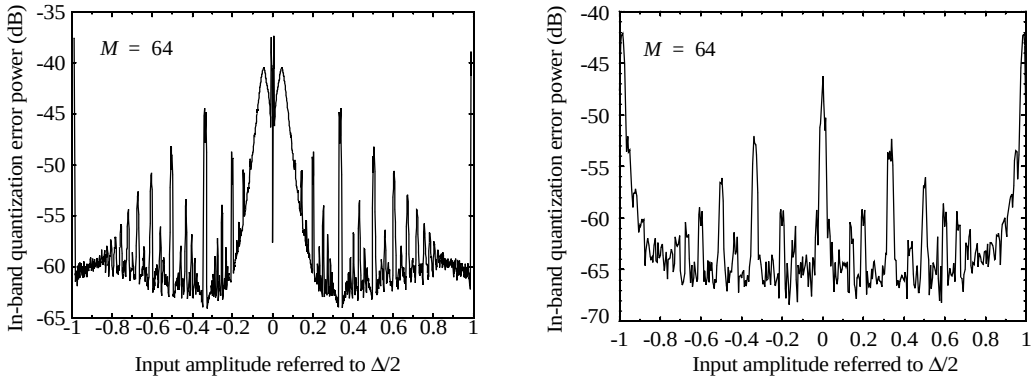



**Figure 12.12:** Pattern noise of a: (a) $2^{nd}$-order BPΣΔM. (b) $1^{st}$-order LPΣΔM.

11.4.1.2*Other LP-to-BP transformations*

The transformation in eq.(12.11) places the zeroes of $N_{TF}(z)$ at $f_n = f_S/4$. This relaxes the IR and anti-aliasing filtering requirements as shown in Section 11.3.1. However, centering the signal passband at $f_S/4$ offers some disadvantages. On the one hand, in the presence of non-linear errors in the analog circuitry of the modulator, any inter-modulation distortion products resulting from the mixing of tones located at $f_S/2$ with input signal will fall inside the passband, thus corrupting the signal information. This will be treated in more detail in the following sections. On the other hand, for a given input IF, the demands for the sampling rate of the modulator are more restrictive than placing the signal passband center frequency between $f_S/4$ and $f_S/2$ [23].

Because the above-mentioned reason, some authors propose to generalize the LP-to-BP transformation in order to locate the zeroes of $N_{TF}$ at any arbitrary frequency, $f_n = f_S/(2p)$ [27]. However, this approach, generally yielding to complex unpractical architectures, has been varely used in the reported BPΣΔM ICs.

### 11.4.2 Optimized synthesis of $N_{TF}(z)$

A more flexible approach for designing BPΣΔMs consists on directly synthesizing the modulator loop filter. This allows us to place the poles and zeroes of both $S_{TF}(z)$ and $N_{TF}(z)$ optimally in order to fulfil a given specification [13]. From this perspective, the design of BPΣΔMs is essentially reduced to a problem of filter optimization.

The resulting architectures are usually of the *interpolative* type like that in the lowpass case [12]. This type of architecture offers the possibility of designing $S_{TF}(z)$ in such a way that it performs an anti-aliasing filter. However, as occurs with other interpolative structures, complicated analog circuitry is required, thus being more sensitive to the precision of the components.

For illustration purposes, Fig. 12.13(a) shows a $4^{th}$-order BPΣΔM, composed of a cascade of resonators, designed using this method [13]. Fig. 12.13(b) shows the pole/zero location of $S_{TF}(z)$ and $N_{TF}(z)$. Observe that the zeroes of $N_{TF}(z)$ are placed around $f_S/4$. In this case $S_{TF}(z)$ realizes a bandpass function which acts as an anti-aliasing filter (see Fig. 12.13(c)).

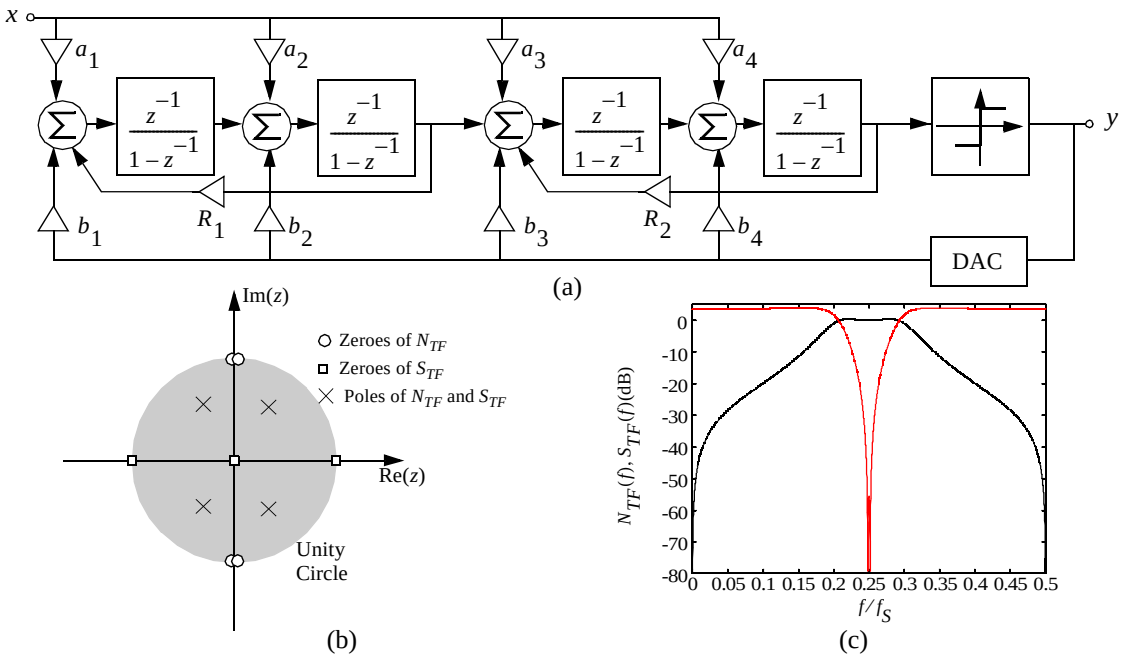



**Figure 12.13:** An example of a $4^{th}$ – order BPΣΔM obtained using the directly $N_{TF}(z)$ method [13]. (a) Modulator architecture. (b) Pole/zero location of $S_{TF}(z)$ and $N_{TF}(z)$. (c) $S_{TF}(f)$ and $N_{TF}(f)$ vs. frequency.

### 11.4.3 Quadrature bandpass ΣΔ modulators

As stated in Section 11.2, the IR problem arising in digital superheterodyne receivers can be overcome by using quadrature mixers in both the RF and the IF sections. An obvious consequence of using quadrature mixing in the RF section is that the IF signal is separated into two components: I and Q. Hence, two BPΣΔMs are required as illustrated in Fig. 12.14(a), which means doubling the required hardware – two BPΣΔMs compared to only one BPΣΔM if a simple mixer is used. This fact motivates finding new strategies that solve the problem of digitizing the I/Q components of the IF signal.

Fig. 12.14(b) shows an radio architecture that uses a complex, or quadrature, version of a BPΣΔM, called *quadrature* BPΣΔM [28]. This type of BPΣΔMs uses only one ADC to perform directly the A/D conversion of both I and Q signals.

Fig. 12.15 shows a conceptual block diagram of a quadrature BPΣΔM. The main difference with respect to conventional BPΣΔMs is the complex BPF embedded in the loop. Thus, the modulator output consists of a pair of bit streams,

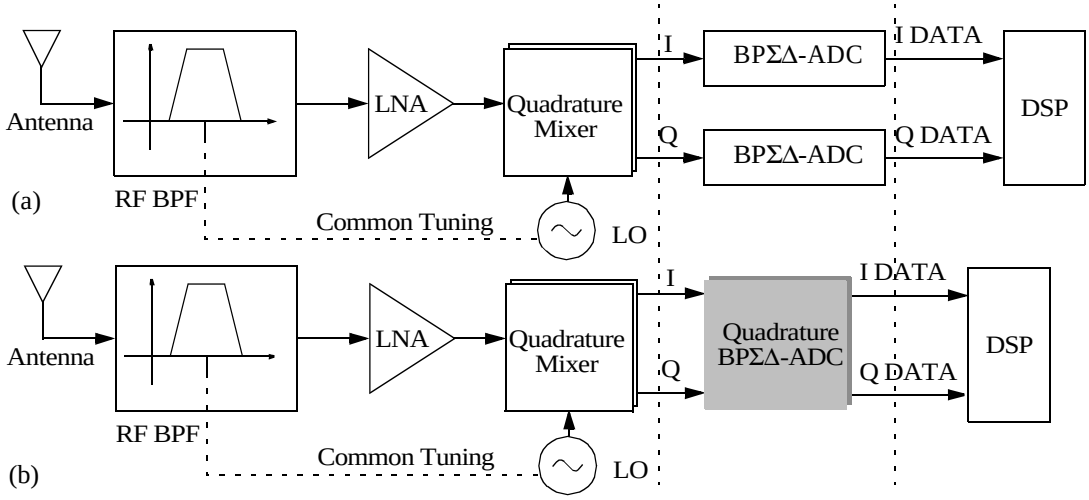



**Figure 12.14:** RF radio receivers using: (a) Conventional BPΣΔMs. (b) Quadrature BPΣΔMs.

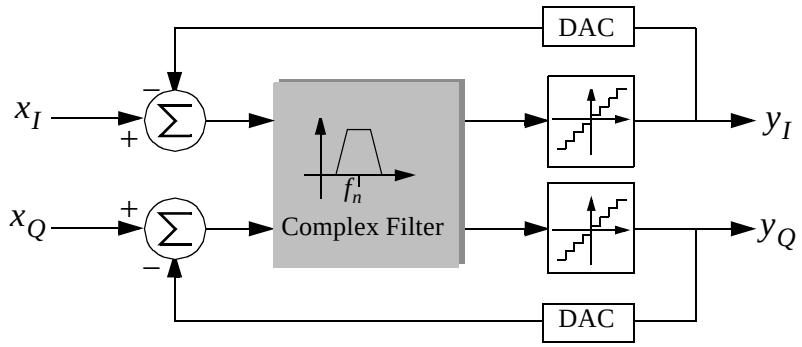



**Figure 12.15:** Conceptual block diagram of a quadrature BPΣΔM.

one of them representing the real output and the other one the imaginary output. When combined, these two outputs form a complex digital signal which represents the complex (I/Q) input signal and the shaped quantization noise.

The complex BPF in a quadrature BPΣΔM can be realized either using DT or CT circuitry. In practice, this filter is constructed from several cross-coupled real filters as illustrated in Fig. 12.16(a). The complex output signal is:

$$X_o(z) = H(z)X_i(z) = X_{o_{Re}}(z) + jX_{o_{Im}} \tag{12.13}$$

where

$$\begin{aligned} X_{o_{Re}} &= H_{Re}(z)X_{i_{Re}} - H_{Im}(z)X_{i_{Im}}(z) \\ X_{o_{Im}} &= H_{Re}(z)X_{i_{Im}} + H_{Im}(z)X_{i_{Re}}(z) \end{aligned} \tag{12.14}$$

Observe that there is an analogy between complex filters and fully differential filters in the sense of that both architectures double the number of elements required to implement a given circuit. As an illustration, Fig. 12.16(b) shows a realization of a complex 1st-order filter with a single pole at $z_p = a + jb$ [28].

The $N_{TF}$ performed by quadrature BPΣΔMs has complex value coefficients and hence, it is not constrained to performing complex-conjugate zeroes or to having a symmetric response respect to DC. This allows an $L^{th}$-order BPΣΔM to place $L$ zeroes at $f_n$ without having any zero at $-f_n$. Therefore, the zeroes of $N_{TF}$ may be a rotated version of those of an $L^{th}$-order LPΣΔM. To illustrate this, let us consider a complex $4^{th}$-order BPΣΔM with $N_{TF} = (1 - jz^{-1})^4$. This function, displayed in Fig. 12.17, presents four zeroes at $f_n = f_S/4$.

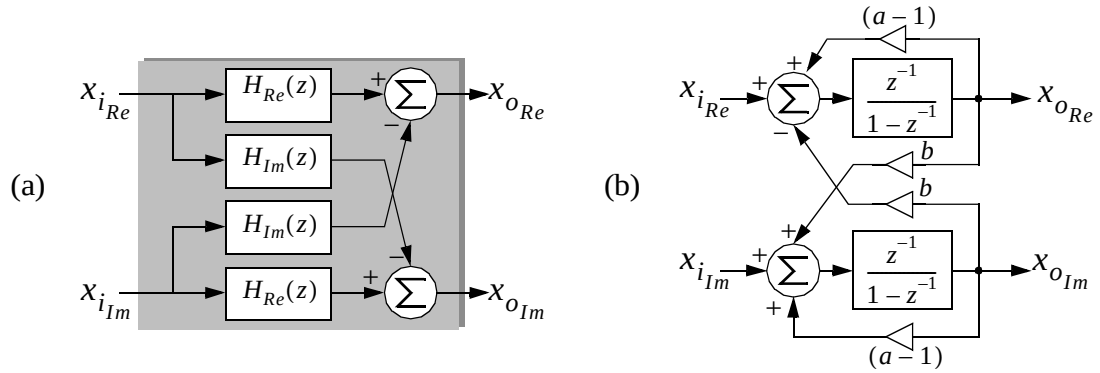



**Figure 12.16:** Realization of complex filters. (a) Conceptual block diagram. (b) Complex filter with a single pole.

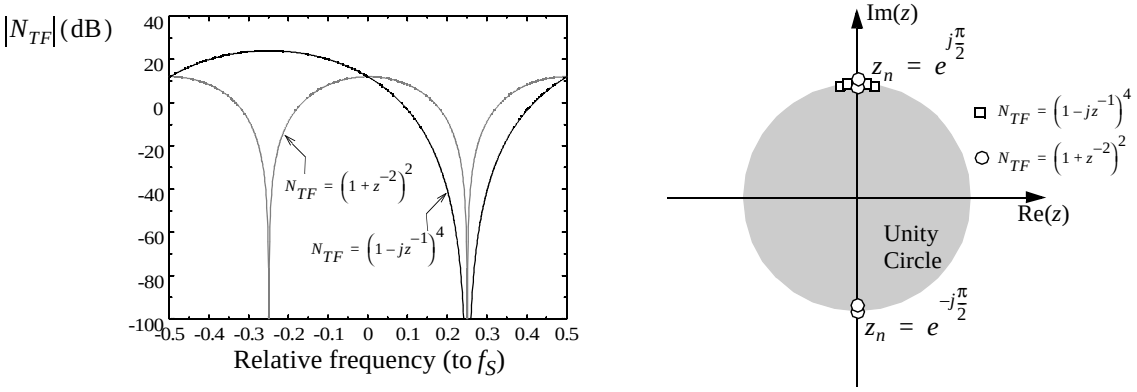



**Figure 12.17:** $N_{TF}$ and noise zero location for a quadrature $4^{th}$-order BPΣΔM.

An important practical limitation of quadrature BPΣΔMs is due to mismatching between real and imaginary channels. As a consequence, signal image components will appear in the signal band, thus corrupting the information. To reduce this effect, quadrature BPΣΔMs must be designed to place some of the $N_{TF}$ zeroes at the image band [28]. However, this reduces the order of the quantization noise filtering performed by the quadrature modulator – one of its main advantages with respect to conventional BPΣΔMs.

### 11.4.4 *N*-path bandpass ΣΔ modulators

Centering the notch frequency at $f_S/4$ has multiple advantages as already mentioned. However, in practical applications, the *DR* of BPΣΔMs becomes increasingly constrained by circuit non-idealities at high sampling rates – needed to digitize signals at IF locations. To overcome this problem, some authors propose the use of *N*-path filters to implement the resonator transfer function [15].

Using the *N-path* design technique, [29], the resonator transfer function can be separated into two high-pass filter, sampled at $f_S/2$, such that:

$$H(z) = \frac{z^{-2}}{1+z^{-2}} = \left.\frac{z_p^{-1}}{1+z_p^{-1}}\right|_{z_p = z^2} \tag{12.15}$$

As an illustration, Fig. 12.18 shows a 2-*path* $4^{th}$-order BPΣΔM [30]. The original architecture is partitioned into two interleaved paths, with the resonators replaced by two high-pass filters as in eq.(12.15).

The main problem of *N*-path architectures is due to the gain and phase mismatches between the different paths. This manifests itself as mirror image signals

which appear in the signal bandwidth and corrupt the information [30].

### 11.4.5 Synthesis of continuous-time bandpass ΣΔ modulators

The architectures described in earlier sections assumed that the loop filter is of the DT type. In recent years, the increased demand for high-speed BPΣΔMs has motivated the development of BPΣΔMs based on CT loop filters, generically known as Continuous-Time BPΣΔMs (CT-BPΣΔMs) [19][20]. This approach offers several advantages. On the one hand, CT filters are much faster than their DT counterparts. On the other hand, it can be shown that CT-BPΣΔMs provide an implicit anti-aliasing filter for out-of-band signals at no cost [22]. However, CT-BPΣΔMs are more sensitive to *clock jitter* than DT-BPΣΔMs. This is because the internal clock that controls the comparison instant, also controls the rising and falling edges of the DAC output. Hence, clock jitter errors are directly added to the input signal [31]. Another important limitation of CT-BPΣΔMs is the *excess loop delay* contributed by each building block in the modulator loop, which can severely degrade the quantization noise transfer function [32].[†5]

Fig. 12.19(a) is a conceptual block diagram of a CT-BPΣΔM. This modulator is

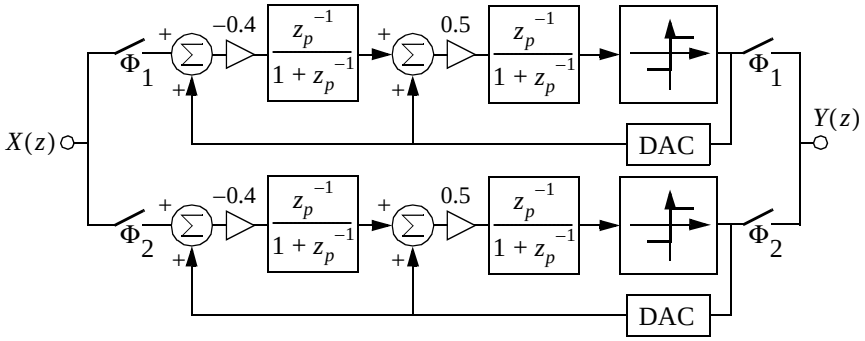



**Figure 12.18:** Conceptual diagram of a 2-path 4th-order BPΣΔM [30].

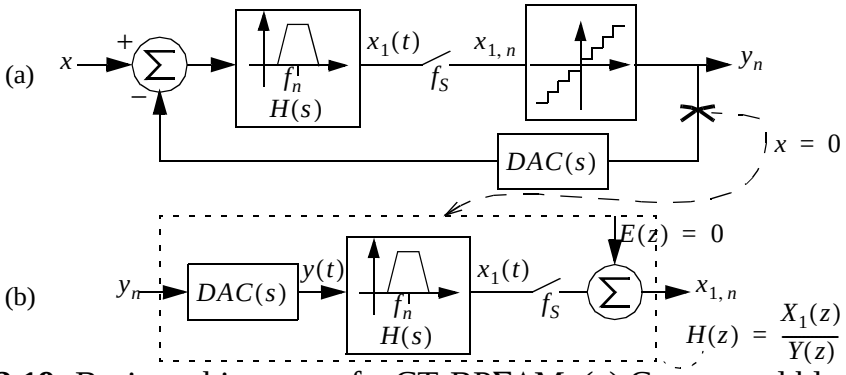



**Figure 12.19:** Basic architecture of a CT-BPΣΔM. (a) Conceptual block diagram. (b) Open loop block diagram.

5 . Section 11.5 will treat these limitations in more detail.

internally a DT circuit since there is an Sampling-and-Hold (S/H) circuit inside the loop, just at the quantizer input. This fact makes the overall loop from the output of the quantizer back to its input have a $Z$-domain transfer function as illustrated in Fig. 12.19(b). The equivalent DT loop filter transfer function is [22]:

$$H(z) = Z\left[L^{-1}[DAC(s)H(s)]\Big|_{t=nT_s}\right] = Z\left[\int_{-\infty}^{\infty} DAC(\tau)h(t-\tau)d\tau\Big|_{t=nT_s}\right] \quad (12.16)$$

where $DAC(t)$ is the impulsive response of the DAC.

The expression in eq.(12.16), known as *pulse invariant transformation,* allows us to obtain an equivalent relation between DT- and CT-BPΣΔMs. Thus, the synthesis process of a CT-BPΣΔM starts from a DT loop filter that satisfies the required specifications and then it is transformed into an equivalent CT filter using eq.(12.16). Therefore, much of the knowledge available for DT-BPΣΔMs can be utilized for synthesizing CT-BPΣΔM architectures.

There are different ways of realizing the DT-to-CT transformation in eq.(12.16) depending on the shape of $DAC(t)$, namely: NonReturn-to-Zero (NRZ), Return-to-Zero (RZ) and Half-delay Return-to-Zero (HRZ). The differences among them will originate several architecture issues, specific of CT-BPΣΔMs. A detailed analysis of those issues – beyond the scope of this Chapter – can be found in several works related to this subject [20][22].

## 11.5 BUILDING BLOCKS AND ERROR MECHANISMS IN BPSDMS

The BPΣΔM architectures described in previous sections have been considered ideal except for the quantization error. In practice, the behaviour of such architectures deviates from the ideal performance as a consequence of their building block error mechanisms. This section discusses the impact of circuit parasitics on the performance of BPΣΔMs, showing their effects on the $N_{TF}$, the in-band noise power and the harmonic distortion.

The study presented here will focus on a single-loop $4^{th}$-order BPΣΔM (4th-BPΣΔM) – derived from applying the transformation in eq.(12.11) to a $2^{nd}$-order LPΣΔM. These modulators are easy to understand and simple to design, are capable of providing high resolution together with large tolerance to imperfections and robust stable operation [12]. Nevertheless, this study can be easily extended to other architectures such as multi-stage cascade architectures [33]. In these architectures, the error contributions due to the first stage – usually a single-loop BPΣΔM like that treated in this section – constitute the most significant degrading

factor of the overall modulator performance.

As a starting point for our study, the resonator – the main block of BPΣΔMs – is analyzed. Several architectures are described as well as their circuit implementation using different circuit techniques.

### 11.5.1 From integrators to resonators

As stated in Section 11.4.1, most of the reported BPΣΔM architectures have been obtained from corresponding lowpass prototypes by applying the transformation in eq.(12.11). As a consequence of this transformation, the integrators which form the loop filter in the original modulator become resonators with the following transfer function:

$$H_{res}(z) = \frac{\pm z^{-a}}{1 + z^{-2}} \qquad (0 < a \leq 2) \tag{12.17}$$

which has their poles located at $z_n = \exp(\pm 2\pi j)$, that is, $f_n = f_S/4$.

There are many filter structures which implement the transfer function in eq.(12.17). Fig. 12.20 shows three alternatives which has been used in BPΣΔMs. Fig. 12.20(a) is based on two delay elements connected in a loop, and is often called Delay-loop resonator [34]. Fig. 12.20(a)-(b) are based on Lossless Direct Integrators (LDIs) and Forward-Euler Integrators (FEIs), referred to as LDI-loop and FE-loop resonators, respectively [14]. Assuming that the scaling coefficients are $A_F = 1$ and $A_{FB,\,FB2} = -2$, the three resonators in Fig. 12.20 are identical. They have the transfer function in eq.(12.17) with $a = 2$ for Fig. 12.20(a) and (c), and $a = 1$ for Fig. 12.20(b).

In the presence of errors, the scaling coefficients $A_F$ and $A_{FB,\,FB2}$ deviate from their nominal values due to either capacitor ratio errors – for SC circuits [15] – or to transistor size ratio errors – in the case of SI circuits [18]. As a result of these errors, the poles of $H_{res}(z)$ experience movements around their nominal positions – different for each resonator structure as shown in Fig. 12.20.

In some structures the filter poles move around the unity circle in the $Z$-plane. This results in the resonant frequency, $f_n$, not being properly placed. This is the case of LDI-loop resonators and FE-loop resonators under changes on $A_{FB,\,FB2}$. In the Delay-loop and FE-loop structures, the effect of errors will move the resonator poles off the unit circle, causing instability. If the poles move inside the unit circle, then the $Q$ factor will be reduced, thus reducing the gain of $H_{res}$ at $f_n$.

Although the possible instability of FE-loop resonators appears to be a draw-

back as compared to LDI-loop resonators, some authors propose to design filters with a small instability with the objective of reducing idle tones in ΣΔMs [35]. This is still a matter of discussion. In fact, the authors in [14] reported similar experimental results from two $2^{nd}$-order BPΣΔMs, one of them based on LDI-loop resonators and the other one using FE-loop resonators.

The resonator architectures shown in Fig. 12.20 can be implemented using DT circuit techniques. As an illustration, Fig. 12.21 shows the schematics of the resonators in Fig. 12.20 using SC Fully Differential (FD) circuits[†6] [14][34], and Fig. 12.22 shows the corresponding SI (single-ended) realizations[18]. All these

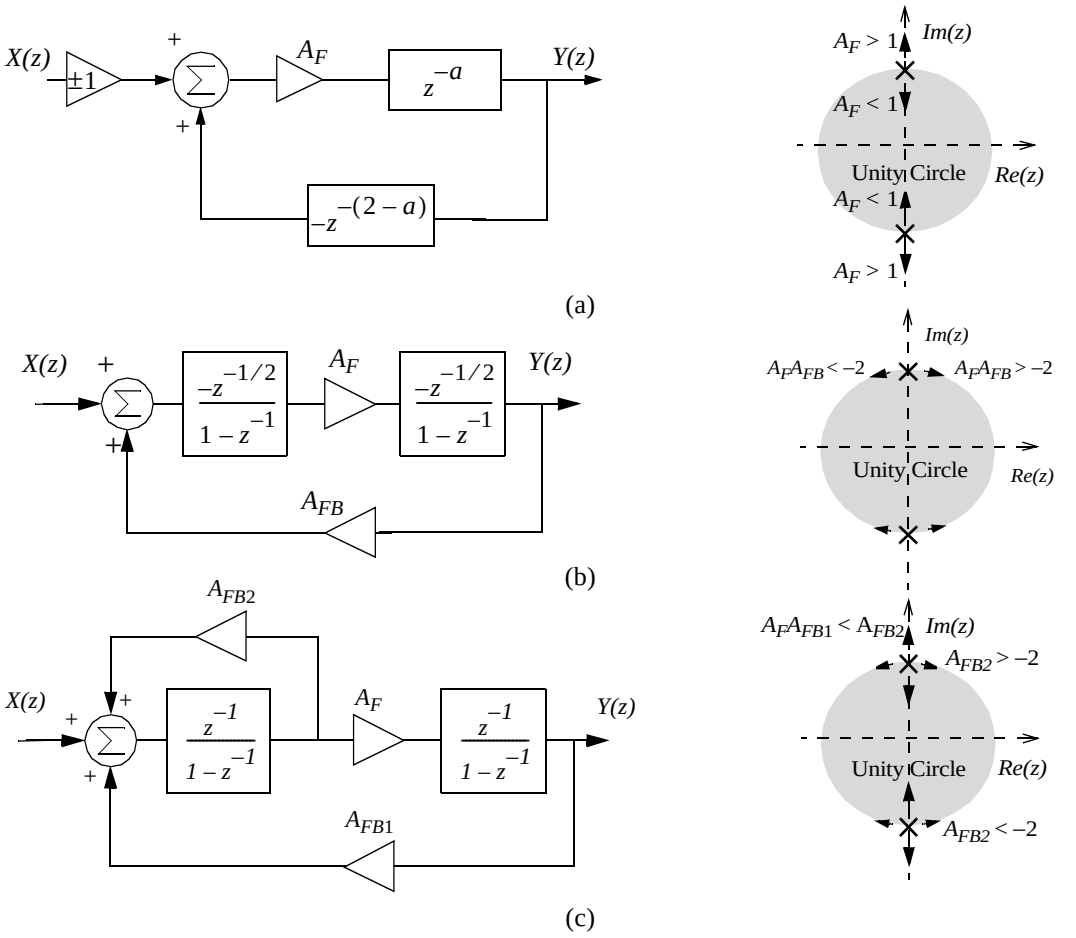



**Figure 12.20:** Different filter implementations of the resonator transfer function and movement of their poles under errors in their feedback gains. a) Delay-loop. b) LDI-loop. c) FE-loop.

6 . SC resonators can be also implemented using a two-path architecture [33][35] – not shown in this Chapter for the sake of simplicity. Their main advantage is that only one opamp is required instead of two as in Fig. 12.21. However, a complex clock phase scheme is used, which needs to be carefully timed in order to avoid image components to appear in the signal band.

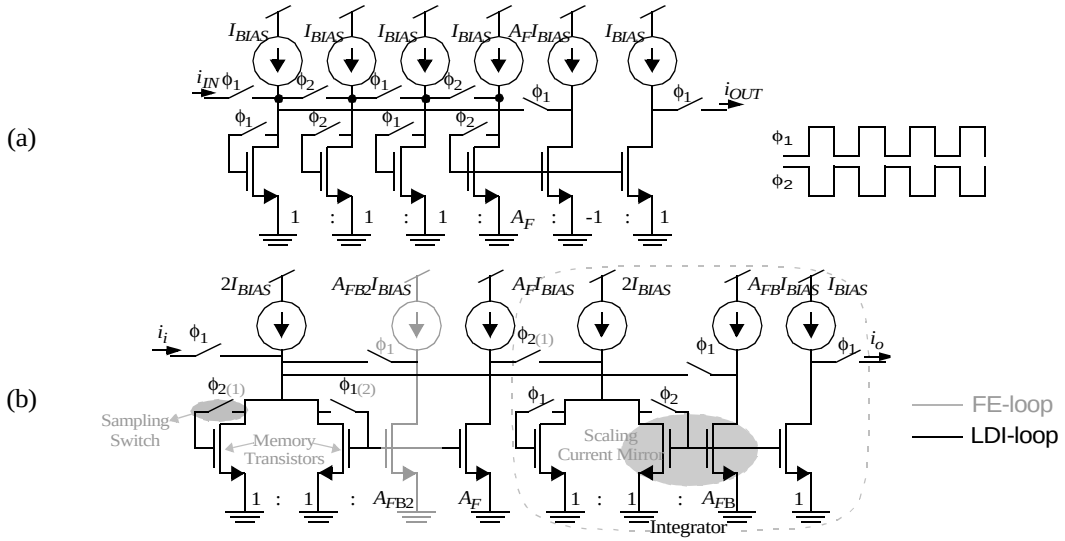



**Figure 12.22:** SI realizations of the resonators in Fig. 12.20. a) Delay-loop and clock phase generator. b) LDI and FE-loop.

resonators have their poles placed at $f_n = f_S/4$ . This is a consequence of the $z^{-1} \rightarrow -z^{-2}$ transformation. However, in some applications such as multi-standard radio receivers, it could be interesting to design the scaling coefficients to be programmable. This will allow us to control $f_n$ without changing $f_S$. This can be done, for instance, by changing $C_{AFB,\,AFB2}/C$ in Fig. 12.21 and the current mirror output transistor size, $A_{FB,\,FB2}$, in Fig. 12.22(b).

In case of CT ($g_m - C$) resonators like that shown in Fig. 12.23, the resonant frequency, given by:

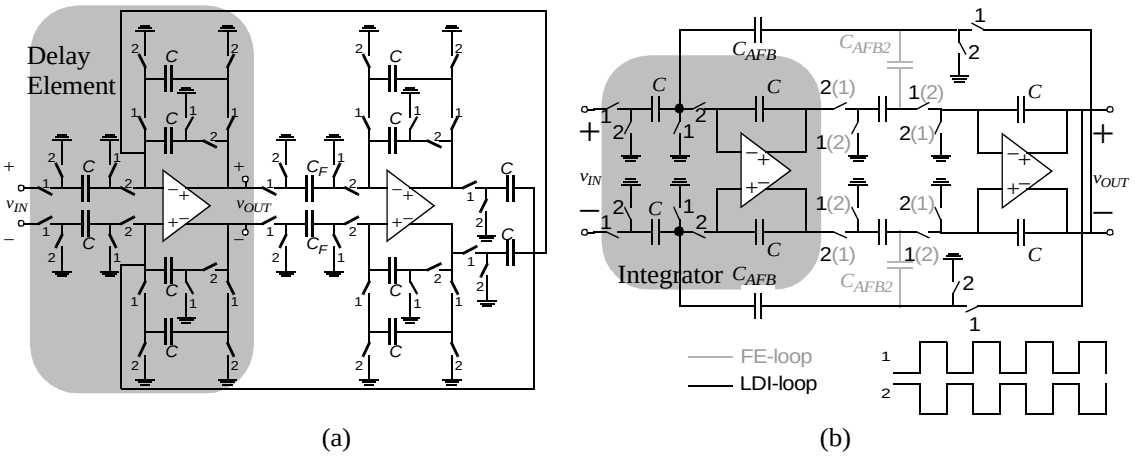



**Figure 12.21:** SC FD realizations of the resonators in Fig. 12.20. a) Delay-loop. b) LDI and FE-loop.

$$f_n = \frac{1}{2\pi}\sqrt{\frac{g_{m2}g_{mR}}{C_1C_2}} \tag{12.18}$$

can be varied by making $g_{mR}$ to be programmable electronically [37].

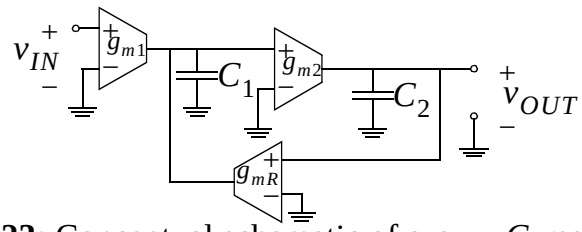



**Figure 12.23:** Conceptual schematic of a $g_m - C$ resonator.

### 11.5.2 Quantization noise shaping degradation due to circuit errors

As discussed in previous section, LDI-loop resonators are the only ones which remain stable under changes in their scaling coefficients. For that practical reason, this has been the resonator structure chosen for our study[†7]. Fig. 12.24 shows the $Z$-domain block diagram of a 1-bit 4th-BPΣΔM based on LDI-loop resonators. Note that the required feedback loop delay has been realized through two additional delay blocks. The scaling factors can be optimized to obtain similar dynamic range for both resonators. This yields to the following nominal values,

$$A_{RES2} = A_{DAC2} = -A_{DAC1} = 1 \qquad A_{RES1} = 1/2 \tag{12.19}$$

Ideally, the $Z$-transform of the modulator output is given by eq.(12.2) with

$$\begin{aligned} S_{TF} &= z^{-2} \\ N_{TF} &= (1+z^{-2})^2 \end{aligned} \tag{12.20}$$

and $P_Q$ and $SNR$ are respectively given by eq.(12.8) and eq.(12.12); with

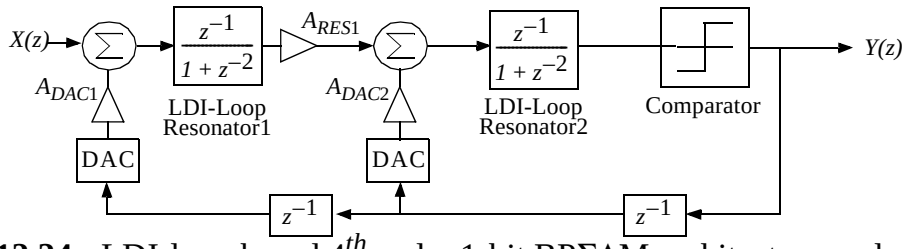



**Figure 12.24:** LDI-loop based $4^{th}$-order 1-bit BPΣΔM architecture under study.

7 . A similar discussion to that presented here can be followed for the case of either FE-loop or Delay-loop based BPΣΔMs.

$f_n = f_S/4$, $N = 1$ and $L = 2$. However, such an ideal performance can only be achieved provided that the resonators in Fig. 12.24 are realized without errors.

In the case of SC realizations, the major sources of error that degrade the noise-shaping of BPΣΔMs are [15]:

- *Finite operational amplifier (opamp) DC gain*, represented by $A_V$.
- *Incomplete settling error,* $\varepsilon_s$, caused by the limited opamp bandwidth. In a first-order approach (single-pole), $\varepsilon_s \equiv \exp[-T_S/(2\tau)]$, where $\tau$ is the closed-loop time constant of the SC integrator.
- *Mismatch capacitor ratio error,* $\varepsilon_m$, in the scaling coefficients ($C_{AFB}/C$ in Fig. 12.21(b)).

In the case of SI BPΣΔMs, the main circuit parasitics are [18]:

- *Finite conductance ratio error*, defined as $\varepsilon_g \equiv 2(g_o/g_i)$, where $g_o$ and $g_i$ are respectively the output and input conductances of SI memory cells.
- *Charge injection error,* $\varepsilon_q$, due to the charge injected, $\delta q$, by the sampling switch onto the storing capacitance, $C_{gs}$, of the memory transistor (see Fig. 12.22(b)).
- *Incomplete settling error*, $\varepsilon_s$, caused by the finite bandwidth, $g_m/C_{gs}$, where $g_m$ is the transconductance of the memory cell.
- *Mismatch error,* $\varepsilon_m$, in $\beta$ and $V_T$, of the current mirror transistors used to implement the scaling coefficients ($A_{FB}$ in Fig. 12.22(b)).

In the presence of the above-mentioned errors, the resonator transfer function is modified into [15][18]

$$H_{res}(z) \cong \frac{(1-\mu)z^{-1}}{1+\xi_1 z^{-1}+(1-\xi_2)z^{-2}} \tag{12.21}$$

where $\mu$, $\xi_1$ and $\xi_2$ are different for each error, as Table 12.2 shows.

Replacing the transfer functions of the resonators in Fig. 12.24 with eq.(12.21), the erroneous $N_{TF}$ of the 4th-BPΣΔM is obtained, giving:

$$N_{TF}(z) \cong [1+\xi_1 z^{-1}+(1-\xi_2)z^{-2}]^2 \tag{12.22}$$

The zeroes of $N_{TF}$ are shifted from their nominal positions at $f_S/4$, thus degrading the filtering performed by the resonators and making the quantization

noise in-band power, and correspondingly, the $SNR$ to decrease.

From eq.(12.7)-eq.(12.10) and eq.(12.22), it can be shown that the erroneous $P_Q$ and $DR$ are approximately given by [18]:

$$P_Q = \frac{\pi^4 \Delta^2}{60M^5}(\nabla P_Q) \qquad DR \cong \frac{15M^5}{2\pi^4(\nabla P_Q)} \tag{12.23}$$

where

$$\nabla P_Q \equiv 1 + \frac{10}{3}(3\xi_1^2 + \xi_2^2)\left(\frac{M}{\pi}\right)^2 + 5(\xi_1^2 + \xi_2^2)^2\left(\frac{M}{\pi}\right)^4 \tag{12.24}$$

is the in-band quantization noise increase caused by circuit parasitics, which in combination with the expressions for $\xi_1, \xi_2$ given in Table 12.2, allow us to know the maximum error permitted as a function of $M$ for a given $DR$.

In addition to the $DR$ loss, circuit parasitics cause a shifting of the position of $f_n$, denoted as $\delta f_n$. Solving the roots of eq.(12.22) and assuming that $\xi_1, \xi_2 \ll 1$, it can be shown that:

**Table 12.2:** Resonator transfer function degradation with circuit errors.

| SC CIRCUITS | $\mu$ | $\xi_1$ | $\xi_2$ |
|---|---|---|---|
| $A_V$ | $\frac{2}{A_V}\left(1 + \frac{C_S}{C_I}\right)$ | $\frac{-2}{A_V}\left(2 + \frac{C_S}{C_I}\right)$ | $\frac{2}{A_V}\frac{C_S}{C_I}$ †* |
| $\varepsilon_s \equiv \exp\left(\frac{-T_S}{2\tau}\right)$ | $2\varepsilon_s$ | $-4\varepsilon_s$ | 0 |
| $\varepsilon_m \equiv \frac{\delta C_{AFB}}{C_{AFB}} - \frac{\delta C}{\delta C}$ | $\varepsilon_m$ | $\varepsilon_m$ | 0 |
| SI CIRCUITS | | | |
| $\varepsilon_g \equiv \frac{2g_o}{g_i}, \varepsilon_q \equiv \frac{\delta q}{C_{gs}(V_{GS} - V_T)\big\|_Q}$ | $2\varepsilon_{g,q}$ | 0 | $4\varepsilon_{g,q}$ |
| $\varepsilon_s \equiv \exp\left(\frac{-T_s g_m}{2C_{gs}}\right)$ | $2\varepsilon_s$ | $-4\varepsilon_s$ | $4\varepsilon_s$ |
| $\varepsilon_m \equiv \frac{\delta\beta}{\beta} - \frac{\delta V_T}{(V_{GS} - V_T)\big\|_Q}$ | $\varepsilon_m$ | $\varepsilon_m$ | 0 |

* $C_s$ and $C_I$ represent the sampling and the integration capacitances, respectively.

$$\delta f_n \equiv f_n - \frac{f_S}{4} \cong \xi_1 \frac{M}{\pi}\left(\frac{B_w}{2}\right) \tag{12.25}$$

Thus, depending on the way that the noise shaping of BPΣΔMs is degraded by circuit errors, they can be grouped in the following families:

- Those errors that cause $\xi_1 = 0, \xi_2 \neq 0$, and hence, their main effect is to reduce the Q-factor of the resonator transfer function, thus lowering the bandstop attenuation of the modulator bandpass filtering, increasing $P_Q$ as illustrated in Fig.12.25(a).
- Those errors in which $\xi_1 \neq 0, \xi_2 = 0$, whose main effect is to change $f_n$. However, $P_Q$ does not significantly increase as shown in Fig.12.25(b).
- Those errors in which $\xi_1 \neq 0, \xi_2 \neq 0$ , causing a combined effect of increasing $P_Q$ and shifting $f_n$ , as illustrated in Fig.12.25(c).

All these results have been validated by time-domain behavioural simulation [15][18]. Thus, Fig.12.25 compares the theoretical model – solid line – with simulation showing a good agreement between simulation and theory.

### 11.5.3 Harmonic distortion in bandpass SD modulators

In Section 11.5.2, circuit errors have been assumed to be linear. However, practically all errors are signal-dependent and hence, in addition to degrade $N_{TF}$, cause Harmonic Distortion (HD) in BPΣΔMs.

As an illustration, Fig. 12.26 shows the increase of the $3^{rd}$-order InterModulation distortion[†8], $IM_3$, due to non-linear settling in FD 4th-BPΣΔMs based on SI

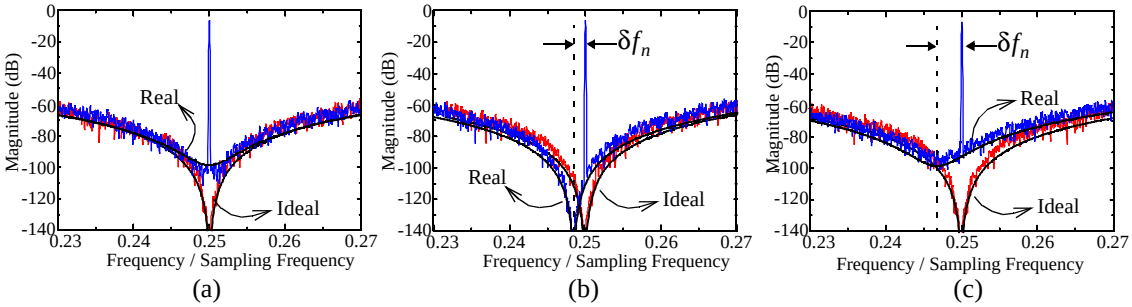



**Figure 12.25:** Noise-shaping degradation with circuit errors: a) $\xi_1 = 0, \xi_2 \neq 0$. b) $\xi_1 \neq 0, \xi_2 = 0$. c) $\xi_1 \neq 0, \xi_2 \neq 0$ .

8 . In bandpass signal processing, $IM_3$ is a more appropriate figure than $HD_3$ for measuring HD. Assuming an input signal formed by two tones at $f_2, f_1$, $IM_3$ is defined as the amplitude of the output at $2f_2 - f_1$ and $2f_1 - f_2$ related to the output amplitudes at $f_2, f_1$.

circuits. In this case, the major source of non linearity is the signal-dependent, $g_m$, which causes main SI errors ($\varepsilon_g$, $\varepsilon_q$ and $\varepsilon_s$) to be non-linear [18].

As in LPΣΔMs, the non-linearity of voltage-mode (SC and $g_m - C$) BPΣΔMs is mainly caused by the following error mechanisms [25]:

- *Slew-Rate*, due to the saturation of the opamp in current, causing a non-linear transient response of the integrator.
- *Non-linear open-loop DC-gain of the opamp*, due to the fact that the transition between the linear and saturation output region is gradual. This effect can be modelled as polynomial dependence of $A_V$ on the opamp output (input), $A_V = A_0(1 + \gamma_1 v + \gamma_2 v^2 + \ldots)$.[†9]
- *Non-linear capacitors*, due to the dependency of the value of the capacitance on its stored voltage; modeled as $C(v) = C^o(1 + \alpha v + \beta v^2 + \ldots)$, where $\alpha, \beta, \ldots$ are non-linear technology-dependent coefficients.

Considering the effect of non-linear errors, the behaviour of a LDI-loop resonator can be generically expressed by the following equation [18][†10]:

$$x_{o,n} = (1-\mu)x_{i,n-1} - \xi_1 x_{o,n-1} - (1-\xi_2)x_{o,n-2} + F_{NL}(x_{i,n}, x_{i,n-1}, \ldots, x_{o,n}, x_{o,n-1}, \ldots, \overline{\xi_{NL}}) \quad (12.26)$$

where $F_{NL}$ represents the non-linearity, which is function of the resonator input, $x_i$, the output, $x_o$, and a vector of electrical parameters, $\overline{\xi_{NL}}$ – different for each error mechanism.

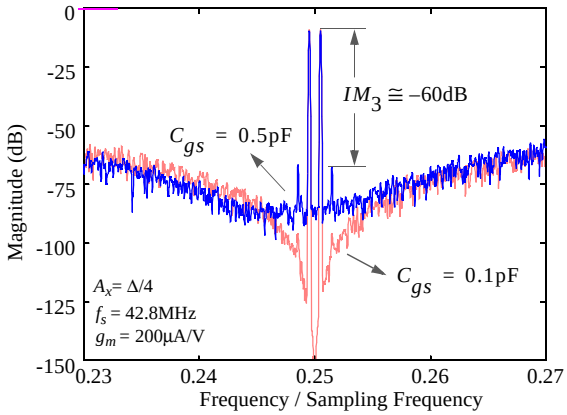



**Figure 12.26:** Harmonic Distortion in SI BPΣΔMs due to non-linear settling.

9 . In CT-BPΣΔMs, the effect caused by the non-linear transconductor is similar to that due to $SR$ and the non-linear $A_V$ in SC circuits [20].

10 .In this Chapter, $x_n$ denotes $x(nT_S)$.

The obtainment of design equations for $IM_3$ requires solving the time-domain equations that govern the behaviour of BPΣΔMs, considering that the first resonator[†11] behaviour is given by eq.(12.26).

Instead of deriving cumbersome expressions of $IM_3$ for each signal-dependent parasitics – beyond the scope of this Chapter[†12] –, we will center our attention on a critical effect: the non-linear sampling process. Contrary to the lowpass case, this error mechanism constitutes one of the most limiting factors in BPΣΔMs used in modern telecommunication systems.

In the front-end of such systems, the input (analog) signal is changing very quickly during the sampling phase interval. As an illustration, Fig. 12.27 shows the transient evolution of a sinusoidal signal of amplitude $X$ and frequency $f_i \cong f_S/4$ , when sampled at $f_S$. In this case, corresponding to a typical input signal in BPΣΔMs, the signal amplitude can change up to $X/\sqrt{2}$ during the sampling phase. This change leads to a non-linear transient response of the sampling circuit which manifests as HD at the output of the BPΣΔM.

For a better understanding of this phenomenon, let us consider the input stage of the SC resonators shown in Fig. 12.21(b). During the clock phase 1 (sampling phase), the input signal, $v_{IN}$, is stored in the capacitor $C$. In practice, this circuit is realized by using CMOS switches as shown in Fig. 12.28(a). These switches are sized such that the *switch-on* resistance, $R_{on}$, verifies $R_{on}Cf_s \ll 1$, thus making the incomplete settling error negligible. This condition is not difficult to satisfy in

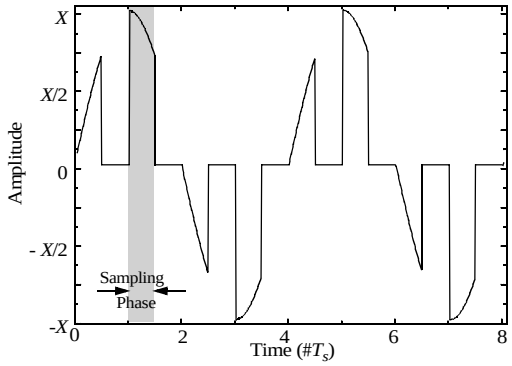



**Figure 12.27:** Transient evolution of a input sinusoidal signal of amplitude $X$ an frequency $f_i \cong f_S/4$ when sampled at $f_S/4$.

11 .The contribution of the second resonator to HD is attenuated by the gain of the first resonator in the signal band. For this reason, only the first resonator contribution has to be considered.

12 .The interested reader is referred to [18] where a complete analysis of HD in SI BPΣΔMs is described for each non-linear error.

practice. However, $R_{on}$ strongly depends on the input signal amplitude as illustrated in Fig. 12.28(b) for a CMOS switch in a 2.5V-0.25µm CMOS technology. As a consequence of this non-linearity, the sampling circuit will cause HD. Based on the Volterra series method, the authors in [38] demonstrated that, in FD SC circuits like that in Fig. 12.28(a), the HD due non-linear sampling is given by:

$$HD_3 \cong \frac{\pi f_i C R_{on}}{2(V_{ON} - V_T)^2} V_{IN}^2 \tag{12.27}$$

where $V_{ON}$ stands for the switch-on voltage[†13].

Note that, $HD_3$ increases with the input frequency. This is because, as the input signal frequency becomes higher, there will be a larger variation of the signal amplitude during the sampling phase, thus enlarging the effect of the $R_{on}$ non-linearity.

An important conclusion derived from eq.(12.27) is that, even for low values of the incomplete settling error, high levels of HD can be obtained. This suggests that, in some applications, either clock-boosting or similar techniques should be used to reduce the effect of non-linear sampling [36].

A similar conclusion can be found in SI BPΣΔMs [18]. In this case, the HD due to dynamic errors is dominated by the non-linear sampling of the front-end memory cell. As an illustration, Fig. 12.29 compares the HD caused by the non-linear sampling with that caused by the incomplete settling. Note that, in practical cases, that is, $\varepsilon_s < 0.1\%$, the HD is dominated by the non-linear sampling.

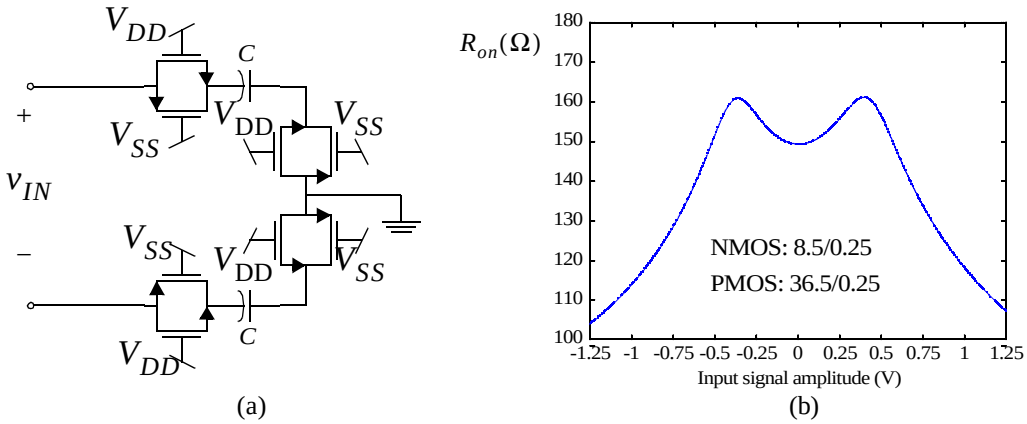



**Figure 12.28:** Non-linear sampling in SC BPΣΔMs. a) Sampling circuit. b) DC characteristic of CMOS switches (2.5V-0.25µm CMOS technology).

13 .The study developed in [38] is based on NMOS switches instead of CMOS switches. In this case, $V_{ON} = V_{DD}$.

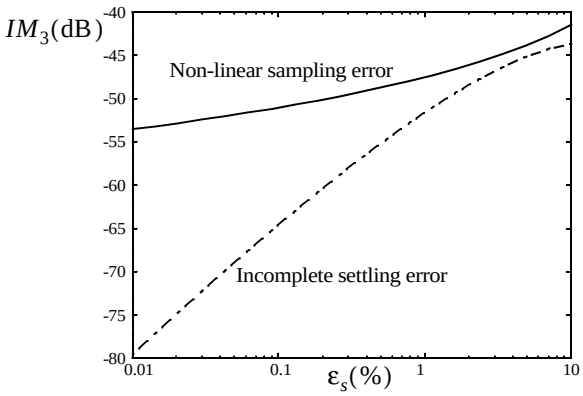


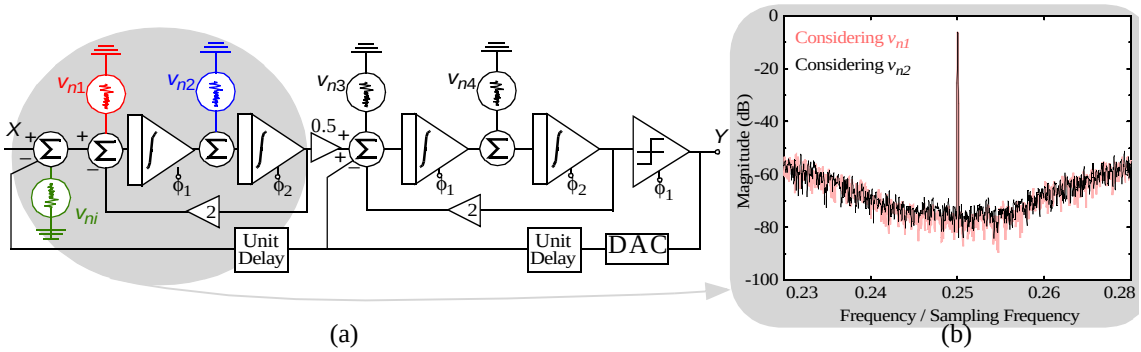

**Figure 12.29:** Comparison of the HD caused by the incomplete settling error and the non-linear sampling in SI BPΣΔMs.

### 11.5.4 Thermal noise

Thermal noise constitutes the ultimate limiting factor of BPΣΔMs. As for the LPΣΔM case, only the thermal noise contributions at the input node of the modulator will be important because they are added directly to the input signal, thus appearing with no filtering in the output spectrum.

In DT BPΣΔMs, as a consequence of the S/H operation, the input-referred noise PSD increases with respect to the CT case. This increase is proportional to the relationship between the equivalent noise bandwidth and the sampling frequency. For that reason, we will center on DT (SC or SI) realizations.

Fig. 12.30(a) shows the most important thermal noise sources in a LDI-based 4th-BPΣΔM. In this block diagram, $v_{nm}$ represents the input-equivalent noise source of the $m$-th integrator. In practical cases, noise contributions of DACs can be considered negligible as compared to that due to resonators. In addition, the noise contributions of both the 3rd- and the 4th- integrators are attenuated by the gain of the 1st resonator in the signal bandwidth. However, the contribution of the 2nd integrator, $v_{n2}$, has to be considered as illustrated in the output spectrum of




(a) (b)

**Figure 12.30:** Thermal noise in LDI-loop based 4th-BPΣΔMs. a) Most important noise sources. b) Contribution to the output spectrum noise.

Fig. 12.30(b).

It can be shown that the contribution of $v_{n2}$ to the input-equivalent noise, $v_{ni}$, is twice that of that due to $v_{n1}$ because in the signal band [18],

$$\left|1 - z^{-1}\right|^2 \Big|_{z = e^{-j2\pi B_w T_s}} \cong 2 \tag{12.28}$$

Therefore, the in-band power of $v_{ni}$ is approximately given by:

$$P_{ni} \cong P_{n1} + 2P_{n2} \tag{12.29}$$

where $P_{n1}$ and $P_{n2}$ are respectively the in-band power of $v_{n1}$ and $v_{n2}$.

In case that $P_{ni} > P_Q$, the *SNR* and the *DR* for a sinusoidal input signal of amplitude $A = \alpha\Delta/2$ are respectively given by:

$$SNR_{th} \cong \frac{\alpha^2\Delta^2}{8P_{ni}} \qquad DR_{th} \cong \frac{\Delta^2}{8P_{ni}} \tag{12.30}$$

### 11.5.5 Jitter noise

In previous sections, ideal clock phase signals have been considered. In practice, the period of the clock signal presents random variations in its nominal value as illustrated in Fig. 12.31(a). This is due to certain intrinsic uncertainties in the time in which clock transitions occur, known as *jitter*. The result is a non-uniform sampling, responsible for extra (white) noise at the output of ΣΔMs [12].

As a consequence of jitter, it can be shown that the *SNR* of DT-BPΣΔMs is degraded as [31]:

$$SNR\big|_{\mathrm{DTj}} = \frac{M}{4\pi^2\sigma_j^2 f_n^2} \tag{12.31}$$

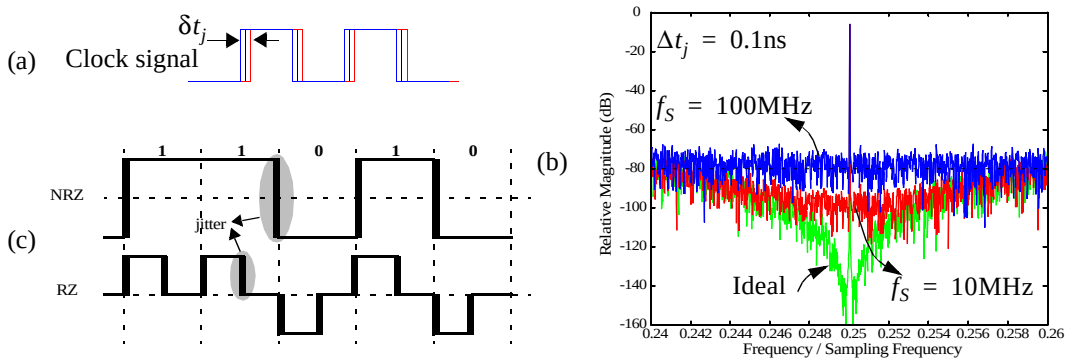



**Figure 12.31:** Jitter noise. a) Uncertainties in the clock transitions. b) Effect on DT-BPΣΔMs. c) Jitter in both NRZ and RZ DAC output responses.

where $\sigma_j$ is the standard deviation of the sampling time error, $\delta t_j$ [†14].

Note that, as in LPΣΔMs, $SNR|_{\mathrm{DTj}}$ decreases with the signal frequency. However, in BPΣΔMs the signal frequency is a substantial fraction of $f_S$, typically $f_n \cong f_S/4$, what constitutes a more limiting factor. As an illustration, Fig. 12.31(b) shows the increase of the in-band jitter noise with $f_S$ in BPΣΔMs.

Jitter noise is specially critical in CT BPΣΔMs. In this type of BPΣΔMs, clock jitter comes from two sources[†15]: the S/H circuit and the DAC. The former is subject to the same filtering than the quantization error, and hence, will have a small effect on the modulator performance. However, the DAC jitter noise is directly added with the input signal, thus increasing the in-band noise power. This power increase will depend on the impulsive response of the DAC. This is because jitter only matters when the DAC output changes sign. Thus, as illustrated in Fig. 12.31(c), for the same bit sequence, the number of DAC output rising/falling edges per clock cycle will depend on the type of DAC response. This will manifest as a different $SNR$ degradation, given by [31]:

$$SNR|_{\mathrm{CTj}} \cong \begin{cases} \dfrac{\mathrm{sinc}(\pi f_n T_S)}{64\sigma_j^2 B_w^2 M} & \text{for NRZ DACs} \\ \dfrac{\mathrm{sinc}(\pi f_n T_S)}{64\left(\dfrac{T_S}{T_0}\right)^2 \sigma_j^2 B_w^2 M} & \text{for RZ DACs} \end{cases} \tag{12.32}$$

Note that, as Fig. 12.31(c) predicts, a lower $SNR$ degradation is achieved by using NRZ DACs. Thus, comparing eq.(12.31) and eq.(12.32) it can be shown that CT-BPΣΔMs are more sensitive to jitter than DT-BPΣΔMs. For instance, considering NRZ DACs in eq.(12.32) (the best case) and $f_n \cong f_S/4$, the condition

$$\sigma_j^2\Big|_{\mathrm{CT}} = \sigma_j^2\Big|_{\mathrm{DT}} \left(\frac{\pi}{8}\right)^2 \mathrm{sinc}\left(\frac{\pi}{4}\right) \cong 0.14\sigma_j^2\Big|_{\mathrm{DT}} \tag{12.33}$$

should be satisfied to obtain the same $SNR$ loss in both CT- and DT-BPΣΔMs.

---

14 .The clock jitter error, represented here by parameter $\delta t_j$, behaves as a random variable with a Gaussian distribution of standard deviation $\sigma_j$ and zero mean.

15 .There is another source of jitter noise caused by comparator *metastability*. This non-ideal effect causes an increase of the in-band noise which can be modelled as a jitter noise as shown in [20]. This kind of jitter is often referred to as signal-dependent jitter because it is due to the signal-dependent comparator delay.

Besides jitter, the DAC time response causes another important degradation in CT-BPΣΔMs which is analyzed in next section.

### 11.5.6 Excess loop delay in continuous-time BPSDMs

Ideally, the DAC output currents[†16] should respond immediately to the quantizer clock edge. In practice, there exists a delay, as illustrated in the *multi-feedback* CT-BPΣΔM[†17] of Fig. 12.32(a). This delay, often referred to as *excess loop delay* or *loop delay*, is normally expressed as a fraction of the sampling period, $\tau_d = \rho_d T_s$, where $0 < \rho_d \leq 1$.

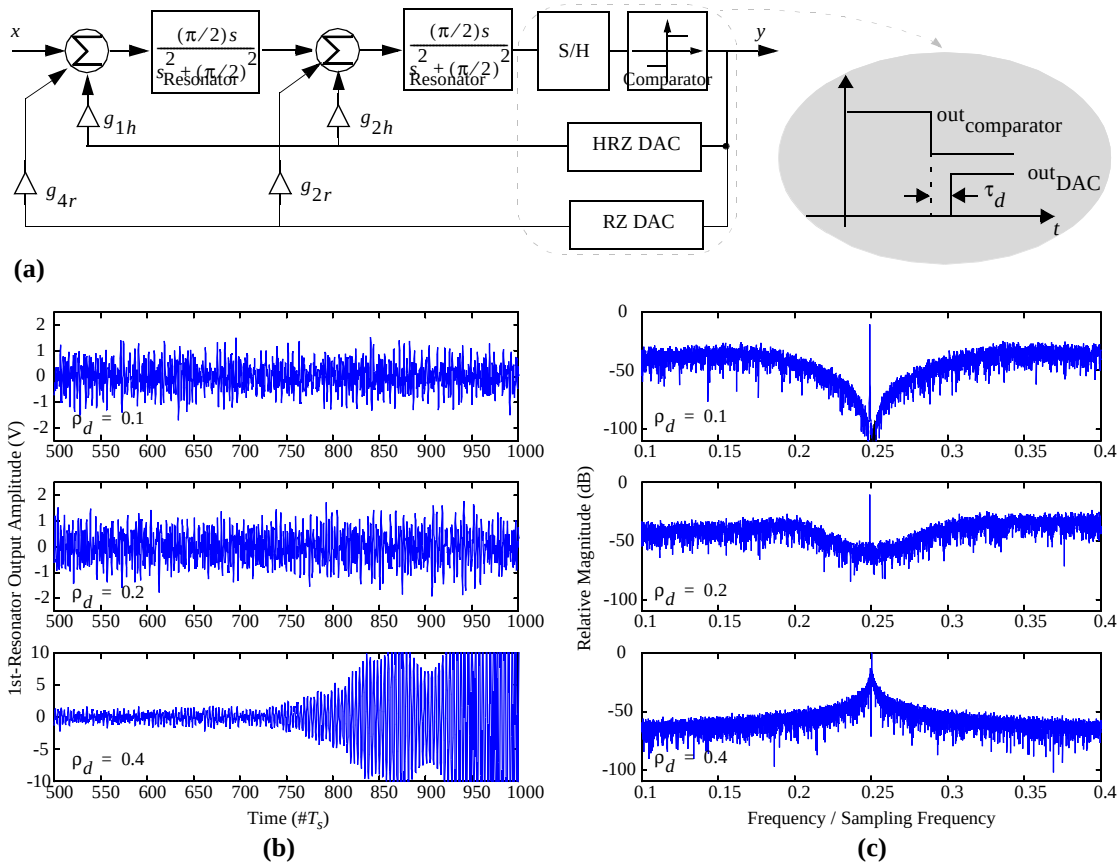



**Figure 12.32:** Excess loop delay. a) DAC time response in CT-BPΣΔMs. Effect on: b) Transient response of first resonator. c) Modulator output spectrum.

16 .In most of CT-BPΣΔMs, DACs are realized by differential pairs driven by the quantizer output.

17 .This architecture uses different types of DACs – each with separately feedback coefficients – to obtain similar noise-shaping than that of the DT-BPΣΔM in Fig. 12.24 [32]. This strategy allows us to use resonator transfer function of the type $s/(s^2+\omega^2)$, which are easier to realize through $g_m C$ circuits than the CT filters resulting from a DT-to-CT transformation like that in eq.(12.16).

As a consequence of the poles introduced by $\rho_d \neq 0$, the noise-shaping transfer functions, $S_{TF}$ and $N_{TF}$, are modified, thus increasing the in-band noise power as illustrated in Fig. 12.32(c). This effect becomes specially critical in telecom applications, in which large values of $\rho_d - \rho_d \cong 0.4$ in the example of Fig. 12.32(b)-(c) – may eventually make CT-BPΣΔMs unstable [20].

Mathematically speaking, complex analyses are required to obtain the stability condition in most common BP-CTΣΔM architectures. Instead of that, simulation-based analyses are normally used to know the critical value of $\rho_d$ leading to instability. This simulation-based approach is used – in combination with other strategies such as coefficient tunning and adding extra DAC branches – to compensate for the excess loop delay as stated in [20].

## 11.6 STATE-OF-THE-ART BANDPASS ΣΔ ADCS

Although the idea of translating the zeroes of $N_{TF}$ from DC to any given IF location was originally presented by Schreier and Snelgrove in 1989 [5], it was not until 1992 that Jantzi, Snelgrove and Ferguson published the first monolithic BPΣΔM IC [39]. Since then, there have been a large number of ICs implemented in several technologies, with diverse circuit techniques; using different supply voltages.

Table 12.3 shows a summary of the CMOS BPΣΔ ADC ICs published to this day. For each of them, the most significant figures are shown, namely: $DR$, $SNR$, $f_S$, $f_n$, $B_w$, the power consumption, the characteristics of the fabrication process and the modulator architecture. For the latter, the synthesis method employed is also given. Note that most modulators use a single-loop architecture, obtained by applying the $z^{-1} \rightarrow -z^{-2}$ transformation, which, as stated in Section 11.4.1, makes $f_n = f_S/4$.

The BPΣΔMs in Table 12.3 cover multiple applications in digital wireless communications, ranging from telemetering [40] to digital radio receivers [13] [14][19][23][33] and modern cellular phones [22][34][41][42]. Depending on the application, there are different specifications for $DR$, $B_w$ and $f_n$. Hence, it is difficult to state a measure of comparison among all reported modulators. Thus, in order to compare different performances, the following *Figure-Of-Merit* ($FOM$) will be used for BPΣΔMs [†18]:

**Table 12.3:** Summary of CMOS bandpass ΣΔ modulators published up to now.

| Author[†*] | $DR$ (bit) | $f_S$ (MHz) | $f_n$ (MHz) | $B_w$ (kHz) | Power (mW) | Technology | Architecture |
|---|---|---|---|---|---|---|---|
| Jantzi'93 [13] | 10.2 | 1.825 | 0.455 | 8 | 210 | 3μm DP / 5V | 4th, Optim. $N_{TF}$ |
| Longo'93 [34] | 15 | 7.2 | 1.8 | 30 | -- | 1μm DP / 5V | 4th, $z^{-1} \rightarrow -z^{-2}$ |
| Song'95 [41] | 9 | 8 | 2 | 30 | 0.8 | 2μm DP / 3.3V | 4th, $z^{-1} \rightarrow -z^{-2}$ |
| Hairapetian'96 [33] | 11.7 | 13 | 3.25 | 200 | 14.4 | 0.8μm DP / 3V | 4-2, $z^{-1} \rightarrow -z^{-2}$ |
| André'96 [43] | 8 | 8 | 2 | 64 | 8 | 0.5μm DP / 3.3V | 6th, $z^{-1} \rightarrow -z^{-2}$ |
| Liu'97 [44] | 11.8 | 0.827 | 0.413 | 2 | -- | 2μm DP / 5V | 4th, Optim. $N_{TF}$ |
| Cormier'97 [21] | 9.5 | 1.25 | 0.25-.375 | 6.25 | -- | 2μm DP / 5V | 4th, $z^{-1} \rightarrow -z^{-2}$ |
| Ong'97 [30] | 12.2 | 80 | 20 | 200 | 72 | 0.6μm SP 3.3V | 4th, $z^{-1} \rightarrow -z^{-2}$ |
| Jantzi'97 [28] | 10.8 | 10 | 3.75 | 200 | 130 | 0.8μm SP / 5V | 4th, Quadrature |
| André'98 [45] | 9.2 | 4 | 1 | 200 | 19 | 0.5μm DP / 3V | 3th-3bit, Optim. $N_{TF}$ |
| Bazarjani'98 [46] | 6.7 | 40 | 20 | 1250 | 65 | 0.5μm DP / 5V | 2nd, $z^{-1} \rightarrow -z^{-2}$ |
| Chuang'98 [47] | 13 | 0.5 | 0.125 | 0.5 | -- | 2μm DP / 5V | 6th, Optim. $N_{TF}$ |
| Van Engelen'99 [19] | 11.7 | 40 | 9.15 | 200 | 60 | 0.5μm DP / 5V | 6th, CT |
| | 10.8 | 80 | 10.7 | 200 | | | |
| Park'99 [48] | 12.2 | 20 | 5 | 200 | 180 | 0.65μm SP / 4V | 4th, $z^{-1} \rightarrow -z^{-2}$ |
| Tabatabaei'99 [42] | 13 | 80 | 20 | 1250 | 90 | 0.25μm DP/ 2.5V | 6th, $z^{-1} \rightarrow -z^{-2}$ |
| Tonietto'99 [49] | 12.7 | 42.8 | 10.7 | 200 | 80 | 0.35μm SP / 3.3V | 6th, Optim. $N_{TF}$ |
| Bazarjani'99 [50] | 9.4 | 68 | 17 | 1250 | 48 | 0.6μm DP / 3V | 4-4, $z^{-1} \rightarrow -z^{-2}$ |
| Tao'99 [51] | 8 | 400 | 100 | 200 | 330 | 0.35μm SP/ 3.3V | 2nd, CT |
| Tabatabaei'00 [52] | 12 | 64 | 16 | 2000 | 110 | 0.25μm SP/ 2.5V | 6th, 2-path |
| Cusitano'00 [53] | 12 | 37.05 | 10.7 | 200 | 116 | 0.35μm SP/ 3.3V | 6th, Optim. $N_{TF}$ |
| Cheung'01[54] | 6.7 | 42.8 | 10.7 | 200 | 12 | 0.35μm SP/ 1V | 2nd, $z^{-1} \rightarrow -z^{-2}$ |
| Salo'02 [36] | 11.7 | 80 | 20 | 270 | 56 | 0.35μm?P/ 3V | 4th, $z^{-1} \rightarrow -z^{-2}$ |
| | 6.7 | | | 3840 | | | |
| Ueno'02 [55] | 12.6 | 10 | 0.566 | 250 | 77 | 0.25μm DP/ 2.5V | 2-2, 3bit |

*** Sorted by date of publication.**

$$FOM_{BP} = \frac{\text{Power (mW)}}{2^{DR(bits)} \times f_n(\text{MHz})} \tag{12.34}$$

Fig. 12.33, plots $FOM_{BP}$ vs. $B_w$ for the modulators in Table 12.3. Note that, the best trade-off among power consumption, resolution and $f_n$ is obtained by LP-to-BP BPΣΔMs, most of them using SC circuits. However, to the best of our

18 .As proposed in [25], $FOM = [\text{Power(W)} \times 10^{12}]/[2^{\text{Resolution(bit)}} \times f_d(\text{Samples/s})]$ can be used for comparative evaluation of LPΣΔMs. This formula, which represents the energy (expressed in picojoules) needed per conversion, is not suited to compare BPΣΔMs because it does not include $f_n$. However, this data constitutes one of the most important design specifications.

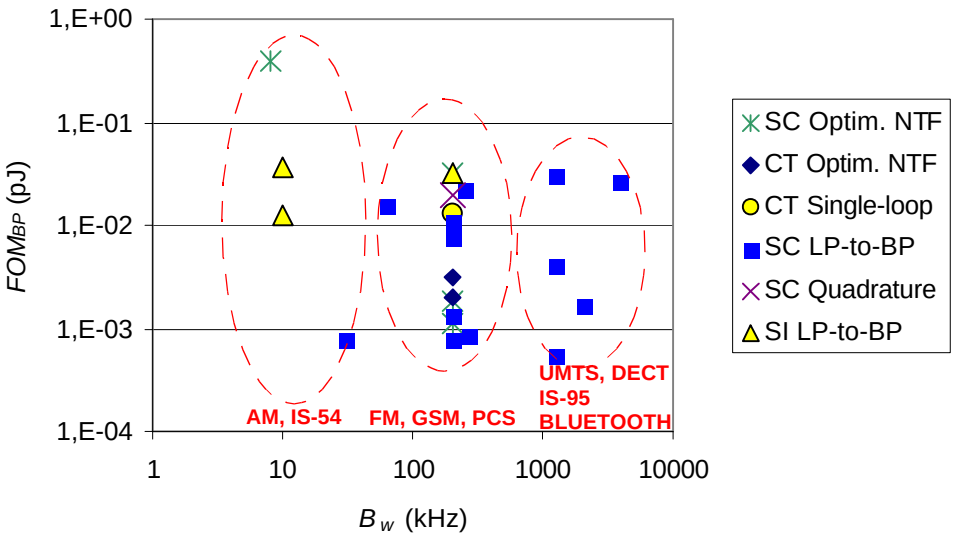



**Figure 12.33:** $FOM_{BP}$ vs. $B_w$ for the modulators in Table 12.3.

knowledge, only a few of them were integrated in a standard CMOS process [30][48][54]. This is due to the fact that SC circuits are very sensitive to capacitor linearity and most linear capacitor structures are formed by two poly layers – not available in standard processes.

This fact has motivated the exploration of other analog techniques compatible with standard, digital VLSI technologies. This is the case of SI circuits, which during the last few years have been used for different analog functions, including filtering and A/D conversion [18][56][57].

In the case of LPΣΔMs, the potential advantages of SI circuits have not been demonstrated in practice. To illustrate this, Fig. 12.34 compares the $FOM$ of both

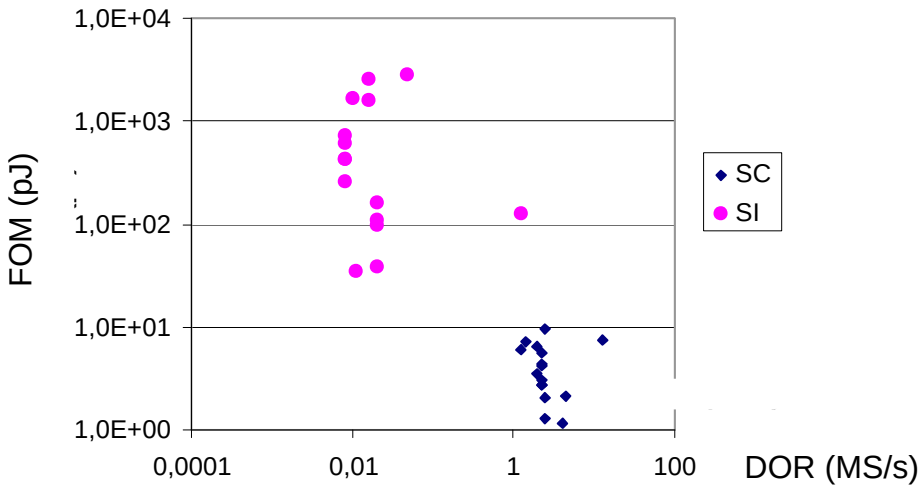



**Figure 12.34:** $FOM$ vs. $f_d$ (DOR) for both SI and SC LPΣΔMs.

SI and SC LPΣΔMs reported in literature. Note that the performance obtained by SI circuits is worse than that obtained by SC circuits. Observe that, while most SC modulators feature an $FOM$ below about $10\text{pJ}$, practically all SI modulators obtain an $FOM$ above $100\text{pJ}$.

However, as demonstrated in [18], the performance of SI ΣΔMs can be enhanced by means of a design methodology supported by a systematic analysis and modeling of error mechanisms. This is illustrated in Fig. 12.33, where the performance of the SI BPΣΔMs reported in [18] – intended for digital radio receivers – is compared to that of the BPΣΔMs in Table 12.3. It can be seen that Fig. 12.33 shows a better performance comparison between SI and SC than in LPΣΔMs (Fig. 12.34), thus demonstrating that the SI technique is a viable alternative to the traditional SC technique for implementing BPΣΔMs in deep submicron CMOS technologies.

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