Control and Acquisition System for a High Dynamic Range CMOS Image Sensor

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***Abstract*—A control and acquisition system for the visualization of the images captured with a High Dynamic Range (HDR) CMOS Image Sensor is developed. The image sensor is inserted in a PCB system, which performs low level control, in communication with a PC software, which performs high level control and images visualization. In order to make it user-friendly, we have opted to use object-oriented method to implement the computer software. The system has an attractive interface, and it is easy to operate. It also includes additional functionalities, such as the increment of the frame rate, enhancement of human perception of details contained in the depicted scene and the possibility to display statistical data for illustrating the behavior of the chip.**

I. Introduction

Since the invention of the photography, the method of the cameras for capturing visible light has evolved from chemical to electronic ones. Despite the high evolution during last decades, some old limitations still survive in the modern electronic cameras. The ideal behavior of an image sensor should have no sensor noise, infinite dynamic range (or at least the maximum dynamic range found in real scenes), high spectral responsivity, very high number of pixels, zero energy consumption and low manufacturing cost. Despite it is technically impossible to achieve these characteristics, great effort has been focus toward number of pixels (lowering pixel size), cost and power consumption producing significant advancement in these aspects. The rest of the properties, such as dynamic range, have experiment a lower development or even decay as pixel shrinking generally diminishes the dynamic range.

The Dynamic Range (DR) in image sensors or imagers is defined as the ratio between the maximum and the minimum measurable illuminations, which must be superior to the DR of the scene in order to be properly captured. However, the dynamic range of the natural world is high, where the difference in contrast is over 100,000,000:1 (DR $>$ 160dB) [1][2]. We have to distinguish two kinds of High Dynamic Range (HDR) situations:

- Inter-frame HDR: the high difference in illuminations does not take place simultaneously (e.g. change of average illumination during the day).
- Intra-frame HDR: the high difference in illuminations takes place in the same frame or scene (e.g. an scene containing both an outdoor area illuminated by direct sunlight and an indoor area illuminated by interior light or even in shadows).

Inter-frame HDR captures can be performed controlling the exposure time. However, intra-frame HDR scenarios imply more complex mechanisms in other to be properly captured. This defines the field of research of High Dynamic Range Image Sensors because typical cameras are limited in intra-frame dynamic range (50-70dB) and some applications need cameras that are prepared to capture images in HDR scene environments in order to work properly.

HDR sensors usually compress the sensed illuminations in order to create a Low Dynamic Range (LDR) representation (avoiding large bit word per pixel), which can be easily displayed and processed. The proposed system is intended to serve as a platform to show the capabilities of a High Dynamic Range CMOS Image Sensor. The system is composed by a Printed Circuit Board, which performs the low level control, in communication with a PC program, which performs the high level control and images visualization. The scheme of the system is shown in Fig. 1.

The organization of paper is as follows. First, the hardware architecture of the system is described. Second, the software implementation is explained. And finally, the image capture operation is detailed.

II. Printed Circuit Board

The HDR Imager is inserted by means of a socket (in order to allow the change of chip samples for test) in a Printed Circuit Board (PCB) system. The control of this PCB system is executed by a Field Programmable Gate Array (FPGA).

The communication with the PC is performed by means of a USB Port, whose low level operation is executed by a USB Data Transfer chip. A set of digital isolators have been included between the FPGA and the USB data transfer, in order to avoid malfunctions due to direct connection to the FPGA.

Among many other peripheral devices included, we find an external RAM to store the captured images to be sent later through the USB port, and an external DAC that generates the analog reference voltages for the chip.

The FPGA can be programmed directly via the JTAG connector or programmed at start-up from a configuration flash memory. This FPGA receives the clock via an external clock generator. Several voltage regulators supply the board from the general 5V supply, separating digital and analog supplies.

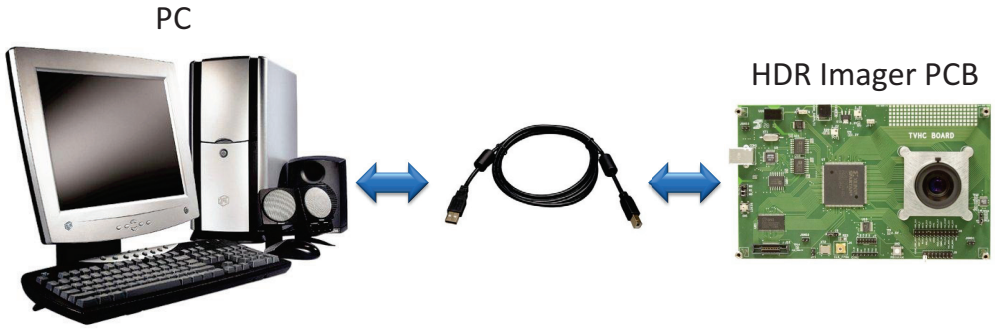

Fig. 1. Control and Acquisition System Scheme.

Fig. 2 shows the block diagram of the PCB and Fig. 3 is a photograph of the board with assembled lens on top of the imager (focus image in sensor plane). The main devices depicted are[1]:

1) **FPGA**: Xilinx Spartan 3 XC3S400 400K System Gates, 288K Block RAM, 56K Distributed RAM Bits, maximum I/O User 141, PQ208 [3].
2) **Imager Chip**: High Dynamic Range Imager under test, 84 JLCC (Lead "J" Shaped).
3) **DAC**: Analog Devices AD7399, Four Rail-to-Rail Channels, Serial-Input 10-Bit DAC [4].
4) **Digital Isolators**: Analog Devices Quad-Channel Digital Isolators with speed CMOS and monolithic air core transformer technology: Analog Devices ADuM1400 and ADuM1402 [5] plus Texas Instrument Hex Inverter SN74LVC04 [6].
5) **SRAM**: Brilliance Semiconductor Inc. (BSI) BS62LV8001 SRAM 1Mx8bit, i.e. 1,048,576 words of 8 bits [7].
6) **USB Data Transfer**: FTDI FT245BL, Single Chip USB Parallel FIFO bi-directional Data Transfer. Maximum data transfer rate to 300Kilobyte/Sec with Virtual Com Port Drivers. Maximum transfer data rate to 1MByte/Sec using FTDI D2XX direct drivers [8].
7) **Analog and Digital Voltage Regulators**: this circuitry generates stable 1.2V, 2.5V and 3.3V for digital supply, and 3.3V for analog supply. These voltages are generated by one Linear Technology LT3021a [9] and two National Semiconductor LM1117 [10]. XP Power IL0505 [11] is also included to allow for supply the general 5V via the USB port.
8) **Configuration Flash Memory**: Xilinx XCF02S 2Mbits Platform Flash In-System Programmable Configuration PROM [12].
9) **JTAG**: a connector which is an interface to download FPGA programming bitstreams into the FPGA.
10) **Clock Generator**: the 50MHz clock signal is generated by a quartz crystal Euroquartz XO91 [13].

[1]Fig. 3 superimposed numbers correspond to item number.

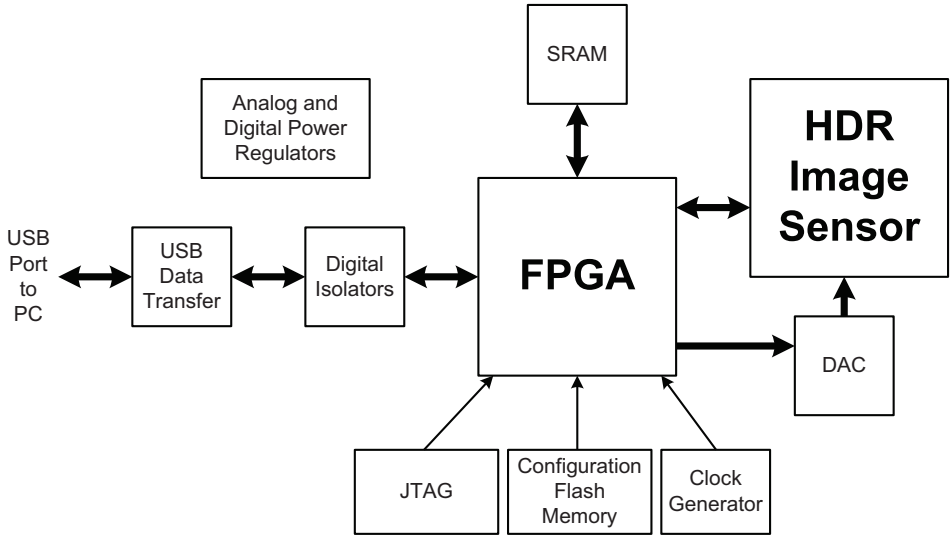

Fig. 2. PCB Block Diagram.

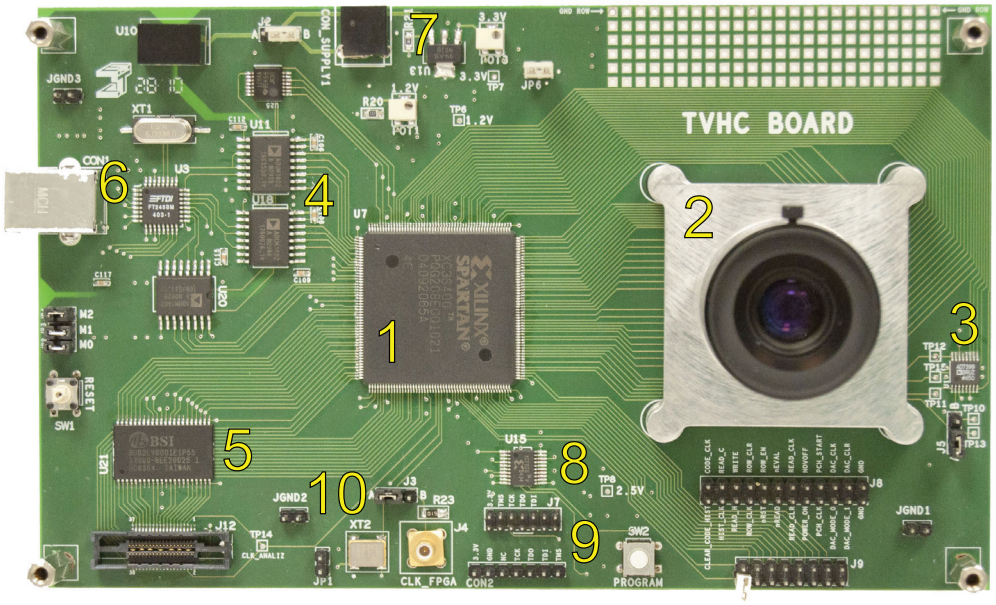

Fig. 3. PCB Photograph.

III. Graphical User Interface

A capture of the Graphical User Interface (GUI) of the software is shown Fig. 4. This interface includes two main tabs: Run and Configuration.

The Run tab contains the representation controls, HDR mode options and capture controls. Its controls are:

- Charts: They represent the statistics of the captured image and the configuration data.
- Image: It represents the image received from the chip after visualization formatting.
- Chart Active: It allows disabling the calculation and representation of statistics in order to increment the frame rate, as software implies the main bottleneck of the system.
- Zoom: It allows the image to expand over the image representation control. However, this leads to artifacts due to the mathematics of the resize operation and therefore it can be disabled for visualization in original size.
- Linear Mode: It sets the chip to work in Low Dynamic Range (LDR) non-compressive mode.
- HDR Mode: It allows choosing between modes of operation.
- HDR Mode Options: It sets the variables for configuring the HDR modes of operation.
- Colormap: It allows choosing different colormaps for the representation of the image.
- Number of Images: It configures the number of images to be received allowing video sequences.
- Receive Images Button: It starts the process of images capture. It changes to red color while the system is busy.

The Configuration tab contains low level configuration values and additional port control:

- Timing Requirements: It sets the timing restrictions and delays, which must be respected in the image operation for proper work.
- Analog References: It sets the values of the analog references of the HDR imager chip, which will be set by the FPGA in the PCB DAC.
- Port Utility: It visualizes the status and correct operation of the communication of the vendor driver with the USB Data Transfer. It also allows individual opening and closing of the port.

Representing images using a gray colormap is usual for monochrome images. However, this will lead to loss of details for human perception due to the characteristics of PC monitor representation (Low Dynamic Range or Low Contrast) combined with the vision system of the viewer (compression toward high illuminations). For the improvement of human perception of details in the represented images, this GUI allows the use of Jet colormap instead of grayscale standard one. The jet colormap performs a rainbow set, which goes from blue assigned to lower values to red in the higher values passing through the colors green, yellow, and orange. The effect of this colormap can be observed in Fig. 5.

IV. Image and Video Capture Operation

The images capture starts when the user clicks in the Receive Images button as the port is already opened at form load. The system will capture the configuration data and format them into a byte stream to be sent through the port. If an error occurs writing or reading to the port, it is reported in a listbox of the Port Utility, in order to allow the user to reopen the port.

Once the configuration is sent, the system waits till receiving a large stream of bytes, which is the image captured by the

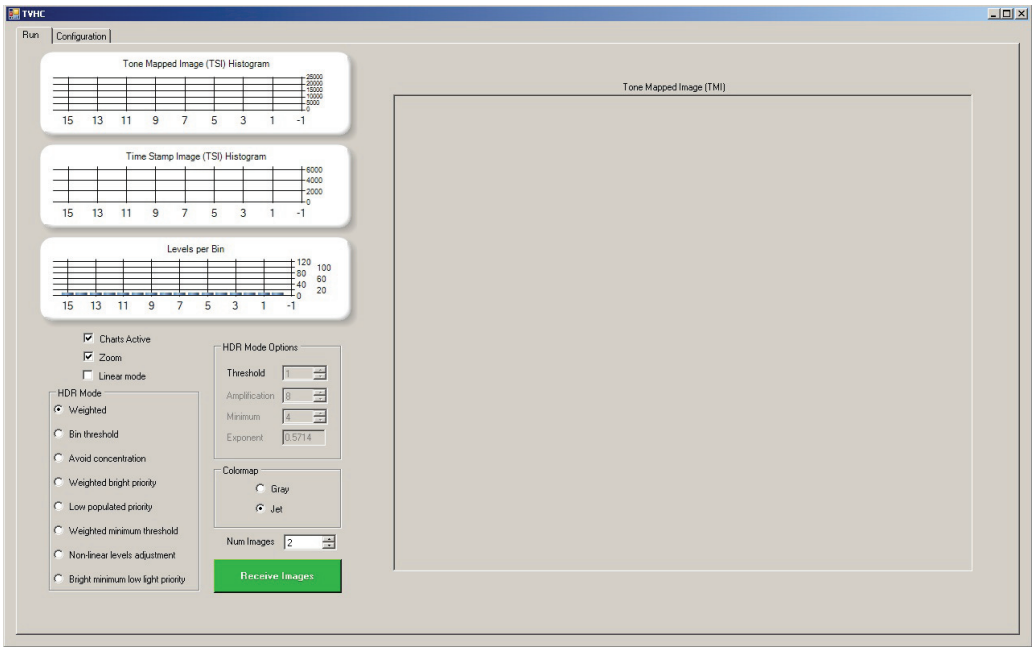

Fig. 4. Graphical User Interface.

chip. This information must be formatted for visualization, such as a flip left to right in order to correspond the captured scene with the visualized one. Later, this information must be loaded in data structures admitted by the controls, in this case a Bitmap array CLI/C++, while linearly adapted to number of levels, such as from 128 levels (7-bits chip output) to 256 levels (8-bit standard representation).

Statistics are calculated over the images, such as the histogram, which are visualized by means of chart controls. The representation controls are refreshed (for proper showing in a loop). From the received data, the configuration for the next acquisition is calculated and sent again to the PC in order to allow for the next frame capture. This process is repeated until the configured number of images have been captured and visualized.

V. Conclusion

It has been developed an acquisition, control and visualization system for a high dynamic range imager. The user-friendly interface and the automation of the capture process introduces a robust and intuitive method for gathering HDR images.

(a) Gray Colormap (b) Jet Colormap

Fig. 5. Effect of colormap in human perception of details in grayscale images.

Future work will involve further enhancement of frame rate minimizing the software computation, such as performing more computation at FPGA level, and/or taking advantage of PC multi-threading capabilities.

Acknowledgment

This work is partially funded by TEC2009-11812, CENIT ADAPTA, ONR Grant N000141110312, FEDER 2007-2013, WiVisNet, PIMA and spanish Project INNPACTO IPT-2011-1625-430000.

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