Introduction to the Special Issue on the 36th European Solid-State Circuits Conference (ESSCIRC)

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I. INTRODUCTION

THIS special issue includes 22 papers selected from some 114 presented at the 2010 European Solid-State Circuits Conference (ESSCIRC). The conference was jointly organized with the European Solid-State Device Research Conference and held September 14–16 in Seville, Spain.

ESSCIRC got 265 submissions from 34 different countries; 55.8% of the papers came from IEEE Region 8, while the rest came from the other IEEE regions. Paper selection for the special issue was based on: 1) the feedback of the audience; 2) the feedback of the session chairs; and 3) the scores given by the ESSCIRC TPC members. Selected papers were invited to submit extended versions on early October 2010. All papers were peer reviewed and most papers got four reviews.

Papers in the issue covers the traditional ESSCIRC topics of analog circuits, digital circuits, data converters, sensors and imagers, and communications and RF circuits. Energy harvesting and biomedical circuits were also within ESSCIRC 2010 topics and are represented in this issue. The papers are briefly introduced in Sections II–V.

II. ANALOG AND DATA CONVERTERS

This section starts with a paper about analog filters. Thyagarajan *et al.* address the sensitiveness of Gm-C filters to parasitic capacitances. They combine Gm-C and active-RC integrators to enhance linearity and speed with negligible noise or power dissipation penalty. Up to 40 dB reduction in the third order intermodulation distortion is reported for a 20MHz bandwidth, fifth order Chebyshev filter in a 0.18 m CMOS process.

The next two papers in the analog subsection addresses challenges related to wireless sensor networks. Both report silicon results in 65 nm CMOS processes. Fan *et al.* present an instrumentation amplifier which consumes 1.8 A from a 1V supply to achieve 1 V offset, 0.16% gain inaccuracy, 134 dB CMRR, 120 dB PSRR and a noise efficiency factor of 3.3. They employ a positive feedback loop to boost the input impedance and incorporate a ripple reduction loop to suppress the chopping ripple. Sebastiano *et al.* present an oscillator whose frequency is set by the electron mobility in a MOS transistor. The chip dissipates 51 Wat 150 kHz. After two-point trim, its frequency spread is less than 0.5% within the 55 C to 125 C temperature range. A current-controlled class-D audio amplifier is then presented by Torres *et al.*. The proposed amplifier achieves a 90 dB SNR over the entire audio band and a total harmonic distortion plus noise as low as 0.02%. The output power is 410 mWwith a 84% peak efficiency.

The subsection on data converters includes results from two 65 nm CMOS silicon prototypes (corresponding to one oversampled ADC and one pipeline ADC) and from one 90 nm CMOS prototype of a successive approximation converter. The oversampled converter, by Prefasi *et al.*, employs a time-encoding quantizer embedded in a continuous-time third-order SD loop. Clocked at 2.5 GHz, the complete ADC consumes 7 mW from a 1.0 V supply to feature a peak-SNDR of 61 dB over a 20 MHz signal bandwidth. The pipeline data converter, by Sundström *et al.*, employs fast open-loop current-mode

amplifiers to achieve a sampling rate of 2.4 GS/s while dissipating 318 mW in the analog core. At the maximum rate the measured SNDR remains above 30.1 dB within the whole Nyquist band. The 90 nm SAR ADC presented by Harpe *et al.* achieves ultra low-power dissipation by using custom-designed 0.5 fF unit capacitors and asynchronous dynamic logic. The circuit dissipates 26.3 W from a 1 V supply to achieve an ENOB of 7.77 bit at a sampling frequency of 10.24 MS/s.

III. RF AND COMMUNICATIONS

The RF subsection starts with an outphasing power amplifiers by Xu *et al.* The presented class-D PA achieves 25.3 dBm output power and is realized in a 32 nm CMOS process. Outphasing combining is here performed via an integrated transformer. Next a low phase noise 65 nm CMOS PLL for 802.15.3c in the 48 GHz band is discussed by Murphy *et al.*. Using a programmable transmission line concept, the PLL achieves a -97.5 dBc/Hz@1 MHz across the entire band meanwhile having more than 22% tuning range. A high performance VCO targeting cellular applications is presented next by Andreani *et al.* The phase noise at 20 MHz offset from a 3.7 GHz carrier is 156 dBc/Hz, meeting the requirement for GSM/EDGE and SAW-less WCDMA transmitter after frequency division by 2 or by 4. The VCO has been realized in an RF 90 nm CMOS technology.
The communication subsection starts with a low data rate FM-UWB transmitter in 90 nm CMOS by Saputra and Long. The energy efficient implementation of the front end using a current controlled oscillator and class-AB power amplifier consumes only 900 W while running continuously at 100 kbits/s. Soldà *et al.* present an IR-UWB transceiver front end in 130 nm CMOS. The achieved sensitivity is 87 dBm at a pulse rate frequency (PRF) of 100 KHz and 70 dBm at a PRF of 5 MHz, while consuming 4.2 mW. The receiver can tolerate interferers up to 12 dBm at 5.4 GHz. A fully integrated 130 nm CMOS 2x2 MIMO tri-band dual mode transceiver is presented by Lim *et al.* By careful LO frequency planning the transceiver chip operates in the fixed and mobile frequency bands of WiMAX and WLAN. The proposed solution reduced the RF interface to only 4 RF pins. This section concludes with a 0.4–6 GHz 40 nm CMOS receiver by Borremans *et al.* The software defined receiver achieves a 3 dB NF and tolerates 0 dBm blockers, achieved using a mixer based high-Q integrated RF filter.

IV. SENSORS, BIOMEDICAL APPLICATIONS AND ENERGY HARVESTING

This section starts with a paper about 3D imagers. Perenzoni *et al.* present one of the first implementations of a CMOS ToF sensor with correction circuitry embedded at pixel level for reset noise removal and fixed-pattern noise reduction. A 160x120 0.18 m CMOS chip biased with 175 mA from a 1.8 V supply is reported and demonstrated for distance measurement up to 4.5 m with precision of 10 cm at 1 m at 55 Fps. The other two papers in the sensor subsection report chips in 0.35 m and 0.16 m CMOS processes respectively. Aaltonen *et al.* present a complete analog front-end for a MEMs gyroscope in 0.35 m CMOS. No external active electronics is required and the reported ASIC embeds all required functions. The noise floors of the two sensors are 0.028 /s/pHz for z-axis and 0.032 /s/pHz for y-axis. The chip draws 2.2 mA from a 3V supply. Souri and Makinwa present an accurate 0.16 m CMOS smart temperature sensor for RFID applications. The architecture employs a zoom ADC which combines coarse SAR conversion with fine SD conversion for energy efficiency. After a single trim at 30 C, the sensor achieves an inaccuracy of +/-0.2 C (3δ) from 30 C to 125 C with a power dissipation of 7.4 μW.

In the area of circuits for biomedical applications, the paper by Liu *et al.* presents a stimulator for use with implanted nerve tripoles. The paper reports a two-channel stimulator implemented in a 0.6- m silicon-on-insulator CMOS process. This stimulator uses high-frequency current switching (HFCS) for safety purposes. The current generator consists of a 4-bit coarse amplitude section with 100 μA steps and a 4-bit differential adjustment section with 6.25 μA steps. The output stage achieves a charge efficiency of about 90% for a 1 kΩ load.

In the area of power conversion, van Breussegem *et al.*, presented a fully integrated capacitive stepdown DC-DC converter in 90 nm CMOS. TheDC-DC converter is controlled by a Single Boundary Multiphase Control (SBMC) without compromising the control loop bandwidth. The converter has an output power capability of 150 mW, a peak efficiency of 77% and a full load efficiency of 74%. Reinisch *et al.* present an energy harvesting RF to DC power conversion system to power up wireless sensor nodes. The system has been developed in a 0.13 m low-cost CMOS technology. Their wireless sensor node includes an on chip temperature sensor and a bulk acoustic wave (BAW)-based transmitter with a maximum output power of 5.4 dBm. The chip consumes only 190 nW in idle mode.

V. DIGITAL

This section presents two VLSI platforms with unique distinct goals: extreme low power, and very high computing performance. The first paper, by Kwong *et al.*, presents a flexible, energy-efficient processor for medical monitoring devices. This platform features accelerators for signal processing to reduce both cycle count and energy consumption. Voltage scaling and block-level power gating was used to optimize energy efficiency under applications of varying complexity. The paper further reports a 10.2x energy reduction on a complete EEG application, and a 11.5x energy reduction on an EKG, using both CPU and accelerators, when compared to CPU-only implementations. Multiple-input multiple-output (MIMO) technology is the key to meet the demands for data rate and link reliability of modernwireless communication systems, such as IEEE 802.11n or 3GPP-LTE. Struder *et al.* describe in their paper the first ASIC implementation of a SISO detector for iterative MIMO decoding. This implementation uses a lowcomplexityminimum mean-squared error (MMSE) based parallel interference cancellation algorithm. The CMOS 90 nm chip exceeds the 600 Mb/s peak data-rate of IEEE 802.11n.

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