Design Considerations for an Automotive Sensor Interface ΣΔ Modulator

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ABSTRACT

In this paper we discuss design considerations for a Sigma-Delta modulator (ΣΔM) forming part of a sensor interface for automotive applications. This ΣΔM contains a programmable-gain input interface to accommodate the output signal level of a variety of automotive sensors. We show that this characteristic can be efficiently implemented by proper architecture selection and ad hoc sampling and integration capacitor structures. Behavioral simulations of a 17bit 40kS/s modulators are included to illustrate the design considerations.

1. INTRODUCTION

In modern automotive industry, sensors and ICs are more and more interrelated. On-chip or on-package low-cost smart sensors proliferate in our cars and forecasts are that both the market and the number of applications will grow in coming years [1]-[3]. From the designers' point of view, this market trend is synonym for new design challenges: ever more accurate and reliable analog-to-digital (A/D) interfaces are required under the hostile environmental conditions in the sensor's neighborhood (high temperatures, electromagnetic interferences, etc.).

The need for high-resolution interfaces is derived from the typically weak sensor output signals (ranging from μVs to hundreds of mVs). Because of this, a very low-noise high-gain stage is normally the first block in a sensor front-end [4][5]. In some multi-purpose applications, this preamplifier has a switchable gain to accommodate different signal levels [4]. Once the sensor signal has been boosted to workable levels, an A/D converter digitizes it and the rest of processing is carried out in the digital domain. To this purpose, oversampled ΣΔ converters have gained ground recently [4]-[12], the reasons being diverse: First, they are best suited for the low-, moderate-frequency context, where a large oversampling ratio contributes to reinforce the a priori superiority of the ΣΔM concept (reduced and robust analog content). Second, in some applications, the principle of the sensing devices fits in with the topology of the ΣΔM, thus allowing partial or total integration of the sensor in the converter structure [8][10][11]. Furthermore, the specificities of the ΣΔM enable especial signal processing that has been exploited in sensor interfaces [6][12].

This paper focuses on the first part of this rationale to present design consideration applicable to a high-resolution ΣΔM for sensor interfaces. For a better fitting to the characteristics of different sensor outputs, the ΣΔM here includes gain programmability, so that the front-end gain is distributed between the preamplifier and the input stage of the ΣΔM.

2. CIRCUIT LIMITATIONS

The in-band error power of whatever ΣΔM (in the end, the factor that limits the performance) can be expressed as the summation of the contributions due to several error mechanisms,

$$P_{\text{in-band}} \cong P_Q + P_{cn} + P_{nl} + P_{st} \tag{1}$$

where right-hand side terms stand for quantization error, circuit noise, non-linearity error, and defective settling error powers, respectively. Each of these error powers can be controlled by manipulating some design parameters: for instance, P_Q is basically a function of three design parameters: the modulator order (L), the oversampling ratio (M), and the number of bits in the internal quantizer (B):

$$P_Q \sim \frac{1}{12}\left[\frac{2V_{ref}}{(2^B-1)}\right]^2 \frac{\pi^{(2L)}}{(2L+1)\cdot M^{(2L+1)}} \tag{2}$$

Although, depending on the modulator type, the basic P_Q can be altered by circuit imperfections, the most important impact of such circuit imperfections is to be found in the remaining contributions in (1). For modest performance, the circuit requirements to render $P_{cn} + P_{nl} + P_{st} \ll P_Q$ are not demanding. However, this is not the case for really challenging specifications, when the achievement of either very large resolution or speed (sometimes both) force designers to work on the edge of feasibility. In these designs, the quantization error usually plays a secondary role. Although not included in (1), switching noise is gaining ground as one of the most limiting factors, especially for high-frequency converters [13].

For obvious reasons, out of the circuit imperfections above, dynamic limitations are not an issue in low-frequency sensor applications. On the contrary, circuit noise contribute 90% of the in-band error power in a typical design, thus deserving especial attention in this section. Consider the two-branch SC integrator in Fig.1 in which we assume that

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the signal sampling capacitor, C_{11}, can be different from the feedback sampling capacitor, C_{12}, in order to create a modulator input-output gain $\xi = C_{11}/C_{12}$. In this circuit the noise contributors are the OTA (white + flicker noise) and the switch on-resistance (thermal noise). Also, potential noise coming from the reference voltage generation block must be accounted for, which overall will be a mixture of white and flicker noise. Whereas flicker noise can be very efficiently removed from the signal band by applying chopper techniques [4][5] for example, the low-frequency white noise power spectral density (PSD) is boosted by the well-known aliasing mechanism: due to dynamic requirements, the equivalent noise bandwidths for these contributions are well in excess of half the sampling frequency, thus provoking aliasing of their PSD. A careful analysis shows that the input-equivalent white noise PSD per fully-differential branch can be approximated (at low frequencies) by,

$$S_{in,C_{11}}(f) \cong \frac{4kT}{C_{11}f_s} + \frac{4kT(1+n_t)}{3C_{eq,i}f_s}$$
$$S_{in,C_{12}}(f) \cong \frac{4kT}{C_{12}f_s} + \frac{4kT(1+n_t)}{3C_{eq,i}f_s} + \frac{kT}{C_{12}f_s}\cdot\frac{R_{eq,ref}}{2R_{on}} \quad (3)$$

where k is the Boltzman constant and T is the absolute temperature. The first term corresponds to the contribution of all the switches in each branch, the second one is for the OTA contribution, where

$$C_{eq,i} = C_p + C_{12}(1+\xi) + C_l\left[1 + \frac{C_p + C_{12}(1+\xi)}{C_2}\right] \quad (4)$$

is the OTA equivalent load during the integration phase (ϕ_2 high). In estimating the white noise PSD of the OTA the contributions of MOS devices other than the input ones are compiled in the factor n_t, which equals the summation of the respective transconductance ratios. The third term in $S_{in,C_{12}}$ represents the noise coming from the reference voltages ($R_{eq,ref}$ being its equivalent noise resistance).

By neglecting contributions other than the first integrator's, the ΣΔM output white noise power is obtained: (5)

$$P_{wn} \cong \frac{4kT}{MC_{12}}(1+\xi) + \frac{4kT(1+n_t)}{3MC_{eq,i}}(1+\xi)^2 + \frac{kT}{MC_{12}}\frac{R_{eq,ref}}{2R_{on}\xi^2}$$

where the OTA noise contributions in (3) have been considered fully correlated because it is the same circuitry and its noise is sampled at the same instant. From this point, some recommendations can be made for the design of a high-resolution ΣΔM: (a) For given M and ξ, choose the feedback sampling capacitor, C_{12}, large enough to make the first term in (5) smaller than the maximum allowed in-band error power. (b) The previous recommendation assumes that second and third contributions in (5) are less important, which requires that both the OTA and switch dynamic performances are not oversized.

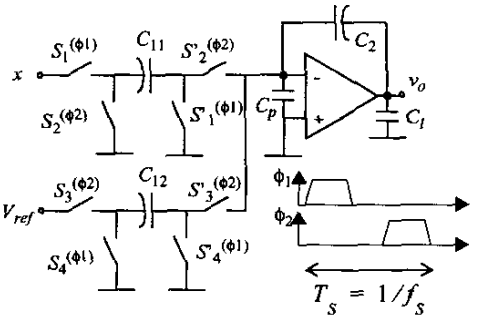


Figure 1. Two-branch SC integrator and clock phases

Another fact clearly visible in (5) is that the output white noise power depends on the ΣΔM gain, ξ. The first two terms increase with ξ, while the third one decreases. The overall trend for P_{wn} is to increase with ξ. Also, as (4) shows, the OTA equivalent load increases with ξ, thus requiring more demanding dynamics and, hence, dissipating more power. The immediate conclusion is that the ΣΔM gain should be as close as possible to unity. In fact, if $\xi = 1$ the second branch in Fig.1 is not necessary thus reducing even more P_{wn} and, consequently, $C_{eq,i}$. This choice, commonly found in literature [4], puts the ball back into the preamplifier's court, rendering its design more complicate and the overall programmability less flexible.

3. ARCHITECTURE SELECTION

In a first step, selecting a ΣΔM architecture consists of assigning values to the three main parameters: oversampling ratio (M), loop order (L), and internal quantizer resolution (B). Out of these, increasing the oversampling ratio has been the most popular resort for augmenting the modulator resolution, the reason being twofold: On the one hand M has a clear, beneficial impact on P_Q in (2). On the other, while changing M basically alters the dynamic requirements of the building blocks, augmenting L and/or B also raises issues at the modulator level, jeopardizing loop stability and/or degrading robustness. Furthermore, given the distinct impact of M in P_Q and, say, P_{wn} – compare eqs. (2) and (5), as the oversampling ratio increases there will a value for which $P_Q \cong P_{wn}$. In order to illustrate this, Fig.2 shows the effective resolution measured from three ΣΔMs (4th-order 3bit, 3rd-order 1bit, and 2nd-order 1bit, all of them with the same front-end integrator) as a function of the oversampling ratio. Differences among curves are justified by the different modulator orders and the fact one of them is multi-bit. However, note that in each curve there is a change in the slope which coincides with the point beyond which the in-band error power is dominated by the first integrator white noise, and quantization error is not an issue any more. This is the reason why the three curves converge for sufficiently high M. Once in this region, doubling M generates a mere 3dB decrease in error power

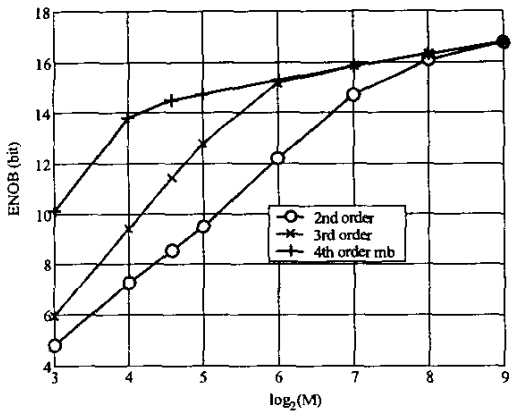


Figure 2. Effective resolution vs. oversampling ratio

(i.e., 0.5-bit increase in effective resolution). In Fig.2, the only way to shift up the white-noise-limited region is to increase the value of the sampling capacitors. Our experience and other design evidences in the open literature show that efficient ΣΔMs are those located slightly inside this region: that is, with some equilibrium between P_Q and circuit-derived error power. Intuitively, this is due to the following rationale: (a) if for the oversampling ratio selected, P_Q clearly dominates the in-band error power (design located at the high-slope region of the curves in Fig.2), the building block specifications are bound to be oversized; (b) otherwise, (for design located deep in the low-slope regions), probably L or B (or both) could have been reduced without significant impact on resolution.

Contrary to high-frequency applications (e.g., communications), in sensor applications we can take maximum advantage of the maneuverability of M, making use of a highly-oversampled ΣΔM to fulfill the high-resolution requirements. This will push our design to the right in Fig.2, so that a high-order and/or multi-bit architectures seem to be impractical. However, note that, if for a certain low-frequency application, the resolution does not have to be that high, thus requiring less oversampling, it will be sensible to try higher-order and/or multi-bit solutions, as the equilibrium point between quantization error and circuit error moves to the left in Fig.2.

In order to quantitatively evaluate these qualitative considerations, an approximate procedure can be implemented making use of the equations in the previous sections to estimate the implementation cost of different architectures. For the sake of brevity, we will only sketch the main steps:

- For given values of L, M, B, V_{ref} and ξ, calculate P_Q and select C_{12} so that $P_Q + P_{wn}$ is smaller than the maximum allowed in-band error power.
- Estimate $C_{eq,i}$ from (4). Then, a linear settling model with settling constant $C_{eq,i}/g_m$ can be used to estimate the OTA transconductance required, since it takes a number $\ln(2^{ENOB})$ of time constants to settle within *ENOB* resolution.
- Relate the OTA g_m with the OTA power dissipation, for which the candidate OTA topology must be known a priori. A suitable selection is extremely linked to the fabrication process: supply voltage, minimal device length, etc. Sensible choices are a folded-cascode OTA up to 3-V supply, and a two-stage amplifier for 2.5V and beyond.
- Once the first integrator power dissipation is known, that of the remaining integrators (in practice with less demanding specifications) can be estimated as a fraction of it. The overall static power of the modulator is then obtained by adding up all the contributions.

Of course, fine-tuning of this procedure is required for more realistic estimations, including the impact of other non-ideal effects (such as finite and non-linear OTA DC-gain, slew-rate, errors in the multi-bit quantizers, etc.), power dissipation in other blocks, as well as the dynamic power dissipation [14]. In addition, the power dissipation and silicon area of the required decimation filter must be included in the trade-off towards architecture selection.

4. DESIGN EXAMPLE

The previous design considerations are applied in this section to the design of a 17-bit effective resolution, 40-kS/s, ΣΔM for an automotive sensor interface requiring signal-to-(noise + distortion) ratio (*SNDR*) > 100dB. The intended technology is a 3.3-V 0.35μm CMOS, with M-i-M capacitors available. The architecture selection procedure sketched above led us to the third order 2-1 cascade ΣΔM shown in Fig.3, with 128 oversampling ratio. This topology has been preferred to a 2nd-order modulator, a prori more efficient, because the latter requires $M = 512$, i.e. the 20.5-MHz sampling frequency, – discarded for switching noise considerations.

Fig.4 shows the first SC integrator, where the input-output gain programmability ($\xi = 0.5, 1, 2$, and 4 in this example) has been mapped onto switchable capacitor arrays, each of

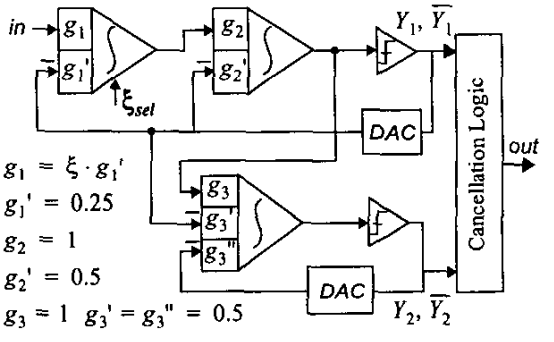
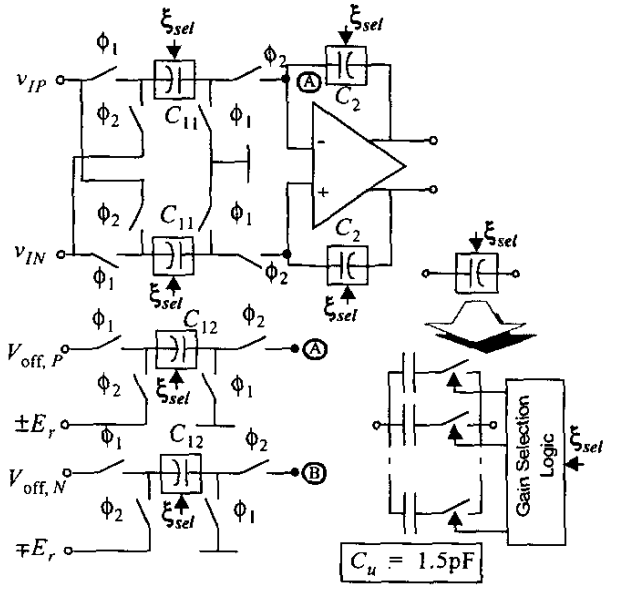


Figure 3. 4th-order 2-1 cascade ΣΔM with embedded gain

them formed by a variable number of unitary capacitors. Such numbers and the unitary value (also shown in Fig.4) are selected for minimum power dissipation, bearing in mind the circuit noise limitation and the high junction temperature required for this interface, 175C. The first integrator contains two differential input branches: one of them is for the sensor signal, in which double sampling is used to achieve an extra signal gain of 2, without increasing circuit noise. The second branch receives the DAC outputs. Making use of the spare connection of the second branch, an external DC signal (V_{off}) can be applied during ϕ_1 to center the sensor signal in the modulator full-scale range. Note that, when ξ changes, not only the value of C_{11} is varied but also those of C_{12} and C_2. In this procedure the OTA equivalent load is minimized (and its dynamics relaxed) while the value of g_1' is kept, which guarantees that the rest of the modulator topology does not need to be changed. Furthermore, by manipulating the tail current of the first OTA, the estimated power dissipation of the complete ΣΔM (tabulated in Fig.4) adjusts to the specific application.

After architecture selection, the modulator specifications have been mapped onto building-block specifications using statistical optimization for design parameter selection, and compiled equations (capturing non-ideal building-block behavior) for evaluation. This process is fine-tuned by time-domain behavioral simulation (using ASIDES). Fig.5 shows the *SNDR* obtained through behavioral simulation. The *SNDR* peak, which moves to the left as ξ increases, is always over 100dB.



ξ	C_{11}	C_{12}	C_2	OTA g_m	ΣΔM Pw.
0.5	C_u	$4C_u$	$16C_u$	1.4mA/V	8.8mW
1	$2C_u$	$4C_u$	$16C_u$	1.6mA/V	9.7mW
2	$6C_u$	$6C_u$	$24C_u$	2.8mA/V	16.0mW
4	$16C_u$	$8C_u$	$32C_u$	5.2mA/V	27.5mW

Figure 4. Switchable-weight SC integrator details

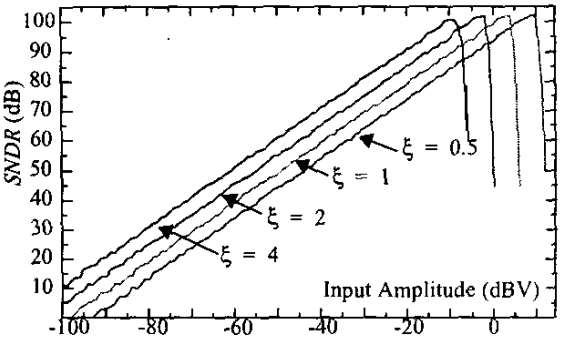


Figure 5. Simulated *SNDR* vs input amplitude

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