A CMOS Fully-Differential BandPass ΣΔ Modulator Using Switched-Current Circuits

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Abstract

This paper presents a fourth-order bandpass sigma-delta modulator that has been designed using fully-differential switched-current circuits in a 0.8μm CMOS technology. The modulator prototype has been obtained by applying a lowpass to bandpass transformation (z^{-1}->$-z^{-2}$) to a second-order lowpass ΣΔ modulator. Specifications are SNR≥60dB@2.5Mhz±15Khz, for a clock frequency of 10Mhz. Preliminary results from the fabricated prototype obtains the correct noise shaping up to 2.5Mhz clock frequency.

I. INTRODUCTION

Bandpass oversampled ΣΔ converters are very convenient for the front-end of modern narrow-band communication systems [1-3]. Similar to lowpass, bandpass ΣΔ converters use oversampling and feedback of the quantization noise to exchange operation speed for resolution and thus increase robustness against unavoidable hardware parasitics and tolerances.

Realizations of bandpass ΣΔ modulators using *continuous-time* circuits with off-chip LC resonators [4] and monolithic discrete-time *switched-capacitor* (SC) circuits [5-7] have been reported. These latter prototypes featured center frequencies in the range of 455kHz to 10.7MHz, bandwidths in the range of 10Khz to 200Khz, and resolutions in the range of 9 to 14bit, in BiCMOS [7] or double-poly CMOS technology [5-6]. However, since standard CMOS have only one poly layer it may be worth exploring the use of *switched-currents* (SI), which require only MOS transistors as design primitives [8]. Besides, these techniques show promise for higher operation speed than switched-capacitors [9], although this is a rather controversial issue. Some preliminary results in this direction have been presented recently in [10].

This paper presents the architecture and implementation of an SI 4th-order bandpass ΣΔ converter in a 0.8μm CMOS digital technology. The prototype occupies 1.2x1.4 mm^2 silicon area and the simulation results foresee 11.6 bit resolution for a signal of 2.5 Mhz ± 15 Khz with 10Mhz sampling frequency.

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II. Architecture of the Modulator

Fig. 1 shows the architecture chosen for the modulator, determined from a second-order lowpass prototype using the transformation z^{-1}->$-z^{-2}$ [5]. This transformation maintains the stability properties of the lowpass prototype, whose practical use has been demonstrated in both SC and SI implementations [11]. Assuming that the 1 bit quantizer in Fig.1 can be modelled as an additional noise source with *k* effective gain, the modulator output is given as,

$$Y(z) = z^{-2}X(z) + (1+z^{-2})^2 E(z) \qquad (1)$$

where *X(z)* is the modulator input signal, *Y(z)* is the modulator output, and *E(z)* is the additional quantization noise source in the linear model. The transfer function of the input is a double-delay and the transfer function of the quantization noise has two transmission zeros in $f_S/4$. This is the equivalent of the two zeros in DC of the lowpass prototype.

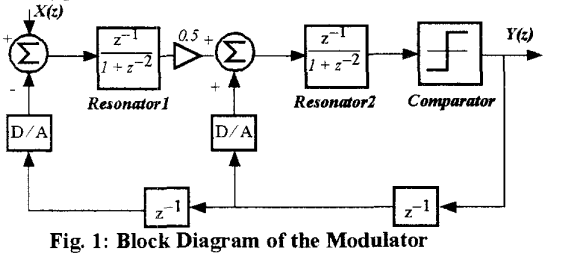

Fig. 1: Block Diagram of the Modulator

Fig.2 presents the simulation results of the proposed architecture obtained using *ASIDES* [12], a simulator of the behavior level of ΣΔ modulators. Fig. 2a shows an *FFT* of the modulator output for a sinusoidal input of -6dB range centered on 2.5 Mhz to a clock frequency of 10Mhz. The coefficient *0.5* offers a similar dynamic range in the output of both resonators as shown in the histogram of Fig. 2b; thus their design can be identical.

III. Design of the modulator blocks

A. Resonator SI

The resonator block has been implemented using a

cascade of two *backward-Euler* integrator blocks with *biquad* feedback [7] as shown in Fig 3. Making $A=B=\pm 1$ and $R=2$, obtains the desired transfer function. This structure has been chosen from others by stability reasons, since its poles remain in the circle unit upon changes in the R coefficient.

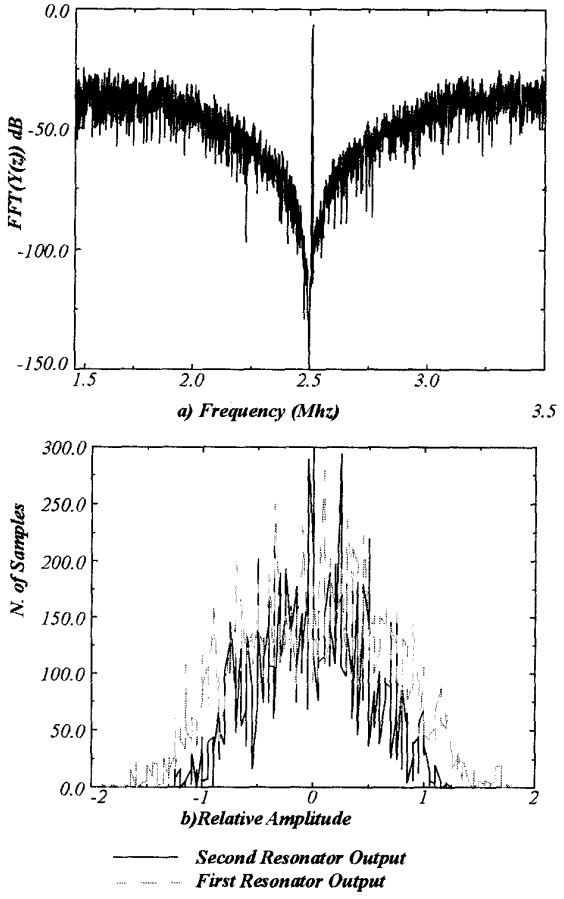

Fig. 2: Behavior Simulations of the Modulator

The implementation of the integrator with SI techniques is shown in Fig. 4. For maximum reduction of errors, we used a fully-differential regulated folded cascode structure [13]. The local feedback of this cell increases the input conductance and the differential structure allows first-order cancellation of the clock *feedthrough*. The common mode feedback *CMFB* stage is shown as the thickest line. Delay versions have been used for the clock phases that control the steering switches. At the same time, minimal dummy transistors were used in the memory switches.

The gain A is performed by scaling the memory transistors at the integrator output stage. Consequently, the coefficient R is realized by adding an additional output stage to the second integrator with *-2* gain as show schematically in Fig. 5.

The gain A is performed by scaling the memory

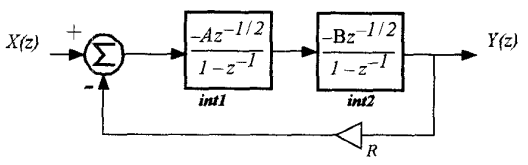

Fig. 3: Block Diagram of Resonator

transistors at the integrator output stage. Consequently, the coefficient R is realized by adding an additional output stage to the second integrator with *-2* gain as show schematically in Fig. 5.

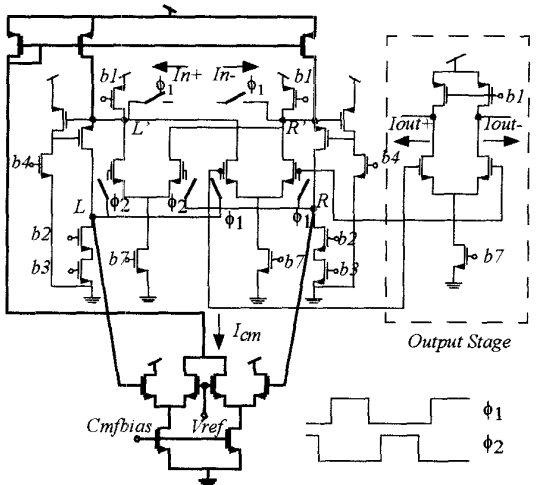

Fig. 4: Regulated Folded-Cascode Integrator with CMFB

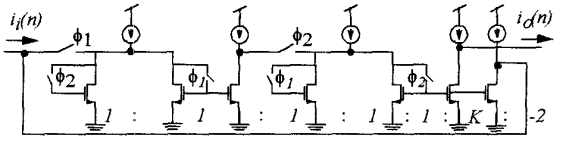

Fig. 5: Simplified Schematic of the SI Resonator.

B. 1-bit D/A Converter

Fig. 6 shows a schematic of the 1-bit D/A converter used, consisting of a current source controlled by the comparator output [11]. The type of current source used has been chosen so that it resembles the structure of the cell memory. The two output currents change the flow direction depending on the comparator output. A small *offset* is no serious problem for the modulator. *Pmos* switches are used due to the input voltage range required in the integrators.

C. 1-bit Quantizer

Fig. 7 shows the quantizer block diagram, made up of a regenerative *latch* [15] and an RS flip-flop that maintains

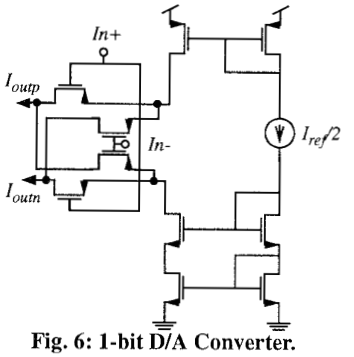

Fig. 6: 1-bit D/A Converter.

the output value in the phase ϕ_1, which is the phase where the phase where the resonators are feedback.

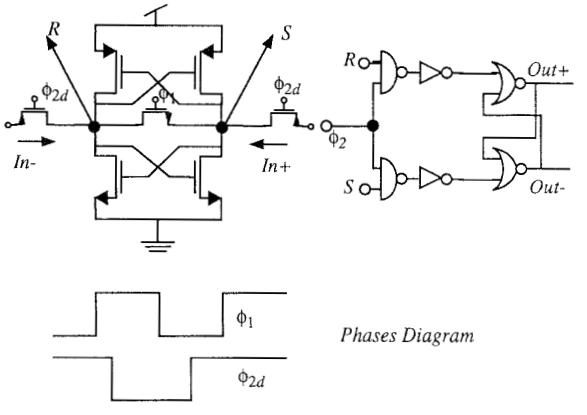

Fig. 7: Block diagram of the Current Quantizer

The regenerative *latch* operates as follows: the input currents are sampled in the complementary ϕ_{2d} phase since the switches are *pmos*, developing a small difference voltage through the *nmos* switch. When the *nmos* switch opens, the current which flows through this switch cuts off abruptly, and the *latch* impedance changes from positive to negative (positive feedback). Consequently, depending on the sign of the small difference of stored voltage, the *latch* output nodes (*R* and *S*) will go to the positive or negative rail. A quick comparison is thus obtained with low input current levels.

IV. Simulation Results

This section presents some results of the electrical simulation obtained throughout the design. Fig.8 shows several simulations made of the modulator blocks using *HSPICE*. Fig. 8a shows an analysis in AC of the cell memory, it presents 50 Mhz bandwidth. Transient simulation of this cell in the storage phase is shown in Fig. 8b, *v(out)* is the gate voltage of the memory transistor, Fig. 8c shows the time response of the integrator to a sinusoidal input of 5μA range and 1Mhz when sampled to 10Mhz. Finally, Fig. 8d shows a simulation of the time response of the Resonator block when it is excited by an impulse signal of 10μA range. The Resonator output should repeat the values in the ranges 10μA, 0, -10μA, 0 periodically. Since

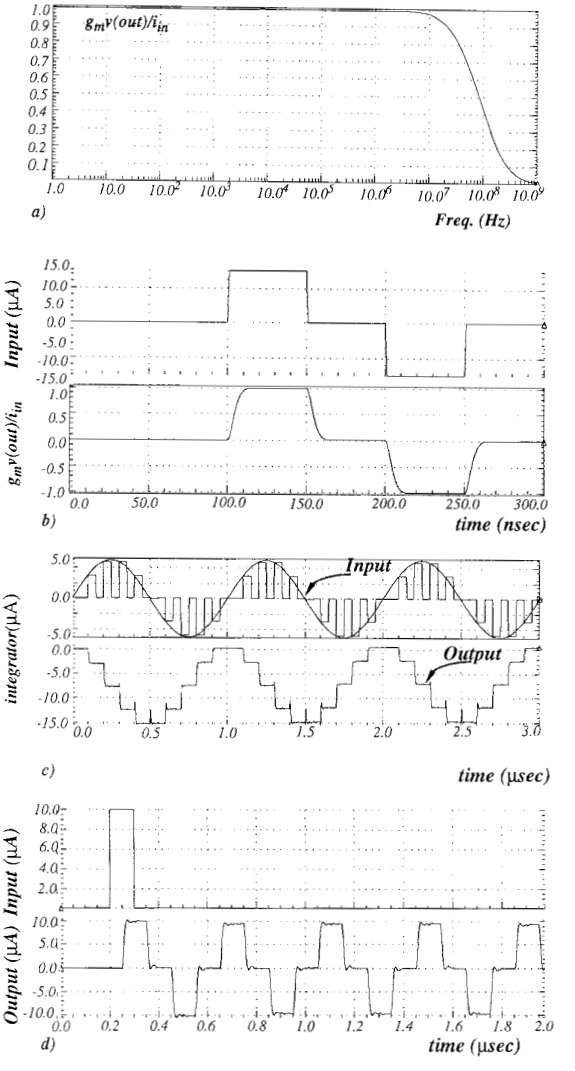

Fig. 8: HSPICE Simulations of the Memory Cell and Resonator.

there are loss coefficients, the output range value attenuates.

Fig. 9 shows simulation of the *SNR* regarding the input range, taking into account the distinct non-linearities appearing in SI circuits. These have been measured using *HSPICE* and introduced in the *ASIDES* models for the modulator blocks. The values of these errors are: finite conductance ratio error e_g=*0.04%*, settling error e_s=*0.27%*, and load injection error e_q=*0.23%*. A variation of 1.0% in the value of *R* has also been considered.

V. Conclusions

An SI bandpass ΣΔ modulator has been designed up to a *layout* level in a CMOS 0.8μm technology of AMS. The arquitecture is based in a second order lowpass prototype using the transformation z^{-1}->-z^{-2}. The SI cell memory used are fully differential regulated cascode to minimize the

errors. The predicted resolution is of 11.6 bits for a sampling frequency of 10Mhz applied to a signal centered on 2.5Mhz with a bandwidth of 30Khz. Fig. 11 shows the entire *Layout* of the circuit, including the pads with an area of 1.2x1.4mm^2. In addition to the modulator, a clock phase generator and a *single-ended* V-I to differential converter have been included to ease testing, as shown in Fig. 10. A preliminary experimental result from the fabricated prototype is shown in Fig. 12. This spectrum corresponds to the output of the bandpass modulator with 2.5Mhz of clock frequency and a -8.2 dB sinusoidal input.The functionality of the SI bandpass is demonstrated, and better resolution and frequency are expected.

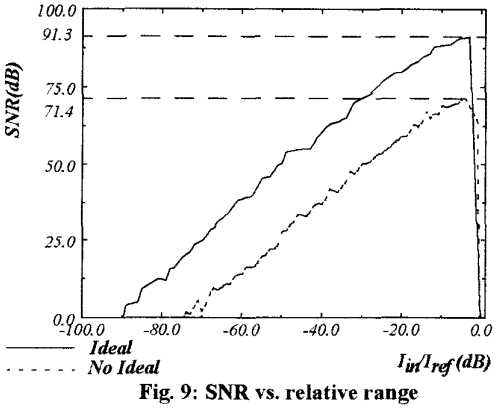

Fig. 9: SNR vs. relative range

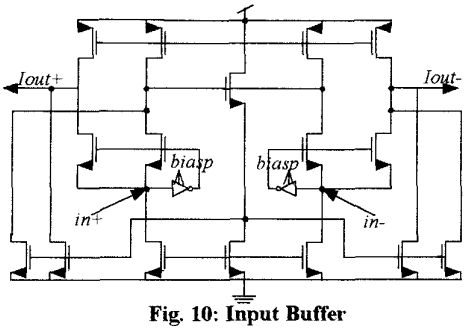

Fig. 10: Input Buffer

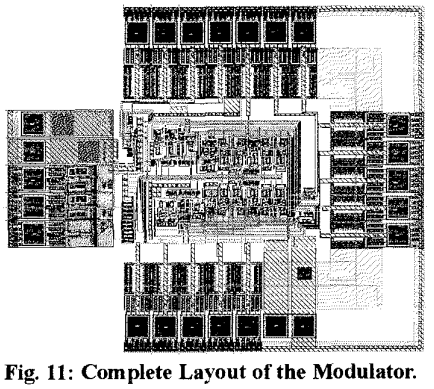

Fig. 11: Complete Layout of the Modulator.

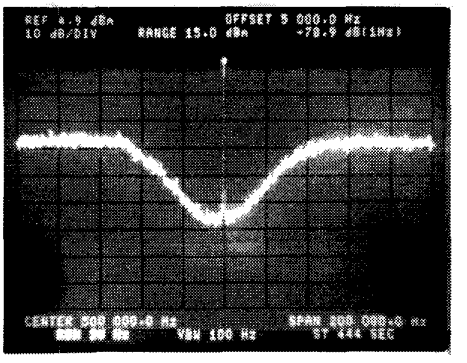

Fig. 12: Preliminary Experimental Result.

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