EFFECT OF NON-LINEAR SETTLING ERROR ON THE HARMONIC DISTORTION OF FULLY-DIFFERENTIAL SWITCHED-CURRENT BANDPASS ΣΔ MODULATORS

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ABSTRACT

This paper presents a detailed study of the effect of the non-linear settling on the harmonic distortion of BandPass ΣΔ Modulators (BP-ΣΔMs) realized using Fully Differential (FD) *SwItched-current* (SI) circuits. Based on the analysis of building blocks, closed-form expressions are derived for the third-order intermodulation distortion of BP-ΣΔMs due to defective settling, on the one hand, and to the non-linearities of the sampling process, on the other. Time-domain simulations and measurements taken from a 0.8μm CMOS 4th-order BP-ΣΔM silicon prototype validate our approach.(*)

1. INTRODUCTION

Up to now, the potential of *SwItched-current* (SI) circuits has been barely demonstrated through actual, practical circuits. Thus, in the case of ΣΔ Modulators (ΣΔMs), performances featured by reported SI silicon prototypes are well below than those of Switched-Capacitor (SC) counterparts, even if the latter are realized in standard technologies without good passive capacitors. Such poorer performances are partly due to the larger influence of SI non-idealities, as well as to the incomplete modeling of their influence. Particularly, for BandPass ΣΔMs (BP-ΣΔMs), and due to the necessity to cope with the frequency specifications required for modern digital wireless communication systems [1], harmonic distortion due to non-linear settling becomes one of the dominant limiting factors.

There have been several attempts to model the non-linear transient response of SI memory cells [2][3][4][5][6]. Regarding harmonic distortion, a precise study of the isolated SI memory cell was presented in [5], but its mathematical complexity precludes to extend its usage to circuits containing heavily coupled memory cells, as it happens for ΣΔMs. The simplified model for Fully Differential (FD) memory cells presented in this paper enables hierarchical systematic analysis of SI circuits composed of memory cells, such as integrators and resonators. This analysis provides closed-form expressions for the third-order intermodulation distortion of BP-ΣΔMs caused by two non-linearities: the incomplete settling and the sampling process at the modulator front-end. The latter causes large harmonic distortion levels even for a low settling error, as confirmed by measurements from a 0.8μm CMOS 4th-order BP-ΣΔM [7].

2. FD MEMORY CELLS WITH NON-LINEAR SETTLING ERROR

Fig.1(a) shows a FD second-generation memory cell. In what follows, it will be assumed that the incomplete settling is the dominant non-ideality. Therefore, the effect of the charge injection error and the finite output conductance, analysed elsewhere [8], will not be considered. Besides, in most practical cases the time constant formed by the drain-source capacitance and the switch-on resistance is much smaller than that due to the gate-source capacitance, C_{gs}, and the small-signal transconductance, g_{mQ}. In such a case, the cell can be modelled by the equivalent circuit in Fig.1(b) during the sampling phase, ϕ_1. In this circuit, the large-signal behaviour is modelled by g_{m+} and g_{m-}, which represent the transconductances of $M_{+,-}$, given by $g_{m+,-} = g_{mQ}\sqrt{1+m_{i+,-}}$, where $m_{i+,-} = i_{i+,-}/I_{bias}$, $i_{i+,-} = \pm i_i/2$, and i_i is the input current [3]. Assuming that i_i keeps stationary during the sampling phase, and that the switch becomes OFF at $(n-1/2)T_s$ (T_s is the sampling period) the differential drain current, $i_d = i_{d+} - i_{d-}$, can be calculated by solving the circuit in Fig.1(b) for the initial condition $v_{g+,-} = v_{g+,-,n-1}$[†1], giving:

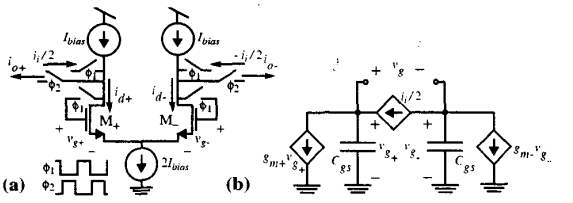

Figure 1. FD memory cell with non-linear settling error. a) Schematic. b) Equivalent circuit during the sampling phase.

$$i_{d,n-1/2} = i_{i,n-1/2}[1-\Psi(m_{i,n-1/2})] + i_{d,n-1}\Psi(m_{i,n-1/2}) \quad (1)$$

where

$$\Psi(m_{i,n}) = \frac{1}{2}\left(e^{-\frac{T_s}{2\tau}\sqrt{1+m_{i,n}}} + e^{-\frac{T_s}{2\tau}\sqrt{1-m_{i,n}}}\right) \quad (2)$$

with $\tau = C_{gs}/g_{mQ}$ and $m_{i,n} = i_{i,n}/(2I_{bias})$.

At the end of the n-th hold phase, ϕ_2, the differential output current, $i_o = i_{o+} - i_{o-}$, is given by:

$$i_{o,n} = -i_{d,n-1/2} \quad (3)$$

From (1)-(3) and considering $i_{d,n-1} = i_{d,n-3/2}$, one obtains:

$$i_{o,n} = -i_{i,n-1/2}[1-\Psi(m_{i,n-1/2})] + i_{o,n-1}\Psi(m_{i,n-1/2}) \quad (4)$$

To calculate the harmonic distortion, the function $\Psi(\cdot)$ must be approximated by a polynomial inside a given interval. For that purpose, we have combined Taylor series expansion for $m_i \ll 1$ and numerical fitting for $-0.5 \le m_i \le 0.5$, $0.01\% < \varepsilon_s < 10\%$, to obtain the following approximation:

$$\Psi(i_{i,n-1/2}) \cong \varepsilon_s + \varepsilon_{s2} i^2_{i,n-1/2} \quad (5)$$

where $\varepsilon_s = \exp[-k_s]$ is the linear settling error, $k_s = T_s/(2\tau)$, $\varepsilon_{s2} = \alpha_s \varepsilon_s k_s[(1+k_s)/(32I^2_{bias})]$, and $\alpha_s = 3/2$ is a fitting parameter.

†1. The notation $v_{g,n}$ is used to represent $v_g(nT_s)$.

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Substituting (5) into (4), yields:

$$i_{o,n} \cong -i^{*}_{i,n}(1-\varepsilon_s) + \varepsilon_s i_{o,n-1} \tag{6}$$

where

$$i^{*}_{i,n} = i_{i,n-1/2} - \varepsilon_{s2}(i^{3}_{i,n-1/2} + i^{2}_{i,n-1/2} i_{o,n-1}) \tag{7}$$

Thus the analysis of a FD memory cell with non-linear settling error can be accomplished considering a memory cell with linear error, ε_s, which has an input current equal to (7). If i_i is a sinewave of amplitude I_i and frequency f_i, i_o will contain harmonics of f_i. In FD circuits, the Total Harmonic Distortion (THD) is approximately equal to the third-order harmonic distortion, HD_3. The analysis of HD_3 can be simplified if i_o is approximated by its first-order harmonic, such that $i_{o,n} \cong -I_i \sin(2\pi f_i n T_s)$. Performing a Fourier series expansion of (7) it can be shown that the amplitude of the third-order harmonic is approximately given by:

$$A_{3f_i} \cong \frac{\varepsilon_{s2} I_i^3}{2(1-\varepsilon_s)} \sin\left(\frac{\pi f_i}{f_s}\right) \tag{8}$$

where $f_s = 1/T_s$ is the sampling frequency, and HD_3 is:

$$HD_3 \equiv \frac{A_{3f_i}}{I_i} \cong \frac{\alpha_s \varepsilon_s k_s (1+k_s)}{16(1-\varepsilon_s)} M_i^2 \sin\left(\pi \frac{f_i}{f_s}\right) \tag{9}$$

with $M_i = I_i/(2I_{bias})$.

Fig.2 compares the theoretical model with HSPICE by plotting HD_3 vs. f_i/f_s, using the same example as in [3] [5] with level-47 MOS models of a 0.8μm standard CMOS technology. In that example, $g_{mQ} = 82.8\mu A/V$, $C_{gs} = 22.1pF$, $I_{bias} = 20\mu A$, $M_i = 0.5$ and $f_s = 512kHz$. Note that predictions given by (9) agree with HSPICE and with those made by the model in [5]. However, as a difference to this latter model, the new one can also be used for predicting the harmonic distortion of higher-level SI blocks, such as integrators and resonators, and finally, complete BP-ΣΔMs.

3. HARMONIC DISTORTION IN SI RESONATORS

Resonators are the basic building blocks of BP-ΣΔMs, playing the same role as integrators in LP-ΣΔMs. Most of BP-ΣΔMs reported in the literature obtain their architecture by applying the transformation $z^{-1} \rightarrow -z^{-2}$ to the corresponding LP-ΣΔMs [1]. As a consequence of this transformation, the original integrators become resonators with a transfer function $z^{-a}/(1+z^{-2})$, where $0 < a \leq 2$. This function can be realized by several filter structures [1]. Fig.3(a) shows the block diagram of one based on LD Integrators (LDI's). This structure is advantageous as compared to the others because it remains stable under changes in the loop coefficients. Let us consider that the integrators are realized as shown in Fig.3(b) and analyse their isolate operation, assuming that memory cells are described by (4). After clock phase ϕ_1, the differential drain current of cell 2, is:

$$i_{ds_{2,n}} \equiv i_{ds_{2+,n}} - i_{ds_{2-,n}} \cong [1-\Psi(i_{x,n})] i_{x,n} + i_{ds_{2,n-1}} \Psi(i_{x,n}) \tag{10}$$

where $i_{x,n} = i_{i,n} - i_{ds_{1,n-1/2}}$ and $i_{ds_{1,n}} \equiv (i_{ds_{1+,n}} - i_{ds_{1-,n}})$ represents the differential drain current of cell 1.After clock phase ϕ_2,

$$i_{ds_{1,n+1/2}} \cong -[1-\Psi(-i_{ds_{2,n}})] i_{ds_{2,n}} + i_{ds_{1,n-1}} \Psi(-i_{ds_{2,n}}) \tag{11}$$

Assuming that the output stage (represented in Fig.3(b) as a simple current mirror) is ideal, the output current of the integrator is:

$$i_{o,n+1/2} = -i_{ds_{2,n}} \tag{12}$$

From (5) and (10)-(12),

$$i_{o,n} \cong -(1-\varepsilon_s) i^{*}_{i,n} + (1+\varepsilon_s^2) i_{o,n-1} + \varepsilon_s^2 i_{o,n-2} \tag{13}$$

with

$$\begin{aligned} i^{*}_{i,n} \cong\ & i_{i,n-1/2} - \varepsilon_s i_{i,n-3/2} - \\ & -\varepsilon_{s2}(i^{2}_{o,n} i_{i,n-1/2} + i^{2}_{o,n-1} i_{i,n-3/2}) \end{aligned} \tag{14}$$

Thus, the analysis of a SI FD integrator formed by memory cells with non-linear settling error can be accomplished considering an integrator with linear settling error whose input is equal to (14).

Let us consider the resonator of Fig.3(a). Assuming that the integrators can be modelled by (13) and (14), the finite-difference equations that govern the behaviour of the resonator are:

$$i_{1,n} = i_{i,n} - i_{o,n} \tag{15}$$

$$i_{2,n} \cong -(1-\varepsilon_s) i_{1,n-1/2} + \varepsilon_s i_{1,n-3/2} + i_{2,n-1} + i_{2H,n} \tag{16}$$

$$i_{o,n} \cong -(1-\varepsilon_s) i_{2,n-1/2} + \varepsilon_s i_{2,n-3/2} + i_{o,n-1} + i_{oH,n} \tag{17}$$

where i_1 and i_2 are respectively the input and the output of the first integrator in the loop and i_{2H} and i_{oH} are non-linear terms, respectively given by:

$$i_{2H,n} \cong \varepsilon_{s2}(i^{2}_{2,n} i_{1,n-1/2} + i^{2}_{2,n-1} i_{1,n-3/2}) \tag{18}$$

$$i_{oH,n} \cong \varepsilon_{s2}(i^{2}_{o,n} i_{2,n-1/2} + i^{2}_{o,n-1} i_{2,n-3/2}) \tag{19}$$

Assuming that $\varepsilon_s, \varepsilon_{s2}|i_{1,2,o}|^2 \ll 1$, solving for $i_{2,n}$ in (17) and substituting it in (16), obtains:

$$i_{o,n} \cong (1-2\varepsilon_s) i_{i,n} + 4\varepsilon_s i_{o,n-1} - (1-4\varepsilon_s) i_{o,n-2} \tag{20}$$

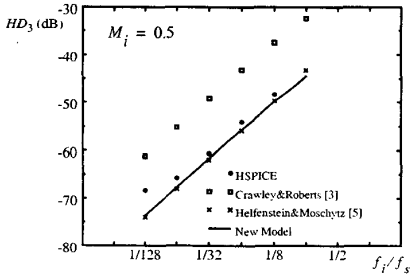

Figure 2. Comparison with HSPICE and previous models.

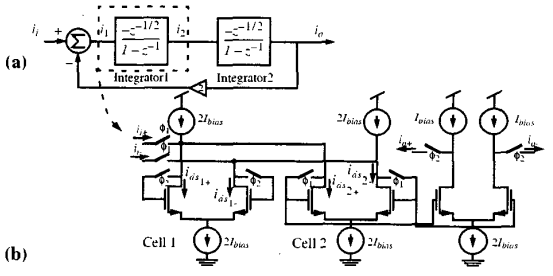

Figure 3. LDI-loop Resonator. a) Block diagram. b) SI FD LDI.

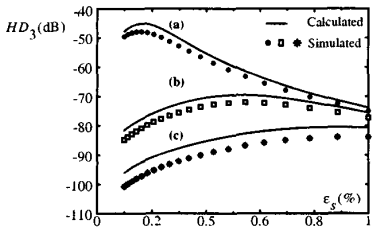

Figure 4. HD_3 at the output of a LDI-loop resonator, with f_i': a) $0.001 f_s/4$. b) $0.002 f_s/4$. c) $0.003 f_s/4$.

where $i'_{i,n} \cong i_{i,n-1} + (i_{oH,n} - i_{oH,n-1} - i_{2H,n-1/2})$.

The harmonic distortion referred to the resonator input can be calculated by analysing the harmonic content of the above expression. Therefore, assuming that i_i is a sinewave of amplitude I_i and frequency f_i, the output of the resonator will be a quasi-sinusoidal signal, with an amplitude approximately given by:

$$I_o \cong I_i \left| \frac{(1-2\varepsilon_s)z^{-1}}{1-4\varepsilon_s z^{-1}+(1-4\varepsilon_s)z^{-2}} \right|_{z=e^{j2\pi f_i T_s}} \tag{21}$$

Performing a Fourier series expansion of $i'_{i,n}$, it can be shown that the amplitude of the third-order harmonic at the resonator input is given by:

$$A_{H,3} = \left| i_{3f_i,n} \right| \cong \frac{\sqrt{2}}{2}\varepsilon_{s2} I_o^3 (1 + 5\pi f_i' T_s) \tag{22}$$

where, $f_i' = f_i - f_s/4$ and $f_i' T_s \ll 1$ has been assumed. Multiplying $A_{H,3}$ by the resonator gain (evaluated at $3f_i$) and dividing the result by I_o, obtains HD_3 at the resonator output. This analysis has been validated by time-domain simulation using the behavioural simulator for SI circuits reported in [9]. Fig.4 shows HD_3 at the output of the resonator as a function of ε_s, for different values of f_i'. This simulation was done by changing g_{mQ}, for $C_{gs} = 1\text{pF}$, $I_i = 0.5\mu\text{A}$ and $I_{bias} = 200\mu\text{A}$, when clocked at $f_s = 10\text{MHz}$. Note that HD_3 does not increase with ε_s because the open loop gain of the resonator is also attenuated by the linear error. Although simulated behaviour is well predicted by theory, their differences become larger when the condition $f_i' T_s \ll 1$ is not satisfied as assumed in theory.

4. HARMONIC DISTORTION IN SI BANDPASS ΣΔ MODULATORS

Let us consider the 4th-order BP-ΣΔM shown in Fig.5, where $A_{DAC2} = 2A_{DAC1}A_{RES}$, and assume that LDI's are realized as in Fig.3(b). For the analysis of the harmonic distortion, the following considerations have been taken into account:

- The harmonic distortion referred to the modulator input is equal to the harmonic distortion referred to the modulator output because the signal transfer function is unity in the signal band.

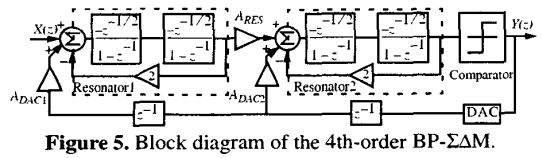

Figure 5. Block diagram of the 4th-order BP-ΣΔM.

- The contribution of the second resonator will not be considered because it is attenuated by the gain of the first resonator in the signal band.
- The quantization error, modelled as an additive white noise source, does not contribute to the harmonic distortion.

The analysis of the modulator in Fig.5 reveals that the amplitude of the first resonator output is given by:

$$I_o = A_x \left| \frac{1 + A_{DAC1} z^{-4}}{1 + z^{-2}} \right|_{z = e^{j2\pi f_i T_s}} \tag{23}$$

where A_x is the input amplitude. Substituting (23) into (22), assuming that $A_{DAC1} = -1$ and dividing by A_x, obtains that HD_3 at the output of the modulator is:

$$HD_3 \cong 4\sqrt{2}\varepsilon_{s2} A_x^2 (1 + 5\pi f_i' T_s) \cong 4\sqrt{2}\varepsilon_{s2} A_x^2 \tag{24}$$

Note that due to the oversampling, it is $f_i' T_s \ll 1$, and hence HD_3 practically does not depend on f_i. A more appropriate parameter for characterizing the harmonic distortion in BP-ΣΔMs is the third-order intermodulation distortion, given by:

$$IM_3 \cong 12\sqrt{2}\varepsilon_{s2} A_x^2 = 3\sqrt{2}\frac{\alpha_s \varepsilon_s k_s (1+k_s)}{8 n_b^2}\left(\frac{A_x}{I_{DAC}}\right)^2 \tag{25}$$

where I_{DAC} is the DAC output current and $n_b = I_{bias}/I_{DAC}$. This expression has been validated by time-domain simulation as shown in Fig.6(a) by representing IM_3 vs. ε_s †2 for different values of I_{DAC} with $A_x = I_{DAC}/2$, $I_{bias} = 200\mu\text{A}$, $C_{gs} = 1\text{pF}$ and $f_s = 10\text{MHz}$. The input signal consisted on two tones of amplitude $A_x/\sqrt{2}$ and frequencies $f_{i1} \cong 0.247 f_s$ and $f_{i2} = 0.248 f_s$. As an illustration, Fig.6(b) shows the output spectrum corresponding to $\varepsilon_s = 1\%$ and $I_{DAC} = 50\mu\text{A}$. Note that, other intermodulation products appears – not critical since they are outside the signal band.

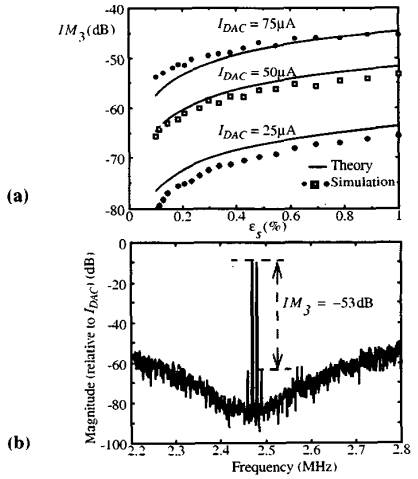

Figure 6. a) IM_3 vs. ε_s for different values of I_{DAC}. b) Output spectrum for $\varepsilon_s = 1\%$ and $I_{DAC} = 50\mu\text{A}$.

†2. The simulation was carried out by varying g_{mQ} such that $0.1\% < \varepsilon_s < 1\%$.

5. EFFECT OF S/H PROCESS AT THE FRONT-END OF SI BANDPASS ΣΔ MODULATORS

In the previous analysis it has been assumed that the input current is constant during the sampling phase. However this assumption does not apply to the memory cell connected at the input node of a BP-ΣΔM. In this case, the ratio between f_i and f_s is close to unity ($f_i/f_s = 1/4$ in the case of the modulator in Fig.5) and hence, there will be large variations of the input current during the sampling phase. As a consequence, additional harmonic distortion will appear even if $\varepsilon_s \ll 1$, which can not be explained by (9).

The harmonic distortion in memory cells connected to continuous-time sinewave currents was analysed in [6]. Here, we will extend that analysis to BP-ΣΔMs. Let us consider first the cell in Fig.1(a) and assume a sinewave input current of frequency f_i and amplitude I_i. In this case, i_d can not be solved as an step-response. In order to find an explicit solution, the circuit in Fig.1(b) was solved for $g_{m+,-} = g_{mQ}$, with the initial condition $v_{g+,-} = v_{g+,-,n-1}$. Once the solution was found, g_{mQ} was replaced by $g_{mQ}\sqrt{1+m_{i,n}}$, yielding to †3:

$$i_{o,n} \cong -i_{i,n-1/2}\varphi_{n-1/2}(i_{i,n-1/2}) + \\ + [i_{i,n-1}\varphi_{n-1}(i_{i,n-1/2})\Psi(i_{i,n-1/2}) + i_{o,n-1}\Psi(i_{i,n-1/2})] \quad (26)$$

being,

$$\varphi_n(i_i) \cong \frac{1-2\pi f_i\tau\cot(2\pi f_i nT_s)}{1+(2\pi f_i\tau)^2} - \frac{6\pi f_i\tau\cot(2\pi f_i nT_s)}{32I_{bias}^2}i_i^2 \quad (27)$$

where $i_i/I_{bias} \ll 1$ has been assumed. Following the same procedure as in Section 2, it can be shown that, for $\pi f_i\tau \ll 1$,

$$A_{H,3} \cong \frac{3\pi f_i\tau}{16(2I_{bias})^2}I_i^3 \quad (28)$$

In BP-ΣΔMs, only the first memory cell connected to the input signal will contain the above harmonic. To calculate IM_3 at the output of the modulator, it is necessary to express I_i as a function of A_x. The analysis of Fig.5 gives $I_i \cong 2\sqrt{2}A_x$. Substituting this expression in (28), and dividing by A_x it can be shown that:

$$IM_3 \cong \frac{9}{8\sqrt{2}n_b^2}\pi f_s\tau\left(\frac{A_x}{I_{DAC}}\right)^2 \quad (29)$$

where $f_i \cong f_s/4$ has been assumed. Fig.7(a) compares (29) with time-domain behavioural simulation by plotting IM_3 vs. τ for

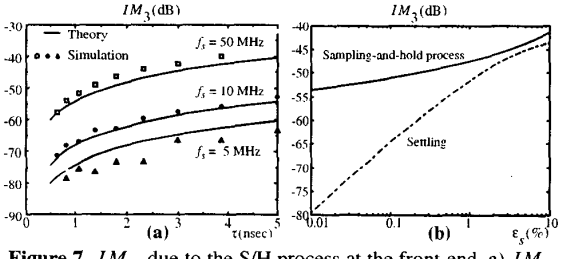

Figure 7. IM_3 due to the S/H process at the front-end. a) IM_3 vs. τ. b) Comparison with IM_3 due to non-linear ε_s.

†3. A more rigorous analysis can be done by using the Volterra series method as we demonstrated in [8], yielding to similar results.

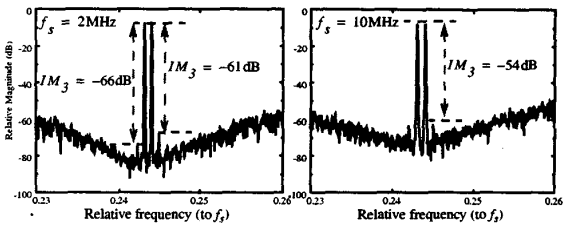

Figure 8. Measured output spectra for different values of f_s.

different values of f_s, $n_b = 4$ and $A_x/I_{DAC} = 1/2$. The theoretical model accurately predicts the simulation results except for some cases where a maximum error of 4dB occurs. In these cases a more exact analysis using the Volterra series method should be used.

To conclude this study, Fig.7(b) compares IM_3 caused by the non-linear settling error and the S/H process for $f_s = 10$MHz and $A_x/I_{DAC} = 1/2$. Note that, for $\varepsilon_s > 3\%$, both expressions approximately converge. However, for practical designs, i.e, for $\varepsilon_s < 0.1\%$, IM_3 due to the S/H process dominates, limiting the performance of SI BP-ΣΔMs unless a S/H circuit will be used at the front-end. This fact has been confirmed by experimental results from a 0.8μm CMOS 4th-order BP-ΣΔM [7]. Fig.8 shows two measured output spectra for $A_x/I_{DAC} = 0.42$ when clocked at $f_s = 2$MHz and $f_s = 10$MHz, obtaining $IM_3 = -61$dB and -54dB respectively. In this case, $g_{mQ} = 360\mu$A/V and $C_{gs} = 2.8$pF ($\varepsilon_s = 0.16\%$ at $f_s = 10$MHz), which according to (29) gives $IM_3 = -64$dB and $IM_3 = -55$dB respectively.

6. CONCLUSIONS

The effect of non-linear dynamic SI errors on the harmonic distortion of FD BP–ΣΔMs has been analysed in detail. Closed-form expressions, validated through time-domain simulation, have been derived for IM_3 due to the non-linear settling and the sampling process. The latter constitutes the main source of harmonic distortion in practical designs as demonstrated by experimental results.

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