Top-Down Design of a xDSL 14-bit 4MS/s ΣΔ Modulator in Digital CMOS Technology

R. del Río, J.M. de la Rosa, F. Medeiro, B. Pérez-Verdú, and A. Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla – CNM-CSIC
Edificio CICA-CNM, C/Tarfia s/n, 41012- Sevilla, SPAIN
Phone: +34 95 5056666, Fax: +34 95 5056686, E-mail: rocio@imse.cnm.es

Abstract

This paper describes the design of a Sigma-Delta modulator aimed for A/D conversion in xDSL applications, featuring 14-bit@4Msample/s in a 0.35μm mainstream digital CMOS technology. Architecture selection, modulator sizing and cell sizing tasks where supported by a CAD methodology, thus allowing us to obtain a power efficient implementation in a short design cycle.

1. Introduction

In many high-frequency applications (xDSL, video) the Nyquist A/D converters are being replaced by oversampled ΣΔ converters, whose reduced analog content makes them attractive for mainstream digital CMOS implementation. In these applications, increasing the signal bandwidth while maintaining an achievable sampling frequency implies the use of a moderate amount of oversampling, which requires either high-order filtering or multibit quantization at the modulator (ΣΔM) in order to keep resolution at an acceptable level. Unfortunately, both measures degrade the claimed robustness of the ΣΔ conversion: (a) Unlike 1st- and 2nd-order loops, high-order ΣΔMs are not unconditionally stable; and (b) for multi-bit quantization, the overall linearity is ultimately limited by that of the multibit DAC in the feedback path.

These insufficiencies have required the participation of correction/calibration mechanisms that significantly involve the derived architectures [1]. Within this category we find, for instance, multi-bit modulators using dynamic element matching (DEM) techniques or digital correction, or high-order loops stabilized by local resetting circuitry. In other approaches, the extra correction/calibration circuits can be eluded by the combined exploitation of some architectural features and a more careful analog design. This is, for instance, the case of the cascade dual-quantization architectures [1]. Note that, in any case, the design of ΣΔMs has become much more complex and some trite topics as "insensitivity to circuit imperfections", "robustness" and "simple design" should be definitively forgotten.

In this arena, the methodological issues are of prime importance for reaching an efficient implementation at the state-of-the-art performance edges in an acceptably short design cycle. As an answer to this necessity, a CAD methodology has been proposed for assisting the design of ΣΔMs [2]. This paper uses that methodology for designing a 4th-order 2-1-1 cascade multi-bit ΣΔM featuring 14bit@4MSample/s aimed for xDSL applications. This modulator has been implemented in a 0.35μm mainstream digital CMOS technology with the objective of minimum power consumption. Architecture selection, modulator sizing and cell sizing were supported and optimized by CAD tools, while the full-custom layout was done manually.

2. CAD methodology

Fig.1 shows a block diagram of the methodology used and already described in [2]. It is supported by three CAD tools whose major features are summarized here for completeness:

- SDOPT is a synthesis tool for ΣΔMs that allows architecture exploration and optimized transmission of the converter specifications down to those of the building

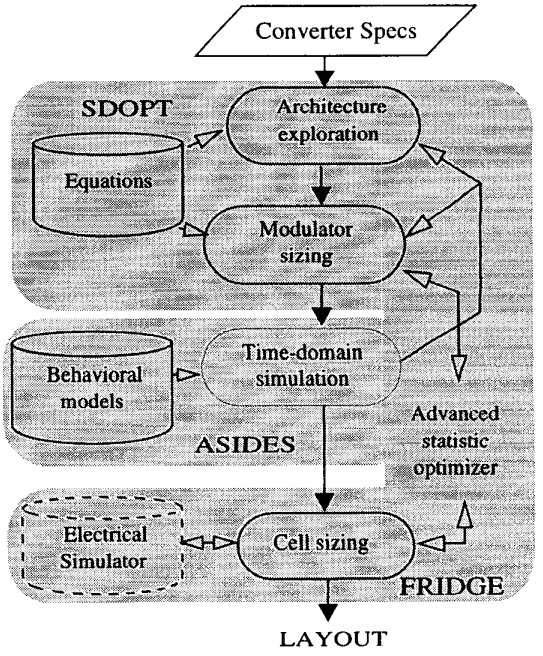

Fig. 1: Block diagram of the design methodology

(*) This work has been supported by the ESPRIT Project 29261 MIXMODEST

blocks. This process is accomplished by combining an equation data base and a statistic optimizer.

- ASIDES is a time-domain simulator based on detailed behavioral models of the building blocks.
- FRIDGE is a tool for optimum sizing of IC basic cells, based on electrical simulation and on the same optimizer used in SDOPT.

The way these tools are combined for assisting the design of the modulator presented here is described next.

3. Architectural features

As stated before, a crucial aspect toward an efficient high-frequency ΣΔM is the reduction of the oversampling ratio required to attain certain resolution. Among the architectural alternatives, the so-called cascade (MASH) multi-bit ΣΔMs are particularly interesting because they produce stable high-order noise shaping – by cascading unconditionally stable 2nd- and 1st-order loops, and robust multi-bit operation – by including a multi-bit quantizer only in the last stage, where the errors associated to the corresponding multi-bit DAC can be largely attenuated at the modulator output. Because of these architectural features, neither correction/calibration nor stabilization techniques are required, thus simplifying as much as possible the design. The price to pay for these simplifications is the necessity of a more careful design of the building blocks. However, as we shown here, these difficulties can be afforded by a proper design methodology, where the effect of the *non-idealities* is accounted for and controlled.

Several cascade multibit ΣΔMs have been reported: a 3rd-order 2-1 cascade (2-1*mb*) [3], a 4th-order 2-2 cascade (2-2*mb*) [4], and a 4th-order 2-1-1 cascade (2-1^2*mb*) [5]. As shown in [5], while in the 2-1*mb* and 2-2*mb* architectures the in-band power of the DAC-induced error is attenuated by M^5 (with M being the oversampling ratio), it is attenuated by M^7 in the 2-1^2*mb*, which considerably reduces the sensitivity of the latter to the DAC non-linearity and simplifies its design.

Fig.2 shows the 2-1^2*mb* cascade ΣΔM. The values of the $H_i(z)$ filters and coefficient in the digital part are shown in Table 1. In practice, the following considerations must be taken into account regarding the selection of the integrator weights in Fig.2: (a) The level of the signal transferred from one stage to the next in the cascade must be low enough to avoid overloading the latter; (b) The output swing required for the integrators, must be physically achievable given the limitation of the supply voltages; (c) Digital coefficient d_3, which amplify the last-stage quantization error power, should be as small as possible. After extensive simulation with ASIDES, the set of coefficients fulfilling the previous considerations has been derived: $g_1 = g_1' = 0.25$, $g_2 = 1$, $g_2' = 0.5$, $g_3 = 1$, $g_3' = g_3'' = 0.5$, $g_4 = 2$, $g_4' = g_4'' = 1$; and consequently $d_0 = -1$, $d_1 = 2$, $d_2 = 0$, $d_3 = 2$. With these values the output swing requirement is reduced to only the reference voltages. In addition, the last-stage quantization error is amplified by $d_3 = 2$. This means a systematic loss of resolution of only 6dB (1bit) respect to the ideal case. As an extension of the former to one more order, a 5th-order 2-1-1-1 cascade multi-bit ΣΔM (2-1^3*mb*) has been presented in [6] that augments the attenuation of the last-stage DAC errors up to M^9, while preserving its small systematic loss. Another 5th-order multibit cascade that can be considered, a 2-2-1*mb* ΣΔM, is discarded at this point because the set of coefficients required to avoid overloading lead to an amplification of the last-stage quantization error by a factor 8 (3bit systematic loss). The same applies to the 2-2-2 cascade. For these modulator the systematic loss can be reduced by including multi-bit quantization in all stages [7], but this further complicates the design due to the need of DEM techniques to attenuate the effect of the multi-bit DAC non-linearity. According to the previous discussion, we will limit the architecture choices to the 2-1^{2}mb and to the 2-1^{3}mb ΣΔMs.

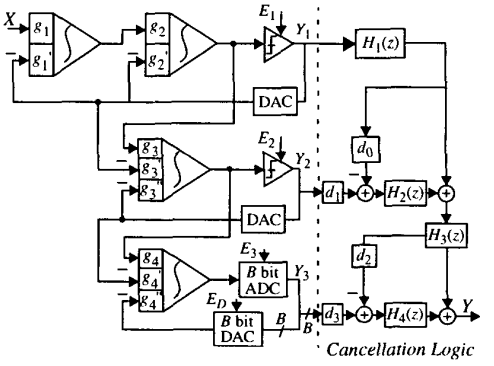

Fig. 2: 4th-order 2-1-1 cascade multibit ΣΔM(2-1^2*mb*)

TABLE 1: Digital transfer functions and relationships for the 2-1^2 ΣΔM.

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - \frac{g_3'}{g_1 g_2 g_3}$	$g_1' = g_1$
$H_2(z) = (1-z^{-1})^2$	$d_1 = \frac{g_3''}{g_1 g_2 g_3}$	$g_2' = 2 g_1' g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3'' g_4$
$H_4(z) = (1-z^{-1})^3$	$d_3 = \frac{g_4''}{g_1 g_2 g_3 g_4}$	

4. Influence of circuit imperfections

Table 2 summarizes the non-idealities analyzed and implemented in SDOPT and ASIDES, together with their impact on the modulator performance. Out of these, integra-

tor leakage (due to the finite opamp open-loop DC gain) and weight mismatching are the most degrading non-idealities for the cascade ΣΔMs. Both result in an incomplete cancellation of the quantization error of the former stages that corrupts the modulator *DR* .

TABLE 2: Non-idealities covered in SDOPT and ASIDES

Building blocks		Non-idealities	Consequences
Integrators	Opamps	Finite, non-linear gain	Shaping degradation, harmonic distortion
		Dynamic limitations	Settling error, distortion.
		Output swing	Overloading, harmonics distortion
		Thermal noise	White noise.
	Switches	ON-resistance, thermal noise	Settling error, white noise, distortion.
	Capacitors	Non-linearity, mismatching	Shaping degradation, harmonic distortion.
	Clock	Jitter	Jitter noise.
	Comparators	Hysteresis, offset	Increased quantization noise.
	Quantizers/ DACs	Non-linearity, gain error, offset	Distortion, extra quantization error

Analysis shows that the extra in-band error power due to these non-idealities is:

$$\Delta P \approx \sigma_C^2 \left[\frac{(g_1 + g_2 + g_2')^2}{A_v^2} \frac{\pi^2}{3M^3} + \varepsilon_1^2 \frac{\pi^4}{5M^5} \right] \qquad (1)$$

where A_v stands for the opamp DC-gain, ε_1 refers to mismatching in weights g_1, g_2, g_3 and g_3'', and $\sigma_C^2 = \Delta^2/12$ is the quantization error power of a single-bit quantizer. These extra error power may eventually mask the benefit of using multi-bit quantization, thus imposing a limit to the maximum useful resolution in the last-stage quantizer. SDOPT and ASIDES have been used to evaluate this limit. Fig.3 shows the effective resolution of the 2-1^2*mb* and 2-1^3*mb* modulators when varying the last-stage quantizer resolution *B*, with *M* acting as a parameter (depicted over each curve). The thick solid line is intended to grossly estimate the limit, over which, increasing *B* would not further improve the modulator *DR*. Nevertheless, resolutions below this limit are enough to significantly relax the circuit requirements with respect to single-bit approaches.

By including the dynamic requirement in the integrators, it is possible to make an estimation of the power consumption associated to the [*M*, *B*] pairs in Fig.3 and use this criterion for automatic architecture selection. Our results show that the minimum power dissipation can be achieved with $M = 16$, $B = 4$ for the 2-1^2*mb* and $M = 14$, $B = 3$ for the 2-1^3*mb* modulator. Fig.4 shows the effective resolution estimated using ASIDES as a function of the mismatching in integrator weights, with typical values of the amplifier gain and last-stage DAC non-linearity. Note that the sensitivity to mismatch is significantly larger in the 2-1^3*mb* modulator than in the 2-1^{2}mb; while the latter can afford up to 0.3%, the performance of the former drops below 14bit for

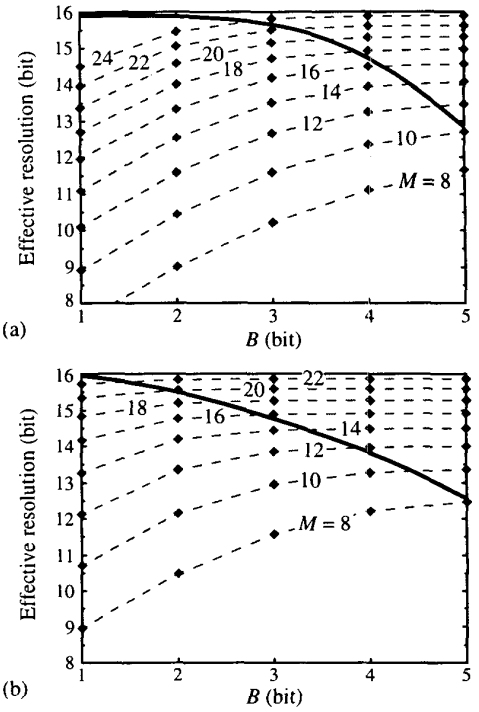

Fig. 3: Modulator resolution vs. last-quantizer resolution for: (a) 2-1^2*mb* ΣΔM and (b) 2-1^3*mb* ΣΔM. (A_v = 2500, weight mismatch σ = 0.1%, and DAC *INL* = 0.4% FS)

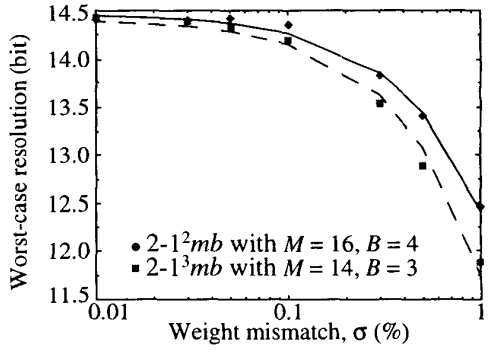

Fig. 4: Simulated resolution as a function of the integrator weight mismatching (A_v = 2500, DAC *INL* = 0.4% FS)

σ larger than 0.1%. This is a crucial aspect due to the absence of double poly capacitors in the intended technology. According to the measurements performed on multi-metal capacitors, their matching is not better than 0.2%, which obligates to discard the 2-1^3*mb* architecture for this application.

5. Switched-capacitor implementation

The transmission of the specifications of the 2-1^2*mb* modulator down to those of its building blocks has been performed using SDOPT. Table 3 summarizes the circuit requirements providing 14bit@4MS/s. The contributions to the in-band error power are also shown. Note that it is dominated by quantization (-85dB). This includes the effect of integrator leakage and weights mismatch. The unitary capacitor value (0.5pF) is set according to thermal noise and dynamic considerations. Both error powers are well below the limit imposed by the modulator resolution.

Fig.5 shows the fully-differential SC implementation of the 2-1^2*mb* $\Sigma\Delta$M. A single-bit quantizer (comparator) at the end of the first stage, together with two AND gates, provides the feedback signals A_1,B_1 to switch the integrator sampling capacitors to either V_r+ = +1V or V_r- = -1V. Since the circuit is fully differential, the resulting reference voltages are ±2V. The second stage and third stages have two-branch integrators. The last integrator drives a programmable ADC whose resolution can be switched among 2, 3, and 4bit, for model fine-tuning purposes.

The requirements in Table 3 for the integrator and the amplifier apply only to the first integrator in the cascade. Some specifications, as amplifier DC-gain and dynamics, can be relaxed for the second, third, and fourth integrator, because their in-band error power contributions are attenuated by increasing powers of M. The same applies for thermal noise, which allows reduction of the unitary capacitor to 0.25pF for these integrators, which further relaxes their dynamic requirements. ASIDES has been used for fine-tuning the specifications of these blocks. For instance, DC gain requirement was reduced to 62dB, 54dB and 54dB for OA2, 3 and 4, respectively.

TABLE 3: Modulator sizing results

SPECS: 14bit@4MS/s@1.1V$_p$		2-1^2*mb*
Modulator	Oversampling ratio	16
	Sampling frequency	64MHz
	Reference voltages	±2V
Integrators	Sampling capacitor	0.5pF
	Unitary capacitor	0.5pF
	Sigma	0.12%
	Capacitor non-linearity ≤	25ppm/V
	Bottom parasitic capacitor	20%
	Switch ON-resistance ≤	250Ω
Opamps	DC-gain	68dB
	DC-gain non-linearity ≤	20%V^{-2}
	Transconductance ≥	2.5mA/V
	Maximum output current ≥	±0.95mA
	Output swing ≥	±2V
Comparators	Hysteresis ≤	30mV
A/D/A Converter	Resolution	4bit
	Non-linearity (*INL*) ≤	0.4%FS
Dynamic range		87.2dB 14.2bit
Quantization noise		-85.0dB
Thermal noise		-94.8dB
Incomplete settling noise		-96.9dB
Harmonic distortion		-99.4dB

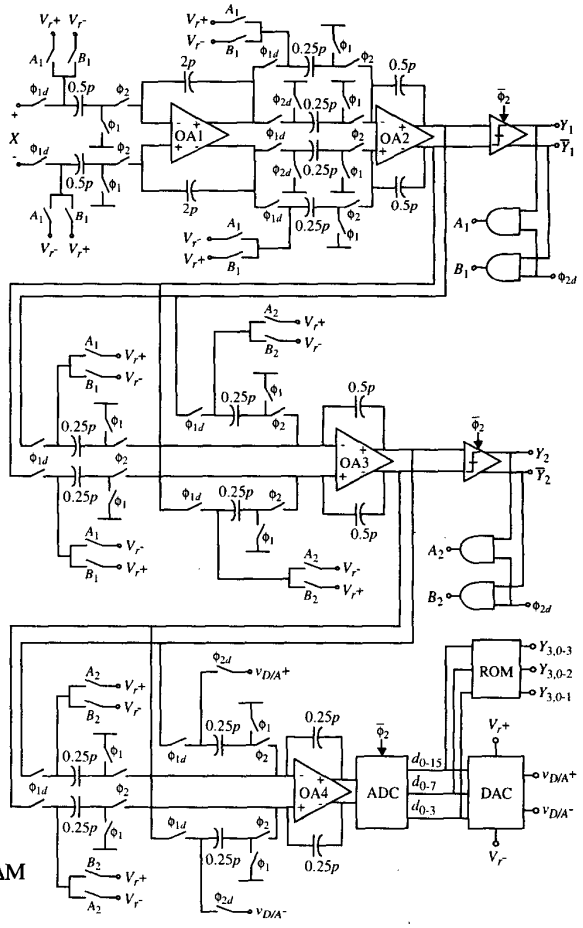

Fig. 5: SC implementation of the 2-1^2*mb* $\Sigma\Delta$M

The diversity of specifications recommends a dedicated design for each amplifier to avoid over-sizing and optimize the power consumption. This task does not imply a significant time penalty due to the use of the basic cell optimizer FRIDGE. A two-stage architecture, was selected for OA1 in order to fulfil its DC-gain requirement. It uses a telescopic first stage and Miller compensation. A single-stage folded-cascode OTA, has been used in OA2, OA3, and OA4 – enough to accomplish their medium-, low-DC-gain requirements. The common-mode feedback nets are of dynamic type for all amplifiers, because it yields smaller power consumption than static ones.

Comparators at the end of the first and second stages of the ΣΔM demand a low resolution time, while hysteresis as large as 30mV can be tolerated. This recommends the use a dynamic comparator based on a regenerative latch, with no need of a pre-amplifying stage. Given the low sensitivity of the 2-1^2*mb* architecture to the imperfections of the las-stage A/D and D/A conversion, a simple design consisting of a 4bit fully-differential flash ADC (with an programmable output code) driving a poly-resistor ladder DAC was adopted.

The modulator has been extensively evaluated in ASIDES, including the non-idealities derived from the final implementation of the building blocks. Fig.6 shows the signal-to-(noise+distortion)-ratio *SNDR* of the modulator as a function of the input level, when operating with $M = 16$ and $B = 4$. For these parameters a *DR* of 85.5dB is achieved. Additional programable operation modes and achieved resolutions are also depicted.

Fig.7 shows the layout of the prototype fabricated in a 0.35μm CMOS digital technology with epi conductive substrate. Its occupies 1.32mm^2 without pads and consumes 78.3mW: 60.2mW for the analog blocks, 4.5mW for the digital part, and 13.6mW for the output drivers. Fig.8 shows the measured output spectrum of the complete modulator and those corresponding to the first stage (2nd-order) and to the combination of the first and second stages (3rd-order). Note the increase in the order of the shaping of the quantization noise. This shaping has almost disappeared in the spectrum corresponding to the complete modulator most probably because of the presence of switching noise as shown by a quick increase of the noise floor with the clock frequency. The switching noise

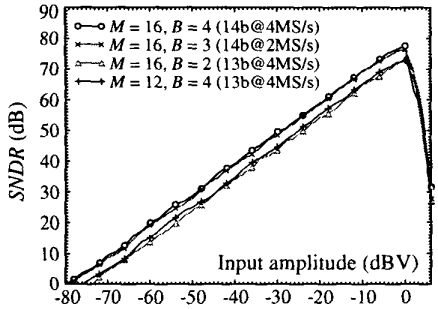

Fig. 6: Simulated *SNDR* curves for different *M,B* pairs

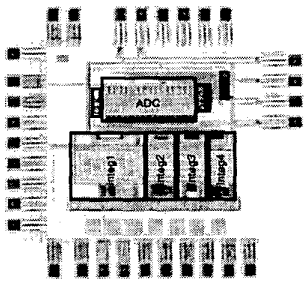

Fig. 7: Layout of the 2-1^2*mb* ΣΔM

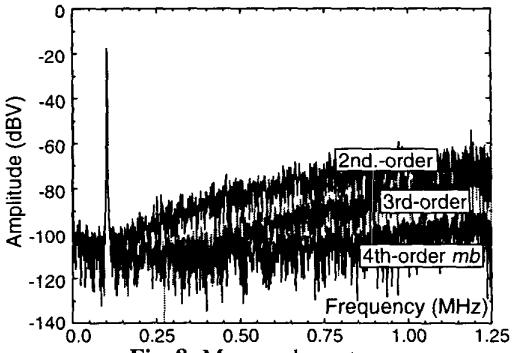

Fig. 8: Measured spectra

(mainly that generated in the output buffers) is coupled to the whole chip due to the conductive nature of the deep substrate in the epi technology used. As stated in [8], no protection is actually effective at the layout level. Because of that, we are now revising our test set-up to reduce this noise at the board level. For the moment, the measured dynamic range is 81dB clocking at 35.2MHz (2.2-MS/s digital output rate) and 74.5dB at 64-MHz clock frequency (4-MS/s digital output rate). A more detailed description of the measurements will be presented at the conference.

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