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A 2.5-V CMOS Wideband Sigma-Delta Modulator

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Abstract *- A high-performance ΣΔ modulator for wireline communication applications is presented. It employs a 4th-order cascade multi-bit architecture that requires only 16 oversampling ratio, and has been implemented using fully-differential SC circuits in a 0.25-μm CMOS technology. Measurements show a dynamic range of 84dB operating at 2.2MS/s output rate, and 79dB at 4.4MS/s. The whole prototype dissipates 65.8mW from a 2.5-V supply.*

I. INTRODUCTION

The increasing demand for ever faster wireline communication challenges mixed-signal designers to integrate A/D and D/A interfaces featuring 12- to 16-bit for signal bandwidths well in excess of 1MHz [1]. In addition, these specifications must be achieved in a low-voltage scenario, making use of poor performance (and often badly characterized) devices, which decreases the "analog speed" of deep-submicron CMOS processes.

In this context, oversampled Sigma-Delta modulation (ΣΔM) [2] is usually preferred to other A/D conversion techniques for its low-complexity analog circuitry and robustness. However, the latter is absolutely true only if the oversampling ratio (M) is high, which obviously cannot be the case in high-speed communication. In fact, in spite of the increasing potential speed of the new CMOS processes, the trend is to decrease M, because of the concurrent increase of the bandwidth specification.

In order to cope with oversampling ratios below 32, high-order filtering and/or multi-bit quantization must be used [3]-[13]. As known, both strategies degrade the original robustness of the highly oversampled low-order single-bit ΣΔ conversion, which often obligates to resort to correction/calibration mechanisms and, definitely, to a more careful analog design.

All these difficulties become harder the lower the supply voltage. On the one hand, reducing the supply voltage hard limits the achievable dynamic range (DR). On the other, it invalidates some popular circuit techniques, such as cascode devices. In fact, only two wideband sigma-delta converters have been reported so far in 2.5-V CMOS technologies, namely [9] and [11]. They are representative of the two main architectural tendencies: a) high-order single-loop multi-bit topologies [10][11]; and b) high-order cascade (MASH) multi-bit topologies [3]-[9], whose pros and cons are beyond the scope of this paper. Although the modulator presented here belongs to the latter category, it has a substantial difference as compared to [9], that is explained in Section 2. Section 3 describes its SC implementation and building blocks. Last, experimental results are given in Section 4.

II. MODULATOR ARCHITECTURE

Fig.1 shows the block diagram of the architecture adopted. The values of the integrator weights have been selected to minimize the systematic loss of dynamic range due to overloading issues, and to easy a 2.5-V supply SC implementation. Instead of using multi-bit quantization in all stages, like in [9] (thus sharing the DAC linearity bottle-neck with the single-loop multi-bit modulators), multi-bit quantization is used only in the last stage of a 3-stage 2-1-1 cascade. This dual-quantization approach [7][8] – single-bit quantizers are used in the remaining stages – considerably

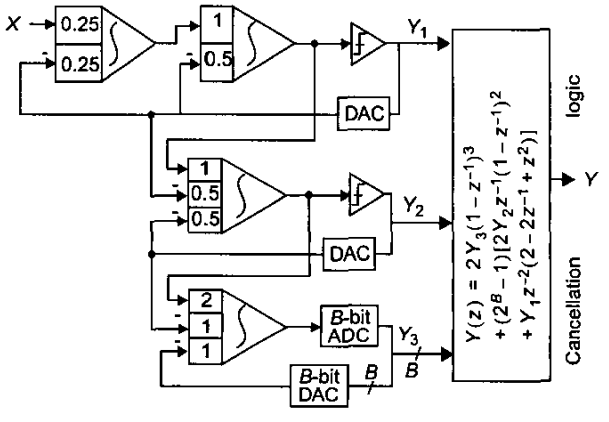

Fig. 1. 4th-order 2-1-1 cascade multi-bit ΣΔM.

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simplifies the design of the circuitry, because the DAC linearity is largely relaxed by the inherent attenuation of such an error in these topologies [8]. The price to pay is a larger sensitivity to some circuit imperfections: namely, capacitor ratio mismatching and finite amplifier DC-gain. All these effects can be combined in the following approximate equation for the in-band error power,

$$P_E \cong \sigma_Q^2 \frac{4\pi^8}{9M^9} + \sigma_D^2 \frac{4\pi^6}{7M^7} + \frac{\Delta^2}{12}\left(\frac{7}{4A_v^2} \frac{\pi^2}{3M^3} + 24\sigma_{cr}^2 \frac{\pi^4}{5M^5} \right) \quad (1)$$

where the first term represents the ideal quantization noise contribution, with $\sigma_Q^2 = [\Delta/(2^B - 1)]^2/12$ being the quantization error power of a B-bit quantizer with Δ full scale. The second term accounts for the contribution of the last-stage DAC non-linearity, where $\sigma_D^2 = \Delta^2 (INL)^2/2$ is an estimation of the error power induced by a DAC with *INL* integral non-linearity referred to the full scale. Note that the latter contribution is inversely proportional to M^7, which considerably attenuates its impact, even for low oversampling ratios. This appealing feature allows us to use straight-forward circuitry for implementing the last-stage ADC and DAC, with neither correction nor calibration required.

The first term in parenthesis in (1) reflects the excess of in-band error power due to integrator leakage (A_V is the amplifier DC-gain), whereas the second term accounts for the impact of mismatching in integrator weights, with σ_{cr} being the sigma of capacitor mismatching error. Note that the latter errors are only 1st- and 2nd-order shaped (their in-band error powers are inversely proportional to M^3 and M^5), so that these extra error powers can ultimately limit the benefits of multi-bit quantization in the last stage. This is illustrated in Fig.2, where we show the resolution of the architecture used vs. the multi-bit quantizer resolution B (with M being a parameter), in the presence of typical values for A_V, σ_{cr}, and DAC *INL*. The thick solid line estimates the boundary beyond which increasing B would not further improve *DR*.

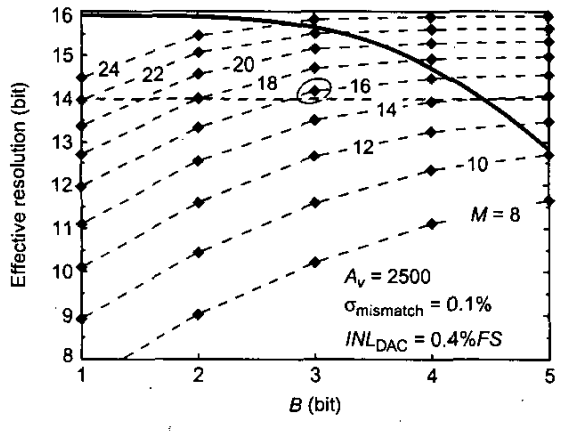

Fig. 2. ΣΔM resolution vs. multi-bit resolution.

However, resolutions below this limit are enough to significantly relax the circuit requirements with respect to single-bit approaches, especially the integrator dynamics, which often establish the feasibility limit in high-speed converters. By including these dynamic requirements, an estimation of the power consumption associated to the different [M, B] pairs can be made, and used for optimum architecture selection. Note that 14bit can be achieved with $M = 16$, $B = 3$, which establishes a good trade-off between circuit complexity and clock frequency (70.4MHz for 4.4MS/s).

III. SWITCHED-CAPACITOR IMPLEMENTATION

Fig.3 shows the SC implementation of the ΣΔM in Fig.1. Note the distribution of the integrator weights among the input stages of the four SC integrators in order to save area. The modulator operation is controlled by two non-overlapped clock-phases. In order to attenuate the signal-dependent clock feedthrough, delayed versions of the two phases, ϕ_{1d} and ϕ_{2d}, are also provided. This delay is incorporated only to the falling edges of the clock-phases, while the rising edges are synchronized in order to increase the effective time-slot for the modulator operations [12]. The comparators and the ADC are activated at the end of phase ϕ_2, using ϕ_{2d} as a strobe signal, to avoid any possible interference due to the transient response of the integrators outputs at the beginning of the sampling phase. The reference voltages have been set to ±1.5V (equivalent to $V_r = 0.75$ in the fully-differential implementation) – enough to accommodate a full-scale DMT signal.

The sampling capacitor of the first integrator, implemented using MiM structures, has been set according to thermal noise and integrator dynamics criteria. A lower value has been used in the remainder integrators, whose contributions to the in-band error power are gradually smaller. This also relaxes the dynamic specifications for these integrators, and the same applies to other specifications such as DC-gain. Although not essential for performance, this relaxation significantly reduces the power dissipation and hence increases the design efficiency at the cost of designing more than one amplifier to fit in with the assorted requirements. After deriving appropriate values for the building block specifications making use of the methodology in [2], two different opamps were designed:

- one for the 1st and 2nd integrator: OPA, requiring 70dB DC-gain, 315MHz gain-bandwidth product, 750V/μs slew-rate, and 1.8V output-swing), and
- another for the 3rd and 4th: OPB, requiring 56dB, 210MHz, 350V/μs, and 1.6V, respectively.

The electrical design was speeded up by the support of the basic cell optimizer in [2].

As known, both the DC-gain/output swing, and slew-rate/output swing trade-offs get tighter in a 2.5-V

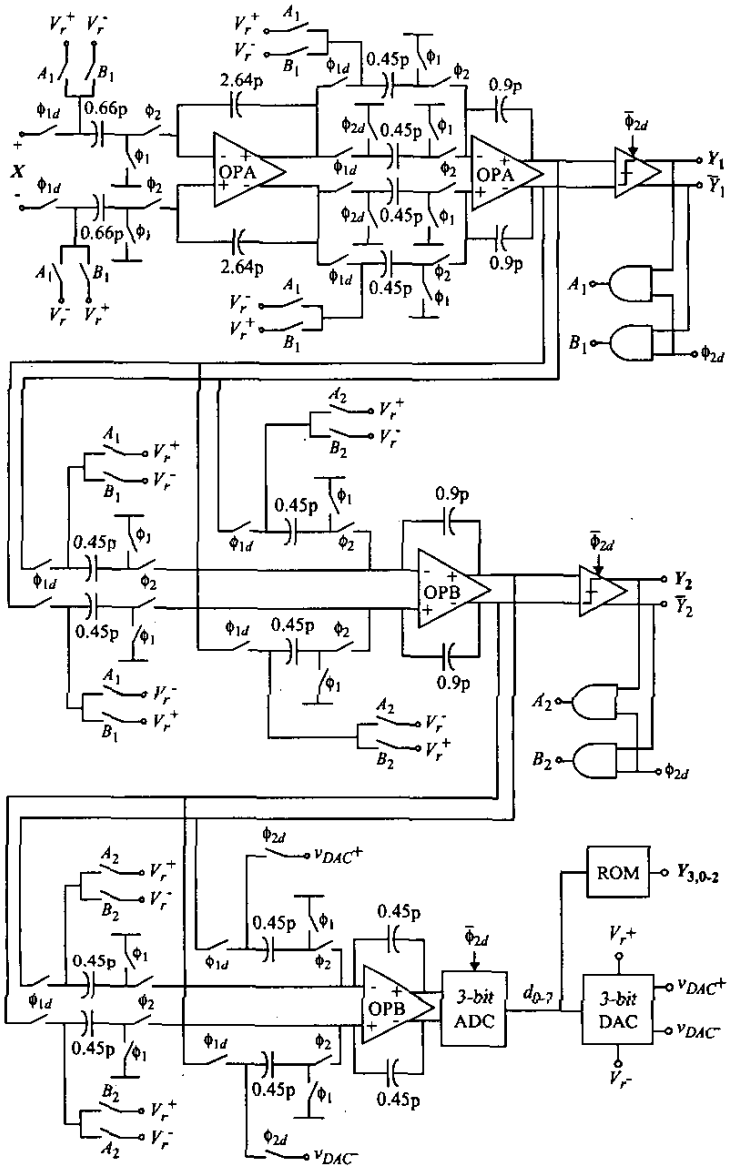

Fig. 3. SC implementation of the ΣΔM.

implementation. On the one hand, the supply voltage shrinking forces to use two-stage amplifiers to obtain high DC-gain in a reduced output voltage range, resulting in highly non-linear gain. On the other hand, high slew-rate requires large device current and hence reduced voltage range. Thus, there is a trade-off between transient response linearity and output swing – the more evident the lower the supply voltage. Both non-linear effects may generate distortion and have been carefully controlled during the design phase following table look-up procedures.

After exploring several alternatives for power optimization, the two-stage topology in Fig.4 was selected for OPA in order to fulfil its larger DC-gain specification. It uses a telescopic 1st-stage, and both Miller and Ahuja compensation [14]. This topology provides a robust control of the current in the second stage, preserving a high output-swing. OPB is a single-stage folded-cascode OTA – enough to achieve its lower DC-gain, with reduced power dissipation. The common-mode feedback nets are of dynamic type in order to further reduce power and avoid voltage range problems.

Switches are also critical in a 2.5-V implementation because the threshold voltage of the MOS devices is not scaled down at the same rate as the supply voltage. So, the CMOS transmission gates exhibit considerable on-resistance

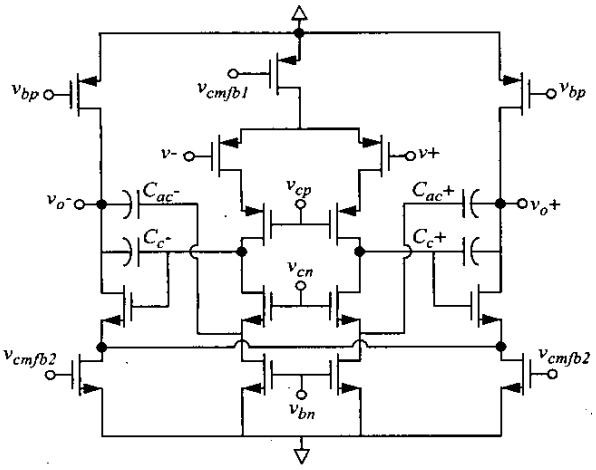

Fig. 4. 2-stage 2-path compensated OTA.

in low-voltage technologies. Most importantly, the on-resistance exhibits a highly non-linear characteristic that may cause dynamic distortion [15]. Including clock-bootstrapping increases complexity and leads to a less robust design. This can be avoided by properly sizing the CMOS switches and the input capacitor in the differential sampling circuitry of the first integrator. Exhaustive electrical simulation reveals that $THD < -95\text{dB}$ for a maximum-frequency full-scale input sinewave. Thus, clock-boosting is not required in the technology adopted.

Comparators at the end of the 1st and 2nd stage of the cascade require a low resolution time, while uncertainty must be kept bellow 20mV. A regenerative latch with a small pre-amplifying stage was adopted. Given the low sensitivity of this ΣΔM to the errors in the multi-bit stage, a simple 3-bit flash ADC driving a poly-resistor ladder DAC was used, with no calibration/correction circuitry.

IV. EXPERIMENTAL RESULTS

Fig.5 shows a microphotograph of the prototype fabricated in a 0.25-μm CMOS technology. It occupies 2.78mm^2 without pads and dissipates 65.8mW (including I/O digital buffers) from a 2.5-V supply. The modulator has been tested in a 4-layer PCB including intensive filtering and decoupling strategies, as well as proper impedance termination to avoid reflections in high-frequency signals. A standard digital tester was used to provided a low-jitter external clock signal that is buffered prior to the on-chip clock-phase generation. The tester was also used to capture the 5 output bitstreams that were later combined and processed by software. The input signal consisted of a high-precision sinewave provided by a fully-differential generator with $THD < -100\text{dB}$. The reference voltages are generated on-chip and their impedance is kept small through both on- and off-chip decoupling

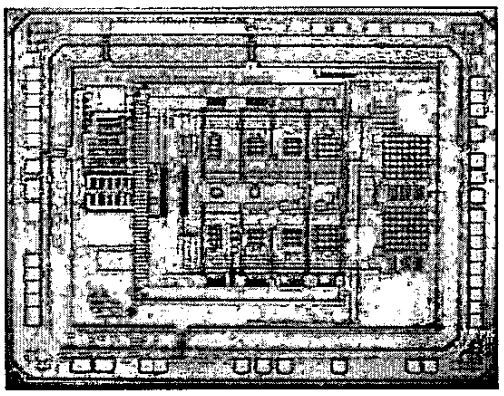

Fig. 5. Die microphotograph.

strategies. Fig.6(a) shows a 65536-sample FFT of the modulator output for a -3.8dBV@150kHz input sinewave sampled at 70.4MHz. The in-band noise is almost flat, and the spurious level is small. However the noise floor is higher than expected and changes with the sampling frequency, as shown in Fig.6(b) for two values of the oversampling ratio. Note that

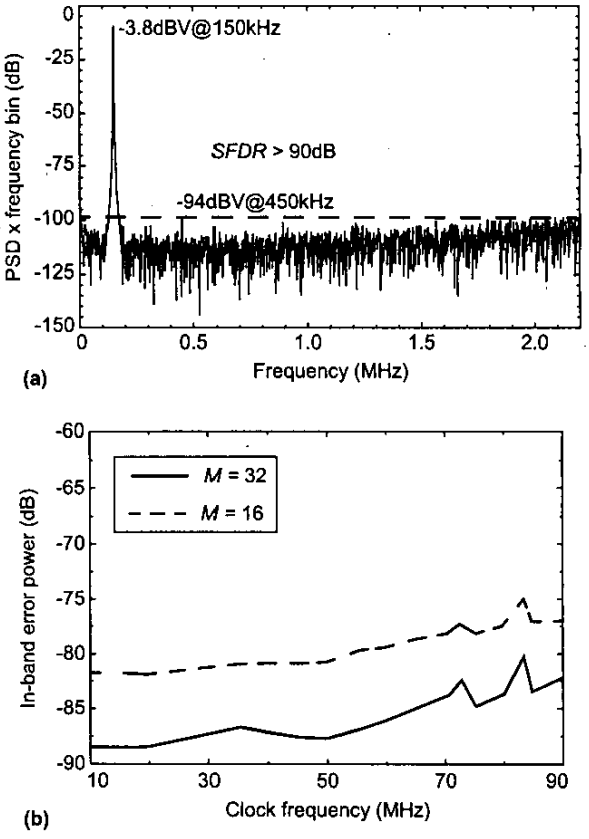

Fig. 6. (a) Measured baseband spectrum, (b) In-band error power vs. clock frequency.

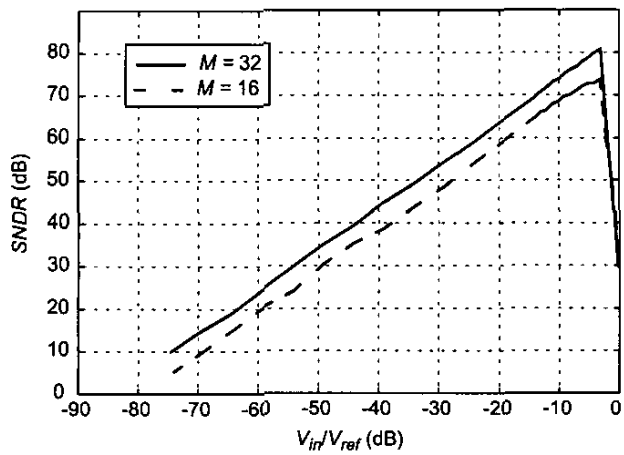

Fig. 7. *SNDR* vs. input level for $M = 16, 32$.

around the nominal clock frequency the performance is degraded due to the impact of the switching activity, specially that in the I/O buffers, which is distributed along the chip through the pad ring. Significantly, the in-band error power decreases with temperature, reaching a minimum at 110°C. This is explained by the slowdown of the digital circuitry caused by the temperature increase, which attenuates the high-frequency components of the switching signals.

Fig.7 shows the signal-to-(noise+distortion)-ratio *SNDR* as a function of the input level (0dB = reference voltage). For $M = 16$, the *DR* measured is 79dB (12.8bit) with a *SNDR* peak of 74dB; for $M = 32$, *DR* = 84dB (13.7bit) and *SNDR* peak = 81dB. With the performance measured at $M = 16$, the low consumption of this prototype yields 2.1pJ for the $Power/(2^{bit} \cdot \text{Nyquist rate})$ figure-of-merit (FOM), which is the third smallest value reported for high-frequency ΣΔ modulators, only behind [6] (5-V 0.5μm CMOS, FOM = 1.3pJ) and [9] (2.5-V 0.5μm CMOS, FOM = 1.14pJ).

ACKNOWLEDGMENT

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