

ANALYSIS OF CLOCK JITTER ERROR IN MULTIBIT CONTINUOUS-TIME $\Sigma\Delta$ MODULATORS WITH NRZ FEEDBACK WAVEFORM

Ramón Tortosa, José M. de la Rosa, Angel Rodríguez-Vázquez and Francisco V. Fernández

Instituto de Microelectrónica de Sevilla – IMSE-CNM (CSIC)
Edificio CICA-CNM, Avda. Reina Mercedes s/n, 41012- Sevilla, SPAIN
Phone: +34 95 5056666, Fax: +34 95 5056686, E-mail: {tortosa|jrosa|angel|pacov}@imse.cnm.es

ABSTRACT

This paper presents a detailed study of the clock jitter error in multibit continuous-time $\Sigma\Delta$ modulators with non-return-to-zero feedback waveform. Closed-form expressions are derived for the in-band error power and the signal-to-noise ratio showing that the jitter-induced noise can be separated into two main components: one depending on the modulator loop filter and the other one due to the input signal. The latter, not considered in previous approaches, allows us to accurately predict the signal-to-noise ratio degradation and to optimize the modulator performance in terms of jitter insensitivity. Moreover, the use of state-space formulation makes the analysis quite general and applicable to either cascaded or single-loop architectures. Time-domain simulations of several modulators are shown to validate the presented approach.^{†1}

1. INTRODUCTION

Nowadays, the increasing demand for ever faster Analog-to-Digital Converters (ADCs) in broadband communication systems has boosted the interest in Continuous-Time (CT) Sigma-Delta Modulators ($\Sigma\Delta$ s). These modulators offer an intrinsic antialiasing filtering and provide potentially higher sampling rates with lower power consumption than their Discrete-Time (DT) counterparts [1][2]. However, CT $\Sigma\Delta$ s are more sensitive than DT $\Sigma\Delta$ s to several circuit non idealities. One of their major degrading factors, especially in high-speed applications, is due to uncertainties in the clock signal edges, commonly referred to as clock jitter [1].

Clock jitter in CT $\Sigma\Delta$ s has been object of several studies reported in open literature [1][3]-[7]. Most of them were carried out considering $\Sigma\Delta$ architectures with an internal single-bit quantizer and a Return-to-Zero (RZ) Digital-to-Analog Converter (DAC). However, multibit quantization has been used in most silicon prototypes achieving medium-high resolutions (11-14 bit) within high signal bandwidths (1-15 MHz) [8]-[10]. The combined use of high-order (3rd-4th order) single-loop architectures with multibit (3-6 bit) quantization allows to reduce the oversampling ratio (normally < 12) while guaranteeing stability and robustness with respect to circuit parameter tolerances – the latter being a very critical error in CT $\Sigma\Delta$ s [1][2]. In addition to improve resolution, multibit quantization can reduce the sensitivity of CT $\Sigma\Delta$ s to clock jitter if a Non-Return-to-Zero (NRZ) feedback waveform is used in the DAC [9]. Therefore, their study is needed in order to optimize the modulator performance in terms of sensitivity to jitter error.

The analysis of clock jitter in CT $\Sigma\Delta$ s considering a NRZ feedback waveform is mathematically more complex than using a RZ

pulse shaping. In most cases, designers resort to semi-empirical estimations based on simulation results and consider a white-noise model for the jitter error [1][5][9]. To the best of the authors' knowledge, only the work in [7] takes into account the effect of the modulator loop filter transfer function on the in-band jitter noise power of CT $\Sigma\Delta$ s with NRZ DAC. However, the analysis in [7] does not consider the effect of input signal for the sake of simplicity.

This paper analyzes the effect of signal-dependent clock jitter in multibit CT $\Sigma\Delta$ s with NRZ DAC. State-space formulation [11] is used to derive closed-form relations among jitter error, modulator specifications, loop filter transfer function and input signal parameters. The results of this study – applicable to any modulator topology – show effects not considered in previous approaches which become critical in high frequency applications. As an illustration several modulators using either single-loop or cascaded topologies are simulated to demonstrate the theoretical predictions.

2. CLOCK JITTER IN CT $\Sigma\Delta$ S WITH NRZ DACS

Fig.1 shows the conceptual block diagram of a single-loop CT $\Sigma\Delta$. The loop filter is CT and the sampling operation is realized before quantization instead of at the modulator input as done in the case of DT $\Sigma\Delta$ s. Thus, the output signal, $y(n)$ ^{‡2}, is DT, the input signal, $x(t)$, is CT and a DT-to-CT transformation is implemented by the DAC to create the CT feedback signal, $y(t)$. Therefore, there are two clocked building blocks subject to jitter error: the sampler and the DAC. The error introduced through the sampling process is reduced by the loop gain and shaped in the same way as the quantization noise and hence, its effect can be neglected. On the contrary, the jitter error associated to the DAC directly adds with the input signal, thus increasing the in-band noise power and degrading the modulator performance.

In the case of a NRZ DAC, the error sequence can be related to the output signal using the following relationship [1]:

$$\epsilon(n) = (y(n) - y(n-1)) \frac{\Delta T(n)}{T_s} \quad (1)$$

where T_s is the sampling period and $\Delta T(n)$ is the time uncertainty.

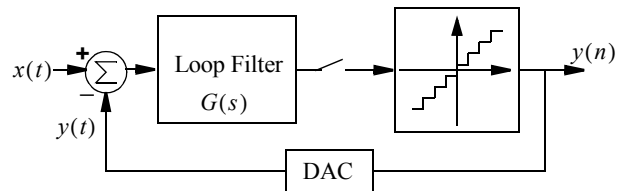


Figure 1. Conceptual block diagram of a single-loop CT $\Sigma\Delta$.

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^{‡2}. In order to simplify the notation, $y(nT_s)$ is written as $y(n)$ with T_s being the sampling period.

Assuming that the input signal and the quantization error are uncorrelated and that $\Delta T(n)$ is a Gaussian random process with zero mean and standard deviation $\sigma_{\Delta T}$, the power of the jitter error signal can be written as:

$$P_\varepsilon = E\{\varepsilon(n)^2\} = \frac{\sigma_{\Delta T}^2}{T_s^2} E\{[y(n) - y(n-1)]^2\} \cong \frac{\sigma_{\Delta T}^2}{T_s^2} (E\{(x(n) - x(n-1))^2\} + E\{(q(n) - q(n-1))^2\}) \quad (2)$$

where $E\{\cdot\}$ stands for the mathematical expectation [12] and $q(n)$ is the shaped quantization noise, given by:

$$q(z) = N_{TF}(z)e(z) \quad (3)$$

where $N_{TF}(z)$ represents the quantization Noise Transfer Function and $e(z)$ is the quantization error – assumed to be a white noise source.

Considering a sinewave input signal of amplitude A and angular frequency $\omega_i = 2\pi f_i$, $\Delta x_n \equiv [x(n) - x(n-1)]$ can be simplified as:

$$\Delta x_n \cong \frac{d}{dt}x(t)|_{t=nT_s} \cdot T_s = A\omega_i T_s \cos(\omega_i(n-1)T_s) \quad (4)$$

and hence,

$$E\{(\Delta x_n)^2\} = T_s^2 A^2 \omega_i^2 E\{(\cos(\omega_i(n-1)T_s))^2\} = \frac{T_s^2 A^2 \omega_i^2}{2} \quad (5)$$

The expectation value of $\Delta q_n \equiv [q(n) - q(n-1)]$ can be derived from (3) giving:

$$E\{(\Delta q_n)^2\} = E\left\{ \left(Z^{-1}[(1-z^{-1})N_{TF}(z)e(z)] \right)^2 \right\} = \frac{X_{FS}^2}{12\pi(2^B-1)^2} \int_0^\pi |(1-e^{-j\omega})N_{TF}(e^{-j\omega})|^2 d\omega \quad (6)$$

where X_{FS} and B are the full-scale and the internal number of bits of the quantizer, respectively.

From (2), (5) and (6), we obtain:

$$P_\varepsilon \cong \left(\frac{\sigma_{\Delta T}}{T_s} \right)^2 \cdot \left(\frac{A^2 \omega_i^2}{2f_s^2} + \frac{X_{FS}^2}{12\pi(2^B-1)^2} \int_0^\pi |(1-e^{-j\omega})N_{TF}(e^{-j\omega})|^2 d\omega \right) \quad (7)$$

where $f_s \equiv 1/T_s$ is the sampling frequency.

In some modulator topologies, the integration in (7) may become mathematically too complex, thus requiring the use of numerical solving methods. This can be simplified if the state-space formulation is used to derive $E\{(\Delta q_n)^2\}$ as shown in next section.

3. STATE-SPACE FORMULATION

Fig.2 shows the state-space representation of $N_{TF}(z)$, which can be described by the following finite difference equations [12]:

$$\begin{aligned} \overline{v(n+1)}_0 &= \overline{F}_0 \cdot \overline{v(n)}_0 + \overline{p}_0 \cdot e(n) \\ q(n) &= \overline{g}_0^T \cdot \overline{v(n)}_0 + e(n) \end{aligned} \quad (8)$$

where \overline{F}_0 is the state matrix, $\overline{v(n)}_0$ is the $L \times 1$ state vector, \overline{p}_0 and \overline{g}_0 are $L \times 1$ vectors and L is the order of N_{TF} .

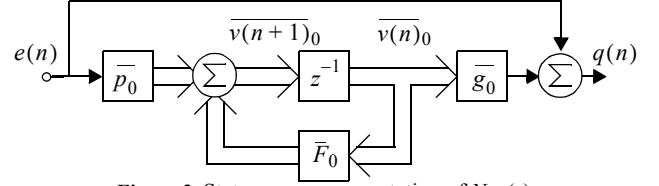


Figure 2. State-space representation of $N_{TF}(z)$.

Equation system (8) can be solved recursively to find the relation between the initial state $\overline{v(n_0)}_0$, previous input ($e(k)$), present input ($e(n)$) and output ($q(n)$) of the system [12]. This gives:

$$q(n) = \overline{g}_0^T \cdot \overline{F}_0^{n-n_0} \cdot \overline{v(n_0)}_0 + \sum_{k=0}^{n-1} \overline{g}_0^T \cdot \overline{F}_0^{n-1-k} \cdot \overline{p}_0 \cdot e(k) + e(n) \quad (9)$$

Assuming that the initial state, $\overline{v(n_0)}_0$, is zero and considering that $E\{e(k)e(j)\} = 0$ for $k \neq j$, it can be shown from (9) that:

$$E\{q^2(n)\} = E\{e^2(n)\} \left(1 + \sum_{k=0}^{n-1} [\overline{g}_0^T \cdot \overline{F}_0^{n-1-k} \cdot \overline{p}_0]^2 \right) \quad (10)$$

Diagonalizing \overline{F}_0 and considering that the system in Fig.2 is stable, the expression in (10) can be re-written as:

$$E\{q(n)^2\} = E\{e(n)^2\} \left(1 - \sum_{k=1}^L \sum_{j=1}^L g_k p_k g_j p_j \frac{\lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right) \quad (11)$$

where λ_i are the eigenvalues of \overline{F}_0 and g_i and p_i are respectively the elements of $\overline{g}^T = \overline{g}_0^T \cdot \overline{T}$ and $\overline{p} = \overline{T}^{-1} \cdot \overline{p}_0$, with \overline{T} being the matrix of the eigenvectors of \overline{F}_0 .

Using a similar procedure, it can be demonstrated that:

$$E\{q(n)q(n-1)\} = E\{e(n)^2\} \left(\overline{g}^T \cdot \overline{p} - \sum_{k=1}^L \sum_{j=1}^L g_k p_k g_j p_j \frac{\lambda_k^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \right) \quad (12)$$

Taking into account that $E\{e(n)^2\} = X_{FS}^2/[12 \cdot (2^B-1)^2]$, and $E\{(q(n))^2\} = E\{(q(n-1))^2\}$, the value of $E\{(\Delta q_n)^2\}$ can be derived from (11) and (12) as:

$$E\{(\Delta q_n)^2\} = 2[E\{(q(n))^2\} - (E\{q(n)q(n-1)\})] = \frac{X_{FS}^2}{6(2^B-1)^2} \cdot \Psi(\overline{g}, \overline{p}, \overline{\lambda}, L) \quad (13)$$

where

$$\Psi(\overline{g}, \overline{p}, \overline{\lambda}, L) = 1 - \overline{g}^T \cdot \overline{p} + \sum_{k=1}^L \sum_{j=1}^L g_k p_k g_j p_j \frac{\lambda_k^{-1} - \lambda_k^{-1} \lambda_j^{-1}}{1 - \lambda_k^{-1} \lambda_j^{-1}} \quad (14)$$

Replacing (6) with (13) in (7) and assuming that the jitter noise is an additive noise source at the input of the modulator, the Signal-to-Noise Ratio (SNR) dominated by jitter can be written as:

$$SNR = \frac{A^2}{B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2 \omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3(2^B-1)^2} \Psi(\overline{g}, \overline{p}, \overline{\lambda}, L) \right]} \quad (15)$$

where B_w is the signal bandwidth.

Note that in the denominator of (15), $(\sigma_{\Delta T})^2$ is multiplied by a factor that is the sum of two terms: one depending on the input signal parameters (A and ω_i) and the other one which is a function of the modulator topology parameters (B , X_{FS} , $\psi(g, p, \lambda, L)$). The first term decreases with f_s while the second term increases with f_s . This is illustrated in Fig.3 where the two terms in brackets in the denominator of (15) are plotted versus f_s for a 5-bit 3rd-order single-loop CT $\Sigma\Delta M$ with $f_i = B_w = 20\text{MHz}$. Note that there is an optimum value of f_s , $f_{sop} = 170\text{MHz}$, that minimizes the in-band jitter noise power and hence, maximizes SNR ^{†3}. Thus, using (15) as a figure of merit in multibit CT $\Sigma\Delta M$ s with NRZ DAC in which jitter is the main limiting factor, the modulator performance can be optimized for given specifications in terms of loop filter parameters, sampling frequency and the number of bits of the internal quantizer.

It is important to mention that the effect of N_{TF} on the in-band jitter noise of multibit NRZ CT $\Sigma\Delta M$ s was previously studied in [7]. However, it did not take into account the impact of signal-dependent jitter term, which can be very critical in broadband applications as illustrated in next section.

4. SIMULATION RESULTS

The presented study has been validated through time-domain behavioural simulation using SIMSIDES, a SIMULINK-based simulator for $\Sigma\Delta M$ s [13]. Fig.4 shows the multibit NRZ CT $\Sigma\Delta M$ s under study. Fig.4(a) is a 3rd-order single-loop and Fig.4(b) is a cascaded 2-1 topology. In both architectures, feed-forward stabilization is used and a feedback coefficient k_r is used to move one of the poles to an optimum position [14]. The modulators were synthesized to handle signals within $B_w = 20\text{MHz}$ for VDSL application.

Three different cases are considered:

- CT $\Sigma\Delta M1$: Fig.4(a) with $f_s = 400\text{MHz}$ and $B = 2$
- CT $\Sigma\Delta M2$: Fig.4(a) with $f_s = 160\text{MHz}$ and $B = 5$
- CT $\Sigma\Delta M3$: Fig.4(b) with $f_s = 160\text{MHz}$ and $B_1 = B_2 = 5$

where B_1 and B_2 are respectively the number of bits of the quantizer in the first- and second- stage in Fig.4(b). Table 1 shows the values of the loop-filter coefficients (k_i) as well as the position of the poles and Table 2 shows the values of g_i , p_i and λ_i for the three cases mentioned above.

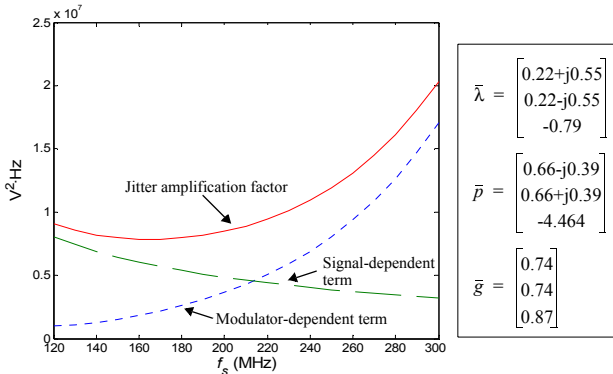


Figure 3. Jitter components vs. f_s for a 5-bit 3rd order CT $\Sigma\Delta M$.

†3. The values of g_i , p_i and λ_i for $f_s = f_{sop} = 170\text{MHz}$ are shown in Fig.3.

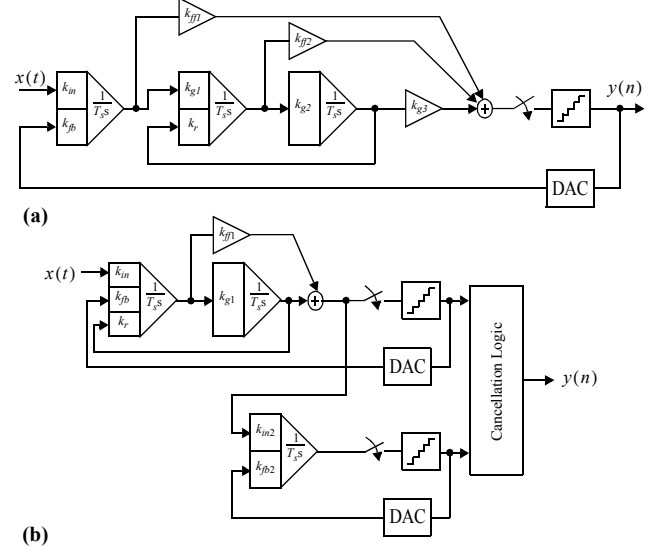


Figure 4. Multibit NRZ CT $\Sigma\Delta M$ s under study. (a) 3rd-order single-loop architecture. (b) Cascaded 2-1 architecture.

Fig.5 shows several simulated output spectra of cases CT $\Sigma\Delta M1$ (Fig.5(a)) and CT $\Sigma\Delta M2$ (Fig.5(b)) corresponding to different values of f_i and $\sigma_{\Delta T} = 25\text{ps}$. Note that in Fig.5(a), the in-band noise power does not depend on f_i as predicted by [7]. However, as B increases from $B = 2$ to $B = 5$, the modulator-dependent term in (15) decreases and hence, the in-band noise is dominated by the signal-dependent term as illustrated in Fig.5(b). This effect is better shown in Fig.6, where the SNR -peak of the modulators in Fig.4 is plotted vs. $\sigma_{\Delta T}$ for several values of f_i , showing simulation results and theoretical predictions^{†4}. For comparison pur-

Table 1: Loop-filter coefficients of CT $\Sigma\Delta M$ s in Fig.4

| | CT $\Sigma\Delta M1$ | CT $\Sigma\Delta M2$ | CT $\Sigma\Delta M3$ |
|-----------|----------------------|--|----------------------|
| k_{in} | 1.5 | 2 | 1.6 |
| k_{fb} | -1.5 | -2 | -1.6 |
| k_{g1} | 1 | 1 | 1.6 |
| k_r | -0.1 | -0.37 | -0.24 |
| k_{g2} | 0.6 | 1 | - |
| k_{g3} | 0.5 | 1.2 | - |
| k_{ff1} | 1 | 1 | 1 |
| k_{ff2} | 0.5 | 1 | - |
| k_{in2} | - | - | 1 |
| k_{fb2} | - | - | -1 |
| Poles | $\omega_1 = 0$ | $\omega_2 = \sqrt{3/5} \cdot 2\pi \cdot B_w$ | |

Table 2: Values of g_i , p_i and λ_i for the CT $\Sigma\Delta M$ s in Fig.4

| | CT $\Sigma\Delta M1$ | CT $\Sigma\Delta M2$ | CT $\Sigma\Delta M3$ |
|-----------------|--|---|--------------------------------|
| $\bar{\lambda}$ | [-0.328 0.664-j0.438 0.664-j0.438] | [0.122+j0.39 0.122-j0.39 -0.667] | [-0.543+j0.64 -0.543-j0.64] |
| \bar{g} | [-0.56 0.853 0.853] | [0.81 0.81 0.959] | [0.766 0.766] |
| \bar{p} | [3.503 0.016-j0.184 0.016+j0.184] | [1.476+j1.722E-3 1.476-j1.722E-3 -5.69] | [-1.78-j1.81 -1.78+j1.81] |

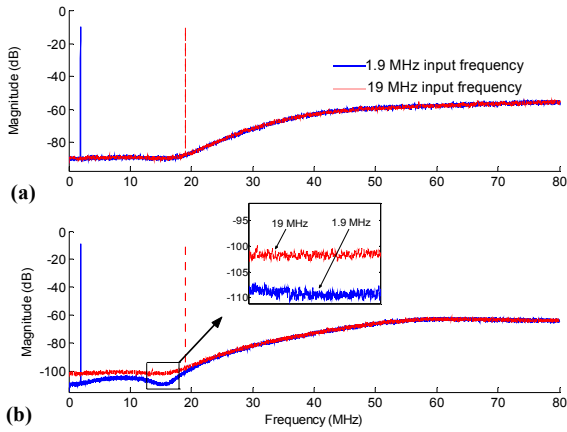


Figure 5. Effect of jitter error on the output spectra of (a) CT $\Sigma\Delta$ M1 and (b) CT $\Sigma\Delta$ M2.

poses, predictions given by [7] are also included. Note that, simulated and theoretical data matched very well when the combined effect of signal- and modulator-dependent jitter noise is taken into account as shown in this work.

CONCLUSIONS

The effect of clock jitter error on multibit CT $\Sigma\Delta$ M with NRZ DAC has been analyzed. Based on the use of state-space formulation, easy-to-compute closed-form expressions have been derived for the noise power and signal-to-noise ratio. It has been demonstrated that the jitter-induced noise has two components: one depending on signal parameters and the other one depending on the modulator loop filter. Their combined effect, not predicted by previous approaches, has been confirmed by time-domain simulations of several CT $\Sigma\Delta$ M intended for VDSL application.

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†4. Expression (15) is replaced in Fig.6 with the ideal value of SNR for $\sigma_{JT} \ll 1$.

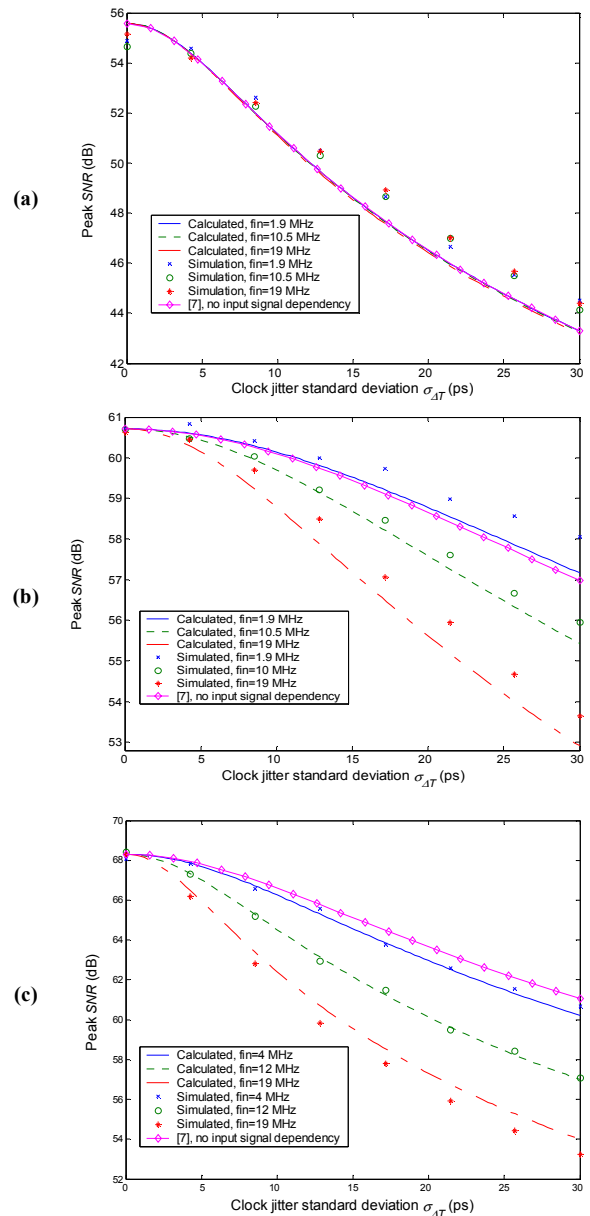


Figure 6. SNR vs. $\sigma_{\Delta T}$ for different values of f_i : (a) CT $\Sigma\Delta$ M1. (b) CT $\Sigma\Delta$ M2. (c) CT $\Sigma\Delta$ M3.

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