AN ALTERNATIVE DFT METHODOLOGY TO TEST HIGH-RESOLUTION ΣΔ MODULATORS

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Abstract

In this paper, a novel DfT methodology to test high-resolution ΣΔ Modulators (ΣΔM) is introduced. The aim of the proposal is to reduce the test time required by conventional methodologies without degrading the accuracy of the results. A detailed description of the additional circuitry needed to perform these tests is presented as well as some initial simulation results to show the utility of the approach.

1.Introduction

Although much effort has been paid in last years to find a practical test methodology for A/D and D/A converters, at the very end, it has become a common practice to use standard FFT techniques for the dynamic test and histogram-based approaches for static test of modulators [1]. Unfortunately, both alternatives require a huge amount of data when the resolution of the *C*ircuits *U*nder *T*est (*CUTs*) is beyond 15 bits. This results in a trade-off among test time and measurement resolution that imposes strong limitations to the test set-up. To alleviate this problem, a new methodology, based on a divide-and-conquer approach is introduced in this paper, paying special attention to the practical circuit implementation.

Although a decomposition of the *CUT* into analog and digital subsystems is, at least a-priory, easy to perform, further decomposition within the analog part is not so direct. However, a basic set of rules can be given:

- Perform the partitioning taking into account the specifications (if some specifications can be propagated to specific subsystems, their control can be performed by only checking the functionality of those subsystems).
- Perform the partitioning in subsystems that are functionally independent of their environment.
- Check that subsystems have non-overlapping functionality.
- Decompose the system into subsystems that can be tested by well-known techniques.
- Carry out the decomposition so that system specifications can be easily mapped into subsystem specifications.
- Carry out the decomposition in a way that testing the subsystems take less time than testing the whole system.

This set of rules justifies that analog macros based on a functional decomposition are natural candidates for test partitioning.

For ΣΔ A/D converters, an obvious decomposition is splitting the system into the analog modulator and the digital decimation filter. However, this level of granularity is not enough when test application time is a critical issue. Testing modulators is a time-consuming task and should be desirable a finer decomposition of the modulator.

2.Reference test circuit and test methods

The methodology proposed in this paper is based on the idea that a proper decomposition of the modulator into several blocks can be used to reduce the time involved in the test of the whole structure. It is expected that an adequate test of the critical blocks in the modulator should reduce dramatically both the test time and the test complexity, offering also the possibility to detect the sources of errors that affect the circuit performance, thus, providing the ways to correct these faults.

Working out different decomposition schemes will also require to combine with another ideas, for instance with the use of Sw-Opamps or any other multiplexing scheme.

To determine the quality of the proposed test approaches, a sensor-interface ΣΔM will be used as the circuit reference. The circuit has been implemented following a cascade 2-1 architecture as shown in Fig. 1, under the specifications described below:

- Resolution: DR = 17bits, SNR_{peak} > 100dB
- Digital output rate: 40kSample/s
- Signal bandwidth= B_w = (0.1Hz-20kHz)
- Temperature range: from -40^{o}C to 175^{o}C
- Minimum power consumption

According to the set of rules given above a number of critical blocks can be identified:

- First, from all the integrators, dominating error sources arise mainly due to the first one. Therefore, an exhaustive test to control the first integrator quality will be of great interest.
- Second, although the quantiser non-idealities are attenuated by the gain of the integrators, a test to check the performance of this block will enable the detection of faults during the fabrication of the modulator.
- Third, the last block to be tested should be the DAC. This test is specially critical for multi-bit quantisers. However, this is not the case here, so this test should not be further considered.

Taking into account these results, three test proposal should be

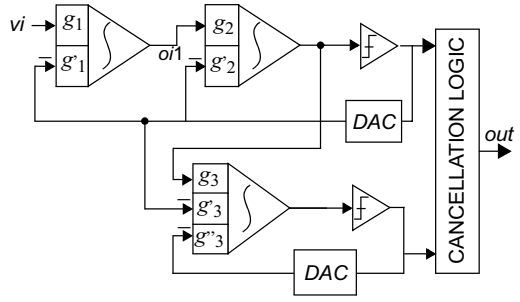

Figure 1. Block diagram of a 2-1 cascade ΣΔ Modulator.

defined and are described now on.

2.1. Test of the first integrator

A methodology to detect the source of errors that degrade the circuit performance due to errors in the first integrator could be the following:

- First, the first integrator is converted into an amplifier.
- Second, the two remaining integrators are connected to form a second order ΣΔM.
- Third, the input signal is connected to the input of the first integrator (now amplifier) and, after a delay, connected to the negative input of the second order ΣΔM. Thus, the second order ΣΔM will process the error signal generated by the non-ideal performance of the first integrator.

These steps are illustrated in Fig. 2.

Three different sources of errors can be detected using this architecture:

- **DC gain errors**: using a pulse-coded input with very low frequency to eliminate the influence of the settling error, the error signal detected at node *oi*1 will include information about the finite gain of the amplifier.

  If the *I*n-*B*and-*N*oise (*IBN*) power is measured for the 2nd order modulator and the filter only, this *IBN* at the output of the reconfigured modulator can be compared to the one obtained when the amplifier is included in the circuit. This comparison enables the possibility to generate a signature to decide if the DC gain error of the first amplifier is or not within the tolerance limits.
- **Settling error**: with the same structure, now increasing the frequency of the input signal, it is possible to care for the error introduced by the settling of the amplifier. Again, a measure of the *IBN* with and without the input amplifier allows to generate a signature with an ambiguity set of two elements (DC gain error and settling of the first amplifier).

The influence of the DC gain and settling errors has been simulated using ASIDES [2], and preliminary results are shown in Fig. 3(a).

- **Thermal noise**: if the input signal is a sine wave with small amplitude and low frequency, by decreasing the frequency sampling of the integration capacitor it is possible to increase the contribution of the thermal noise significantly, thus enabling its direct measurement at the output node. The initial results of this simulation are also shown in Fig. 3(b).

2.2. Test for the quantiser

In the case of a single bit, the quantiser block is reduced to a comparator. This kind of circuits has errors dominated by their input offset and hysteresis. However, due to the location into the modulator topology, these error sources are largely attenuated by the DC gain of the integrators. In spite of this, to enable the isolated test of the first integrator it is important to check that the quantisation error is accurately bounded. To this end, accessible nodes have to become available in the circuit, following the approach in Fig. 4. Then, if the modulator input is set to zero and a test signal (sine-wave stimulus) is applied, this will result in an output where the quantisation noise can be observed by performing an FFT analysis with a reduced set of samples. To make accessible this node, the application of the Sw-Opamp concept described in the next section will be of great interest. An example of the resulting test is given in Fig. 5 for 16384 samples from the bitstream.

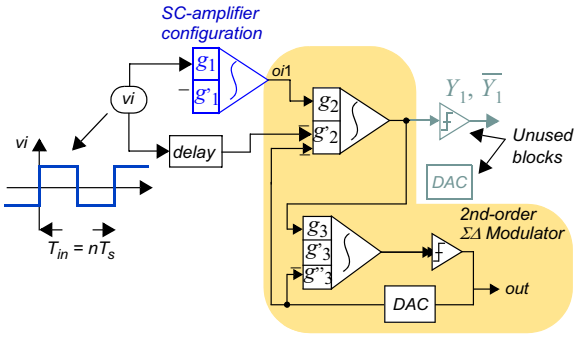

Figure 2. Testing the performance of the first integrator.

2.3. Signal path degradation

An alternative to the methodology described before, is related to allow the observability of some critical nodes to detect the correct operation of the modulator. For the case under study, the critical nodes are located at the output of each integrator. If a buffer is added to these nodes and an additional input is added to the circuit to make it switch between *test* and *normal* operation mode, the signals at those nodes can be observed. This alternative is illustrated in Fig. 6.

3.Building blocks for DfT

As introduced in Section 2, some circuitry has to be added to the

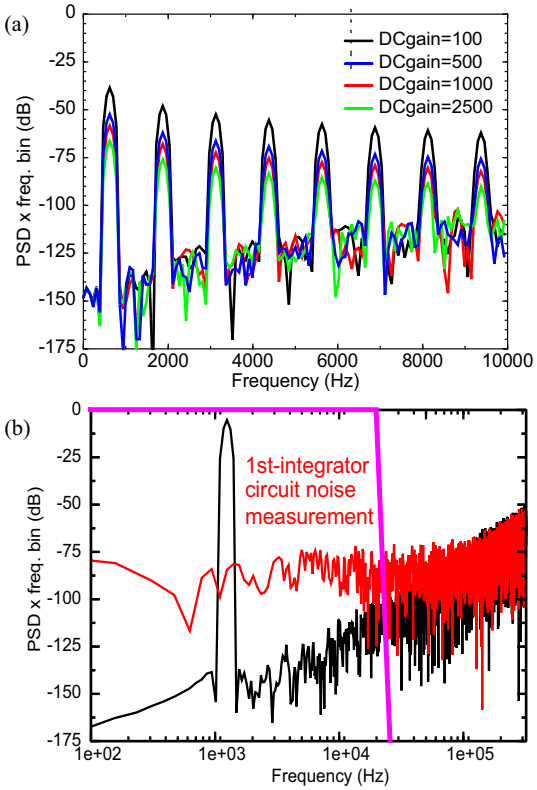

Figure 3. DC gain errors and noise for the first integrator.

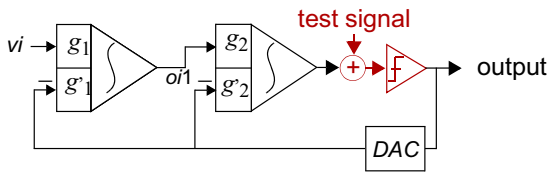

Figure 4. Test signal injection into the Quantiser.

modulator itself in order to allow the different test methodologies. The most critical circuits are those that affect in some way to the signal path. Thus, the output buffers to control the propagation and degradation of the signal through the integrators and the Sw-Opamps within each integrator have been carefully designed to minimize the degradation of the normal operation.

3.1. Analog output buffers

The internal architecture of a buffer able to cope with the low-degradation requirements is shown in Fig. 7.

The specifications achieved by this buffer are:

- DC Gain: -0.03 dB
- f_{-3dB}: 30.9 MHz (with 10 pF output load)
- Power: 0.68 mW

It is important to point out that this kind of blocks can be used as parametrisable library cells to be added to the circuit which is desired to test.

3.2. Sw-Opamps

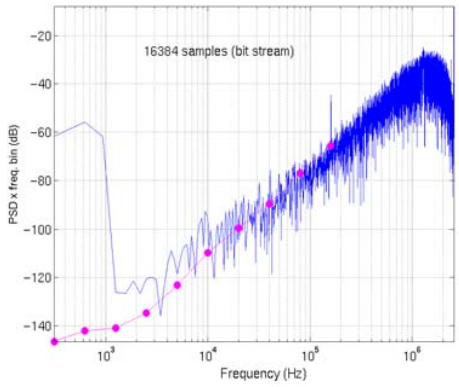

Figure 5. Noise transfer function evaluation.

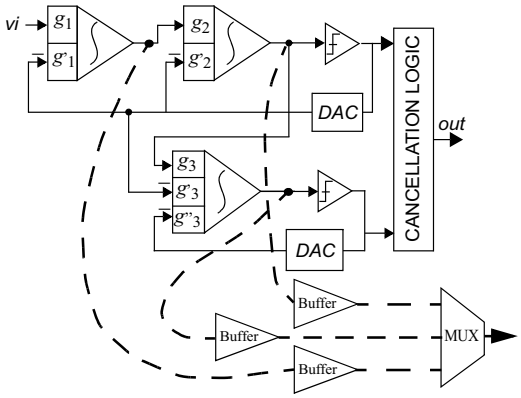

Figure 6. Using buffers to access to internal nodes.

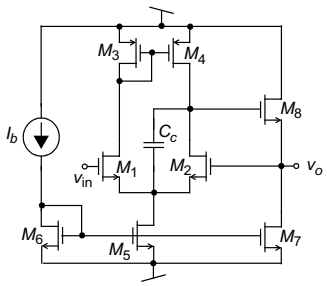

Figure 7. Analog buffer proposed for test objectives.

The idea here [3],[4], is to separate the link between the analogue blocks and the test stimuli by changing the operational amplifiers used for integration purposes by Sw-Opamps, where two different input stages, controlled by a digital signal, allow that the amplifier works in *normal* or in *test* mode.

A way to carry all this task in an efficient, yet simple manner, is to use Sw-Opamps. They essentially consist of operational amplifiers in which the differential input pair has been duplicated, thus providing two operational modes, commanded by a digital control signal:

- *Normal Mode*: the circuit operates as an opamp, with a differential input and a single-ended (or differential if required) output.
- *Buffer Mode*: the circuit acts as a buffer, where the signal present at an extra terminal is passed to the output, isolating in this mode the regular input signal.

This is illustrated in Fig. 8.

To enable this modification, the differential input pair of the amplifier has to be duplicated and connected to the remaining circuitry by means of switches that controls the operation mode. Then, a digital control decides if the operation of the amplifier is *test mode* or *normal mode*.

Although this operation can be performed by simply inserting the switches as shown in Fig. 9, this alternative will result in a significant degradation of the circuit performance due to the parasitic resistance caused by S_1, S_2 in the signal path.

The key point here is to design an Sw-Opamp that minimizes the impact on the circuit performance, power dissipation and area consumption by inserting the switches in appropriate places.

In Fig. 10 two alternatives are shown, as introduced in [5]. The first one requires eight switches external to the amplifier, while the second one requires four internal switches. In both cases the increase of area is very small. Also, the power consumption should not be increased since the two operation modes involve the same structure.

Three HSPICE simulations have been done to compare the original behaviour (amplifier without a Sw-concept) with the alternatives proposed in Fig. 10.

The results of this comparison is summarized in Table 1 for the folded-cascode opamp in Fig. 10, where the first row corresponds

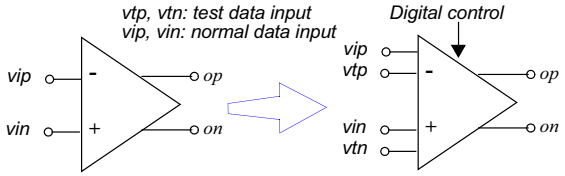

Figure 8. Basic integrator and SW-Opamp concept.

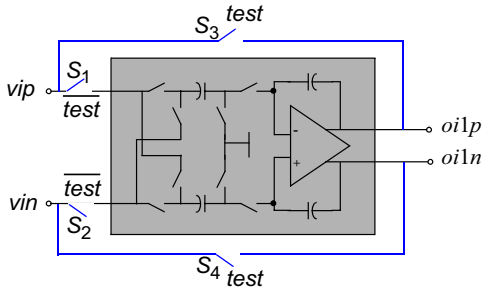

Figure 9. Insertion of switches.

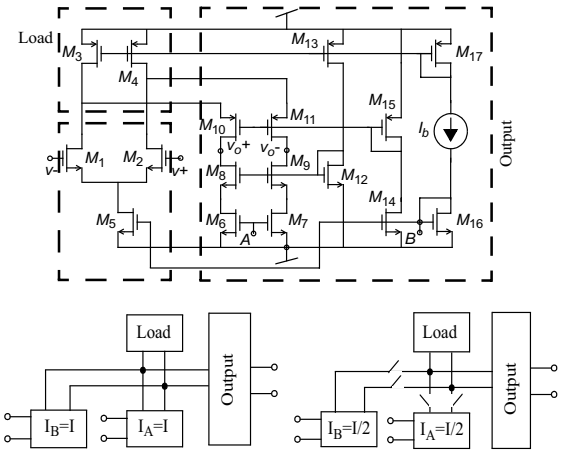

Figure 10. Folded-cascode opamp and possible sw-opamp alternatives.

to the original behaviour (*Ref*), the second to the alternative using internal switches (*in-sw*) and the third one to the alternative based on inserting external switches (*ex-sw*).

Table 1. Degradation caused by the sw-concept.

	A_0 (dB)	GB (MHz)	PM (deg)	SR (V/µs)	Area (µm²)	Power (mW)
Ref	72.62	22.67	86.98	21.71	50.86	7.95
in-sw	72.61	22.59	84.49	21.71	51.6	7.96
ex-sw	72.54	22.52	86.43	21.71	51.6	7.94

It can be seen from the simulations how the original behaviour is very slightly varied by the inclusion of the additional circuitry.

The final implementation of the first amplifier including the Sw-Opamp concept is shown in Fig. 11.

Also, in Table 2, the simulation results including information about the comparison of the worst-case behaviour in all the corners tested for the operational amplifiers, are shown.

Table 2. Worst case operations for first and second (third) amplifiers with and without Sw-Opamp architectures.

	WC (1st)	WC (1st SW-OP)	WC (2nd)	WC (2nd SW-OP)
a0 (dB)	71.09	69.93	65.13	64.51
gb (MHz)	13.99	13.73	21.08	20.55
PM (º)	85.50	83.33	82.61	76.45
SR (V/µs)	21.10	20.21	30.23	29.90
os (V)	5.02	5.01	4.99	4.99
power (mW)	7.24	7.78	2.48	3.06

Finally, the operation of the circuit in *buffer mode* has been tested

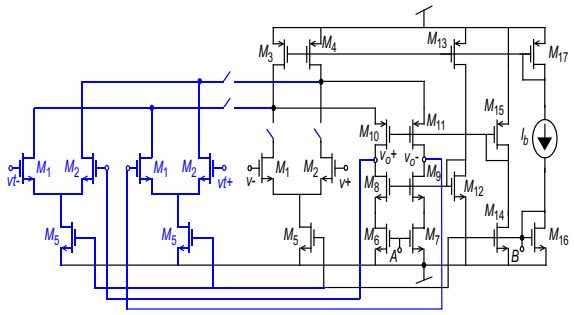

Figure 11. Sw-Opamp final architecture.

to ensure that the resolution is enough to propagate the stimulus signal without affecting the test results. The outcome of this test is shown below:

- First Sw-amplifier HD_3 = -104.81 dB (17.47 bits)[1]
- Second Sw-amplifier HD_3 = -101.67 dB (16.95 bits)

4.Layout

The layout of the prototype including the DfT circuitry is shown in Fig. 12. The DfT circuitry is highlighted in the Figure, showing that the area overhead is small as compared with the total area of the prototype. This prototype has been sent to fabrication and it is expected that, in some weeks, practical experimental results will be obtained.

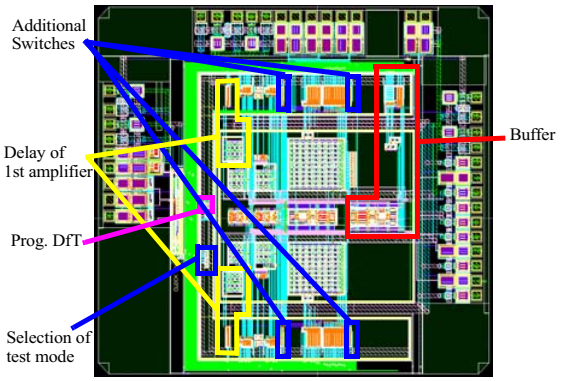

Figure 12. Layout of the ΣΔM including DfT circuitry.

5.Conclusions

In this paper, several alternatives to the DfT of high-resolution ΣΔ modulators that depart from the usual techniques are introduced. Circuit details are given on how to implement the different methodologies proposed and preliminary simulation results are shown while final experimental results are generated.

References

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1. HD_3 is the most dominant distortion term due to the differential architecture chosen for the amplifiers.