Asynchronous spiking pixel with programmable sensitivity to illumination

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Abstract— **A spiking pixel to be used in image sensor arrays for asynchronous frame-based operation is presented. The pixel features both local and global adaptive sensitivity to the illumination level. Local adaptation is performed by adjusting the voltage stored in an embedded analog memory according to the average illumination within a neighborhood. Global adaptation to the overall illumination of the array is implemented by adjusting a voltage value common to all the pixels. These programming capabilities allow full control on the sensor sensitivity, pixel output data flow, and energy consumption, thus, ovecoming the limitations oberved in current image sensors based on spiking pixels. Experimental results validate the functionality of the proposal.**

Index terms – **Integrate and fire pixels, AER, Light adaptation, Image sensors, Spiking pixels.** [1]

I. INTRODUCTION

Asynchronous luminance spiking sensors [1]–[3] consist of pixels that fire with a frequency proportional to the illumination level. Such systems can outperform classic frame-based image sensors in terms of dynamic range, latency and bandwidth consumption and, accordingly, they target application scenarios where these features are preferred over image quality [4], [5].

Current spiking sensors are not able to locally adapt to light, as occurs in biological vision systems [6], [7]. On the contrary, they can only be globally adjusted by setting a common bias parameter. This, however, poses a trade-off between sensitivity and the amount of data to be handled. In order to detect the spiking activity of pixels exposed to low illumination levels, the overall system sensitivity should be large thus leading to large spiking rates in pixels operating under high illumination conditions. In medium and large pixel arrays, the total event rate which can be processed by the readout circuitry is limited (e.g., modern asynchronous arbitration systems can tolerate spiking rates in the order of 20Meps [8]) and, therefore, the global sensor sensitivity to light cannot be made arbitrarily large to extend the dynamic range and expose darker regions.

To overcome this trade-off, it would be desirable to locally adapt the sensitivity of low illuminated pixels to reduce their latency without increasing the firing activity of pixels under higher illumination values. Further, it would be also beneficial to keep the possibility of global adaptation to control the total data throughout and the bandwidth and power consumption requirements.

Emerging 3D fabrication technologies facilitate the design of pixels with processing capabilities on the focal plane and allow higher programmability without degrading the pixel fill factor [9], [10]. In this scenario, analog memories are key components to store local pixel parameters or to incorporate on-chip intelligence [11]. Memories can be placed on tiers below/above the sensing photodiode without degrading the fill factor. The reported pixel, with an in-pixel analog memory, is an example of how these novel technologies could be exploited efficiently to make event-driven luminance sensors more competitive.

In this article, we analyze the performance of a spiking pixel that implements global and local adaptation to light intensity. Local adaptation is accomplished by storing a voltage reference on an in-pixel memory implemented with a floating diffusion capacitance [11]. The presented pixel is intended for a new generation of image sensors that combine frame-based processing with asynchronous operation to increase dynamic range [3]. In this paper, we focus on the asynchronous operation and the local and global adaptation to light intensity. Experimental results obtained with a prototype pixel implemented in a 180nm HV fabrication process are reported. These results validate the proposed approach.

II. PIXEL'S OPERATION

Fig. 1 shows the proposed pixel architecture. Main building blocks are highlighted with different colors. One block (surrounded with a red dashed line) performs asynchronous light-to-frequency conversion. It generate spikes, i.e., trains of pulses with a frequency proportional to illumination. Another block (surrounded with a green dashed line) is used to store the integration voltage, $V_c(t)$, on the floating diffusion capacitance FD_2, whenever the control signal SH is enabled. Finally, the circuit surrounded with a blue dashed line is an asynchronous logic block to read the pixel outputs.

The pixel has two possible operation modes: High Dynamic Range (HDR) and octopus [3]. In both cases, the pixel operation starts after a global reset period during which the voltage in the integration capacitance C_1 is cleared.
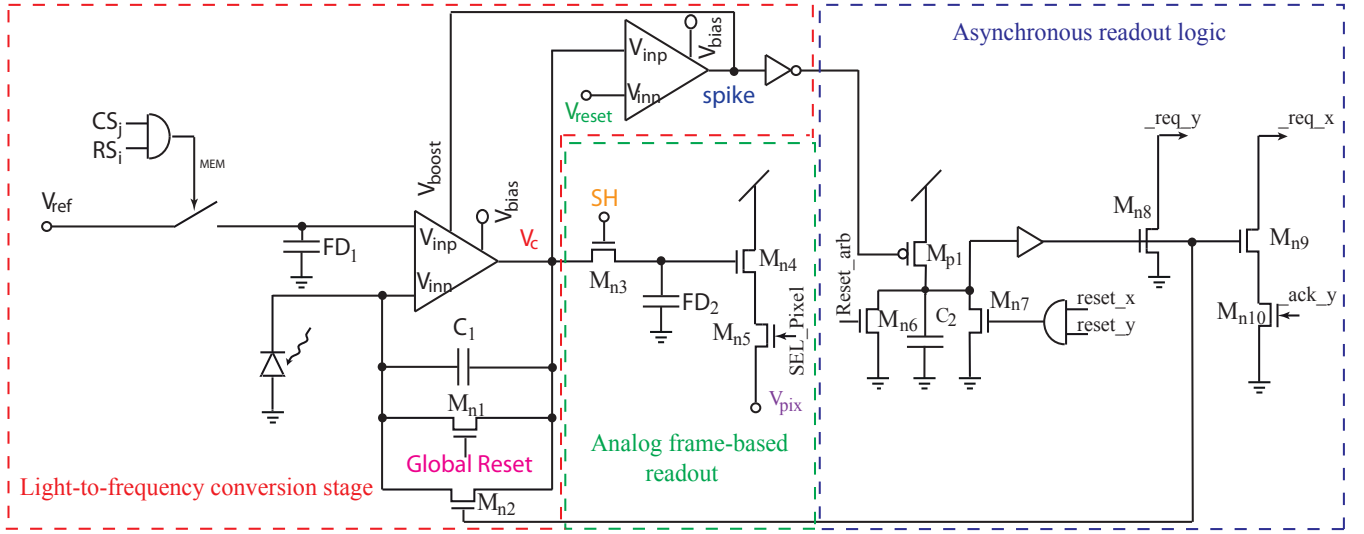
Fig. 1. Pixel's schematics. Main functional blocks are highlighted. The blocks surrounded by a red and a blue dash line are involved in spike generation and spike communication, respectively. The block surrounded by a green dash line is activated to operate in the HDR mode. It is used to read the voltage at the integration capacitance C_1, at the end of the integration period, T_{int}. Transistor sizes are (W/L, µm/µm): $M_{n1}=M_{n2}=M_{n3}=M_{n5}=M_{n6}=M_{n9}=M_{n10}=0.5/0.7$, $M_{n4}=1/0.5$, $M_{p1}=0.5/1$, $M_{n8}=1/0.7$, $C_1=35fF$, $FD_1=45fF$, $FD_1=C_2=30f$.

In the HDR mode, operation is defined by an user-defined integration time, T_{int}, as shown in Fig. 2. During this period, the number of pixel over-exposures (spikes) are transmitted and stored off-chip. To assure good linearity, voltage V_{reset} should be higher than the transistor threshold voltage, V_T, in the selected technology. Once the integration time is over, signal *SH* is enabled and voltage $V_c(T_{int})$ is stored on the floating diffusion capacitance FD_2. A source follower, formed by transistor M_{n4} and a biasing transistor shared by columns in a prospective pixel array (not shown in Fig. 1), buffers the voltage at FD_2 and obtains the analog output V_{pix}, whenever the pixel is selected. Finally, voltage V_{pix} is digitized with a ramp ADC shared by all the pixels per column, as done in a prior implementation using the same technology [3]. Illumination values can be encoded by linearly combining the result of the ADC conversion (less significant bits) and the number of generated spikes (more significant bits).

In the octopus mode, there is no defined integration time and the control signal *SH* is always disabled. Hence, circuit operation is continuous an the pixel spikes asynchronously with a frequency proportional to light intensity. Analyzing the light-to-frequency conversion block, it can be easily demonstrated that the spiking frequency is given by:

$$f_{osc} \approx \frac{I_{ph}}{C_1 \cdot (V_{reset} - V_{ref})} = \frac{I_{ph}}{C_1 \cdot \Delta V} \qquad (1)$$

where C_1 is the integration capacitance and I_{ph} is the photodiode current. In this mode, images are encoded taking into account the average spiking frequency within an observation interval. To transmit the spikes, the asynchronous communication Address Event Representation (AER) protocol is used [12], [13]. The in-pixel asynchronous circuitry needed to transmit spikes is shown in Fig. 1 (block surrounded by a blue dashed line). This circuit was already implemented in
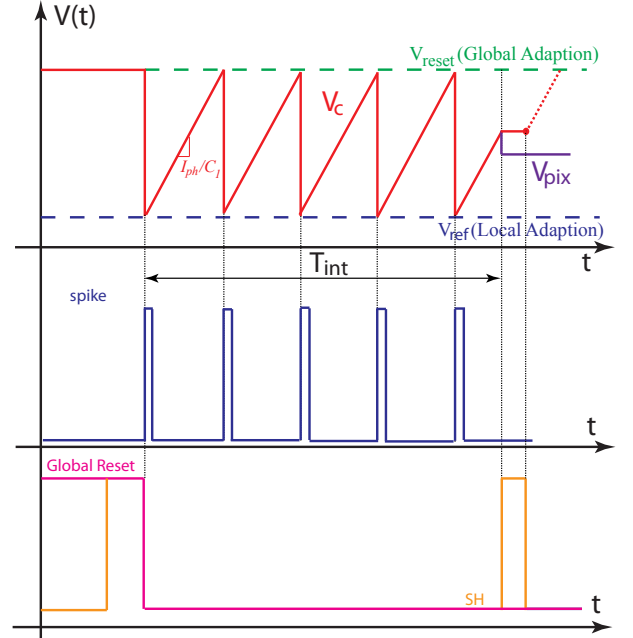

Fig. 2. Timing diagram of the pixel operating in the HDR mode. Initially, signal *Global Reset* is enabled to reset the voltages at C_1 and FD_2. Then, the voltage $V_c(t)$ rises with a slope proportional to illumination. Events are transmitted asynchronously every time that $V_c(t)$ reaches the value V_{reset}. When signal *SH* is on, voltage $V_c(t)$ is stored on FD_2 (analog readout).

prior designs [3], [14], [15] in conjunction with an external arbitration circuitry to handle the entire pixel array [16].

In this study, the focus is on the control of the spiking frequency of the light-to-frequency conversion block (module surrounded by a red dashed line in Fig. 1) assuming that pixel operation is asynchronous and continuous. Hence, unless otherwise stated, it is assumed the octopus operation mode.

The block has been devised to allow both local and global adaption to light intensity.

After monitoring the overall system event rate, global adaptation is implemented by tuning the analog voltage V_{reset}, shared by all the pixels of a prospective pixel array. By increasing its value, the spiking frequency decreases, thus avoiding the risk of event overrun, at the expense of increasing the sensor latency globally. As shown in Fig. 2, the maximum value of signal $V_c(t)$ is set by V_{reset}.

In some situations, local adaptation can be found useful to reduce the pixel latency of low illuminated regions. This can be done by controlling the analog voltage V_{ref}. This voltage is stored in an in-pixel analog memory which is implemented with a floating diffusion capacitance (FD_1). The higher the voltage V_{ref}, the lower the pixel latency. With the dedicated peripheral circuitry (shown in Section III), different values of V_{ref} can be set on each pixel. The target is to equalize the pixel array latency dynamically. Pixels with lower spike rates can be tuned to provide faster response to illumination. As will be shown, the tuning procedure is implemented with an ad-hoc synchronous logic, without interrupting the asynchronous in-pixel light-to-frequency conversion.

Fig. 3 shows the schematic of the OTA used in Fig. 1. It is a two-stage Miller compensated OTA. Transistor M_{n4} boots the bias current of the OTA if the pixel is about to reset the integrator (*spike* signal becomes active). The comparator in Fig. 1 is implemented in a similar manner, but the Miller capacitance and the boost transistor are eliminated to save pixel area. The boosting mechanism operates as follows: if the voltage at the integration capacitance C_1 is below the voltage threshold V_{reset}, the boost transistor is disabled and the OTA is biased with a small current of 90nA to minimize the static power consumption. If the voltage at the integration capacitance reaches the voltage threshold V_{reset}, the boost transistor is temporarily on until the asynchronous readout logic enables transistor M_{n2}. The arbitration hand-shaking cycle lasts typically below 100ns [8] since the signal *spike* becomes active. Hence, the boost transistor is active during a short amount of time, just to speed up the reset of the integration capacitance.

III. Pixel's Control Circuitry

Fig. 4 shows the circuit used to locally program the reference voltage, V_{ref}, per pixel. The pixel matrix readout circuitry is not displayed for simplicity. Circuit operation is controlled by an external FPGA or microntroller attached to the sensor. On the bottom, a column selection block sequentially addresses the columns CS_j, $j = 0, \ldots, N-1$, where N is the number of columns of the sensor array. Only one column can be enabled at a time. The row selection block on the left addresses the rows RS_i, $i = 0, \ldots, M-1$, where M is the number of rows of the sensor array. In this case, different rows can be activated simultaneously.

The V_{ref} voltages are generated by a K-bit DAC controlled by the external FPGA or microcontroller. This latter is also responsible to define the V_{ref} value per pixel, depending on the desired sensitivity to light and data throughput. For each
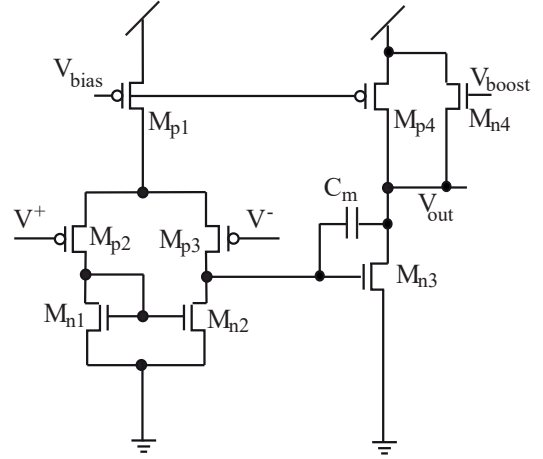

Fig. 3. Schematic of the in-pixel OTA. Transistor M_{n4} increases the bias current when the pixel is being self-reset. C_m and M_{n4} are not present in the comparator's design. Transistor sizes are (W/L, μm/μm): $M_{p1} = M_{p4} = 1/1$, $M_{p2} = M_{p3} = M_{n1} = M_{n2} = M_{n4} = 1/0.7$. $M_{n3} = 3/0.7$. The Miller capacitance amounts C_m = 40fF.
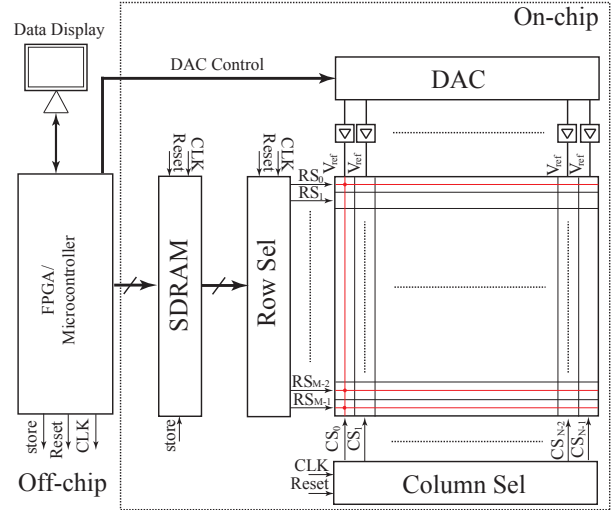

Fig. 4. Pixel matrix and digital circuitry devised to program the pixel values of the V_{ref} voltage. The column selector block selects sequentially the pixel columns. The row selection block selects simultaneously all the pixels that operate with the same V_{ref} value (red lines in the figure). The V_{ref} values that correspond to each pixel are stored on-chip on a SDRAM memory. All the possible values of V_{ref} are sequentially generated with a DAC.

selected column, all the possible values of V_{ref} are swept sequentially. The row selection block activates those rows for which pixels operate with the same V_{ref} reference. A SDRAM memory stores the DAC programming words associated to the different V_{ref} values. This information is transferred to the external FPGA/microcontroller and it is updated every time that a new column is selected.

The programming procedure is illustrated in the timing diagram of Fig. 5. First, the pixels of the first column, $j = 0$, are selected by activating the signal CS_0. While CS_0 is on, the different values of V_{ref} are swept and set by the DAC. Signals RS_i are active whenever the V_{ref} value that corresponds to the pixel $(i, 0)$ is set. The same operation is repeated column
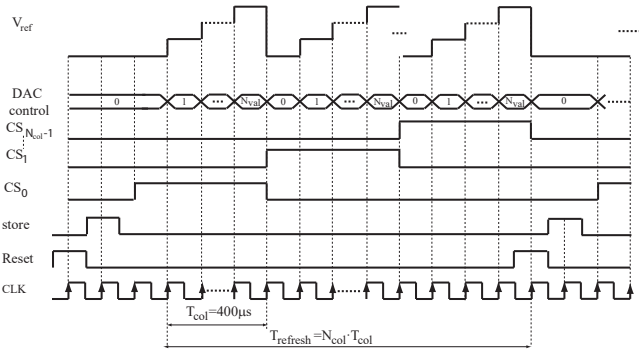
Fig. 5. Time sequence with the digital signals involved in the programming of the different V_{ref} voltages. The amount of time to refresh or program all the V_{ref} values of a pixel column is T_{col}.

Fig. 6. Proposed resistive DAC implementation to generate the V_{ref} values.

by column until all the in-pixel FD_1 memories are updated.

A resistor-string architecture is proposed for the DAC. It is shown in Fig. 6. Every column uses an individual buffer to drive the internal memories of the selected pixels. The resistor string is biased between voltages V_{top} and V_{bot}. On the one hand, V_{top} should be lower than V_{reset}, otherwise, if they were similar, the spiking frequency would be quite large. On the other, V_{bot} should be higher than the threshold voltage of transistor M_{n4} in Fig. 1 to assure the linearity of the pixel response.

Fig. 7 illustrates how the pixel spiking frequency can be adjusted by varying the V_{ref} value. In the figure, V_{reset} is set to 4V and voltage V_{ref} is varied from 0.5 to 4V. The rest of parameters in (1) are kept constant. Two different DAC resolutions, $K = 4$ and $K = 8$, have been considered. In both cases, voltages V_{bot} and V_{top} were set to 0.5V and 4V, respectively. The relative spiking frequencies span almost three decades with the 8-bit DAC, and more than one decade with the 4-bit DAC. In practice, a 4-bit DAC can give enough programming flexibility with the added benefits of reduced complexity and fast operation speed.

It is worth observing that while the peripheral readout circuit per pixel operates in an asynchronus manner, the control circuit for selecting, programming, and storing in local memories the V_{ref} settings is essentially synchronous. The strategy for making both operations compatible has been described in detail in a previous work [3].

IV. PIXELS' PROGRAMMABILITY PROCEDURE

The FPGA or microcontroller of Fig. 4 implements a control algorithm for selecting and adjusting the local in-pixel V_{ref} voltages of the pixel array. The goal is to equalize the pixel output frequencies. Let us assume that the average target pixel spiking frequency for the whole array is f_{avg}. The procedure for updating the V_{ref} values per pixel is as follows:

1) Calculate the average spiking rate $\overline{f_{i,j}}$, $i = 0, \ldots, M-1$ and $j = 0, \ldots, N-1$, for every pixel in the array during an observation interval. This is done by keeping track of the number of spikes which are transmitted through the AER protocol from every coordinates (i, j) of the array.
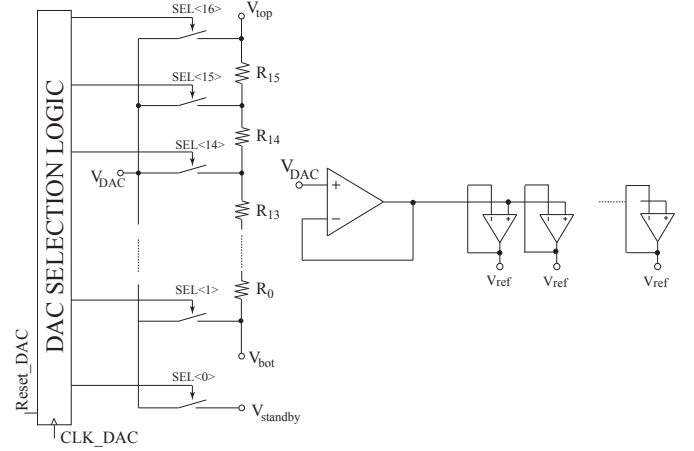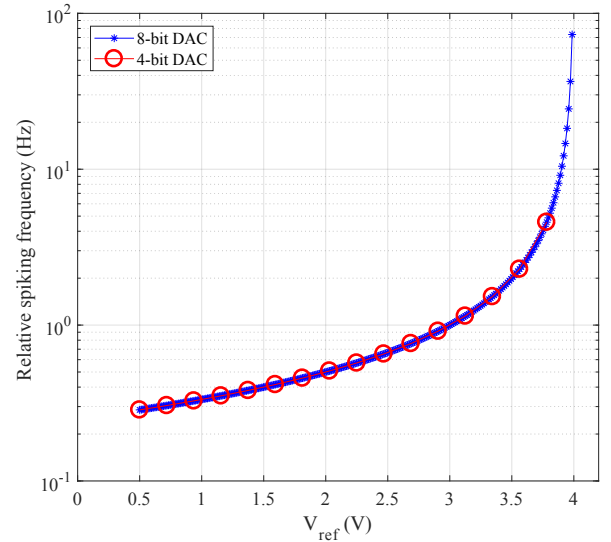

Fig. 7. Pixel spiking frequency versus V_{ref} voltage. The V_{reset} voltage is set to 4V and V_{ref} is swept using an 8-bit and a 4-bit DAC.

As mentioned, The $\overline{f_{i,j}}$ value depends on the locally stored voltage $V_{ref_{i,j}}$ and the global voltage V_{reset}.

2) If the average spiking frequency of the pixel with coordinates (i, j) exceeds a fraction α of the target frequency, i.e., if $\overline{f_{i,j}} > \alpha \cdot f_{avg}$, the DAC is adjusted so that the updated reference voltage $V'_{ref_{i,j}}$ amounts:

$$V'_{ref_{i,j}} \leftarrow \left\lfloor \frac{V_{ref_{i,j}} \cdot f_{avg}}{\overline{f_{i,j}}} \right\rfloor \quad (2)$$

where $\lfloor \cdot \rfloor$ denotes the next available value lower than the argument.

3) If the average spiking frequency of the pixel with coordinates (i, j) is lower than a fraction β of the target frequency, i.e., if $\overline{f_{i,j}} < \beta \cdot f_{avg}$, the reference voltage $V_{ref_{i,j}}$ is updated as

TABLE I

MAIN FEATURES OF THE PIXEL

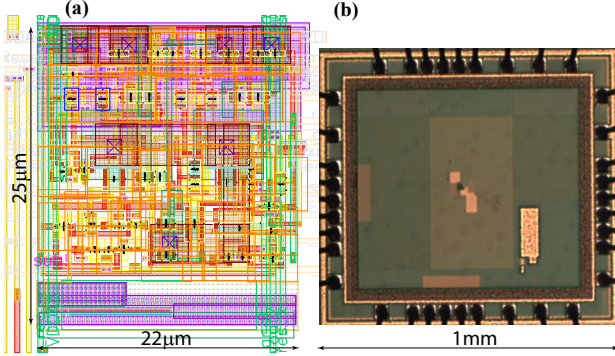| Technology	AMS 0.18μm HV
Power Supply	5V
Pixel Size	25μm × 22μm
Pixel Complexity	45 Transistors + 5 Capacitors
Fill Factor	6.25%
Dynamic Range	>120dB
Analog power consumption	450nA
Pixel sensitivity to light	1.76 pulses / $\Delta V \cdot$ lux
Temporal noise	1.1%
Chip to chip spiking f deviation	1.3%
Sense Node Capacitance	35fF

Fig. 8. (a) Pixel layout. Vertical and horizontal metal lines are arranged to assemble with the neighbouring pixels. Its dimensions are 22μm × 25 μm. (b) Microphotograph of the fabricated chip containing one prototype pixel, its biasing circuitry, and two scan buffers.

$$V'_{ref_{i,j}} \leftarrow \left\lceil \frac{V_{ref_{i,j}} \cdot f_{avg}}{\overline{f_{i,j}}} \right\rceil \qquad (3)$$

where $\lceil \cdot \rceil$ denotes the next available value higher than the argument.

4) If the average spiking frequency of the pixel with coordinates (i,j) is comprised between the above limits, i.e., if $\beta \cdot f_{avg} < \overline{f_{i,j}} < \alpha \cdot f_{avg}$, the reference voltage keeps the previous value,

$$V'_{ref_{i,j}} \leftarrow V_{ref_{i,j}} \qquad (4)$$

Of course, although the procedure has been described for individual pixels, the same approach can be followed if groups of pixels are collectivelly updated. Indeed, this helps to alleviate the computational burden and speed up the process of in-pixel sensitivity programming.

V. PIXEL'S EXPERIMENTAL CHARACTERIZATION

A dedicated chip in a standard 180nm HV technology has been fabricated. In Fig. 8(a) the pixel layout is depicted.

Its dimensions are $25 \times 22\mu m^2$. A chip photograph is displayed in Fig. 8(b). It contains one pixel prototype, the external analog biasing circuitry for its operation, two analog buffers [17] to scan the analog voltages $V_c(t)$ and $V_{pix}(t)$, and logic to handle the pixel asynchronous readout. The main features of the proposed pixel are summarized in Table I.
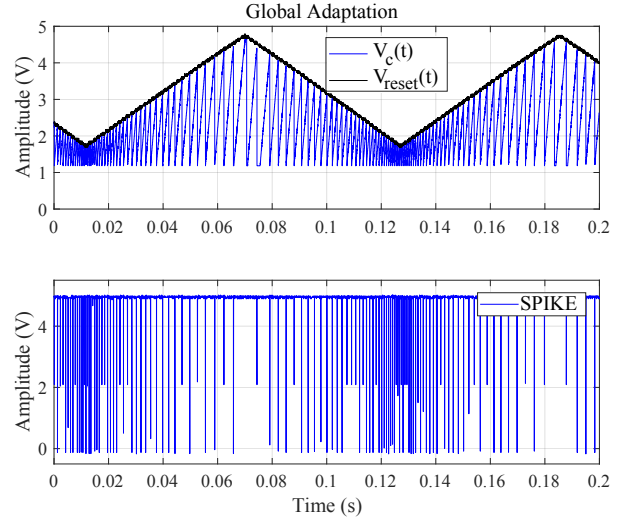

Fig. 9. Top: Effect of the global adaptation parameter V_{reset} on the voltage V_c at the integration capacitance C_1. Bottom: pulses fired by the pixel.
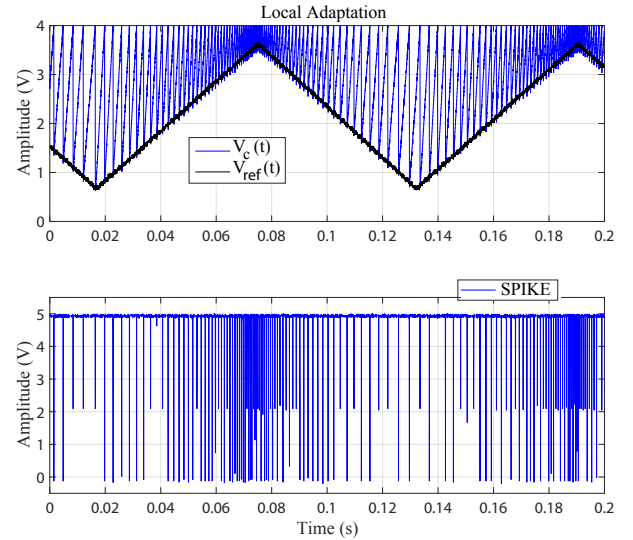

Fig. 10. Top: Effect of the local adaptation parameter V_{ref} on the voltage V_c at the integration capacitance C_1. Bottom: pulses fired by the pixel.

A. Local and global adaptation to light

In order to test the global adaption to light, the voltage V_{reset} has been linearly swept and voltages V_c and *spike* have been recorded under constant illumination conditions. Plots are shown in Fig. 9. Note that the pixel firing frequency decreases for large V_{reset} values.

Similarly, the local adaptation to light has been tested by sweeping the value of V_{ref}. Results are displayed in Fig. 10. In this case, the recorded spiking frequency increases with V_{ref}.

B. Memory leakage impact

Fig. 11 illustrates how the leakage from the diffusion capacitance FD_1 affects the voltage V_c at the integration capacitance of the pixel and, hence, the performance of the
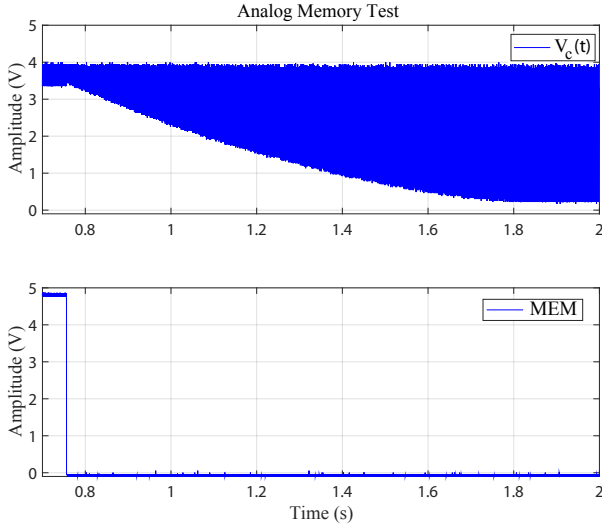
Fig. 11. Test of the impact of the leakage from the analog memory FD_1. After storing a V_{ref} value, the pixel is operated continuously without refreshing the memory to gauge the transient voltage variation of V_c.

Fig. 12. Pixel sensitivity to light measured interms of the spiking frequency for different chip illuminance values.

local pixel adaptation to light. This effect is of major relevance as it implies a trade-off between the maximum time slot during which voltage V_{ref} can be stored without refreshing and the size of the diffusion capacitor. In the presented design, the measured analog memory leakage is $L =3.34$ mV/ms.

Assuming a 4-bit DAC and a clock operation speed of $f_{clk} = 100$MHz, the time interval allocated to sweep the V_{ref} values in one column is $T_{col} = 2^K/f_{clk} = 1.6$µs. In a pixel array with $N = 256$ columns, the V_{ref} values can be thus refreshed or reprogrammed every $T_{refresh} = N \times T_{col} = 0.4$ms. Considering that the minimum voltage excursion is $\Delta V = V_{reset_{min}} - V_{ref_{max}} = 0.5$V, the worst-case relative error due to memory leakage is given by

$$\epsilon\,(\%) = \frac{T_{refresh} \cdot L}{\Delta V_{max}} \quad (5)$$

which amounts 2.7% with the proposed pixel circuit.

C. Pixel sensitivity to light and dynamic range

Fig. 12 shows the pixel sensitivity to light. The plot is obtained by calculating the spiking rate for different illumination values. Together with the measured results, the plot also includes a linear data fitting (in red). The pixel exhibits a linear response to illumination over five decades, in accordance to (1). In the experiment, $\Delta = V_{reset} - V_{ref} =3.7$V and the obtained pixel sensitivity is 1.76 pulses/ΔV· lux.

The pixel dynamic range can be computed as the ratio between the maximum and the minimum photocurrent that can be measured during a time interval:

$$DR_{dB} = 20\log_{10}\left(\frac{I_{ph_{max}}}{I_{ph_{min}}}\right) \quad (6)$$

Examining the experimental data of Fig. 12 and considering that the pixel photocurrent is proportional to illumination, it
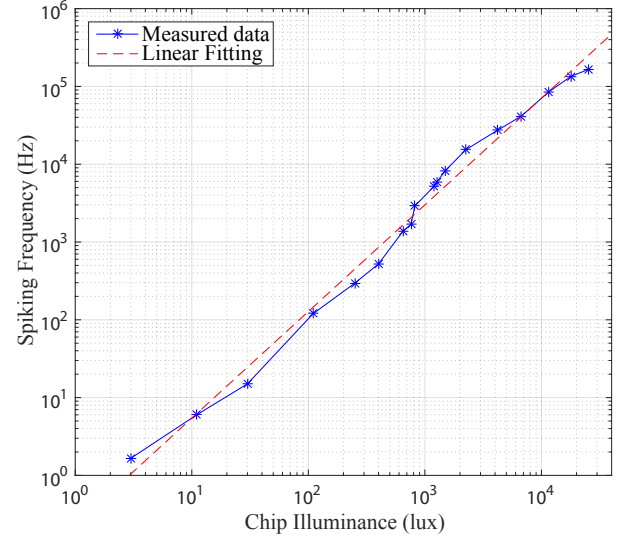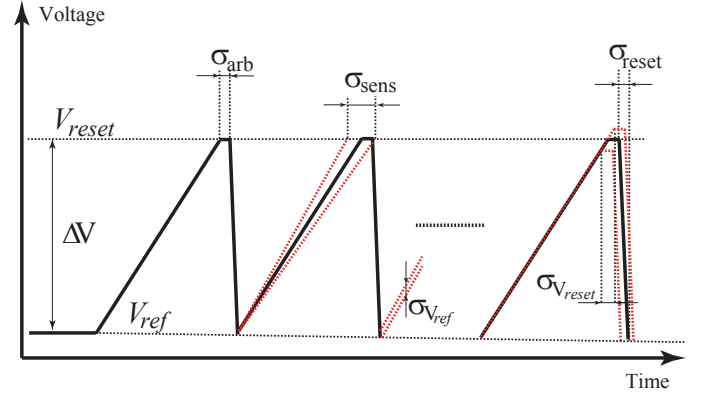

Fig. 13. Illustration of the impact that the different noise sources have on the voltage at the integration capacitance, V_c. The error induced by each noise source in the spiking performance is indicated.

can be deduced that the sensor is able to linearly encode illumination levels spanning for more than four decades.

In HDR mode, the dynamic range can be increased beyond 120dB, as it is discussed in a prior work [3]. In this mode, the voltage variation at the integration capacitance can be digitized with an external ADC and, hence, the effictive ΔV necessary to encode one illumination value is lower.

D. Noise sources

Fig. 13 illustrates the impact of the main error sources on the light-to-frequency conversion performance. There are two types of noise sources: static and dynamic. Static noise sources are due to inter-pixel design parameter deviations. Dynamic noise sources are due to the AER arbitration logic, as well as, to thermal and shot noise contributions. As shown in Fig. 13, both types of noise sources cause inter-pixel frequency oscillation variations.

The dominant static noise sources are:

a) Variations of the comparator's threshold ($\sigma_{V_{reset}}$) cause that integration capacitances in the array are not reset at the same voltage value.

b) Inter-pixel variations of the well capacitance and the integration capacitance affects the pixel sensitivity [see (1)]. This leads to slope variations (σ_{sens}) in the transient voltage at the integration capacitance.

c) Variations of the analog memories capacitances FD_1 ($\sigma_{V_{ref}}$). This creates mismatch between the effective V_{ref} voltages stored on each pixel.

d) Variations on the time required to discharge the integration capacitance (σ_{reset}). Transistor mismatch in the differential pair of the OTA in Fig. 3 and inter-pixel variations of the integration capacitance are the main responsible for this behaviour.

The dominant dynamic noise sources are:

a) The AER arbitration logic [8] introduces transient delays (σ_{arb}) in the time needed to re-start the pixel operation when the voltage at the integration capacitance reaches the voltage threshold V_{reset}. Such delays mainly depend on the global pixel activity. If the AER communication logic is not congested, typical arbitration delays are below 100ns [8], [12]. According to the measurement results of Fig. 12, pixel spiking frequencies with high illumination are normally below 100Khz. Thus, the error introduced by the arbitration logic is not usually significant.

b) Thermal and shot noise cause random variations in the V_c voltage that affect the pixel oscillation frequency.

The overall pixel temporal noise (TN), due to the dynamic noise sources, has been measured by exposing the pixel to a constant illumination of 400lux and gauging the time intervals between consecutive spikes during 10s. TN is computed as

$$TN = \frac{\sum\limits_{k=1}^{Q} \sqrt{\left(f_k - \bar{f}\right)^2}}{Q \cdot \bar{f}} = \frac{\sigma_f}{\bar{f}} \qquad (7)$$

where f_k is the measured spiking frequency between two consecutive spikes at the k-th time interval, Q is the number of spikes generated by the pixel during the 10s time window, and $\bar{f}$ is the average spiking frequency during the entire observation window. The measured TN value is 1.1%.

The inter-pixel frequency deviation introduced by static noise sources has been also tested. For a given illumination value, the average spiking frequencies have been measured on ten different chips. The obtained chip to chip spiking frequency deviation is 1.3%.

E. HDR mode readout test

Fig. 14 illustrates the pixel performance in HDR mode. In this mode, after an integration time, T_{int}, $V_c(T_{int})$ is transferred to a floating diffusion capacitance FD_2, when the control signal SH is active. Fig. 14 shows the buffered version, V_{pix}, of the voltage stored on FD_2 for different values of $V_c(t)$. As shown in Fig. 1, the buffer consists in a source follower with the biasing transistor placed off-pixel as it is intended to be shared by all the pixels in a column.
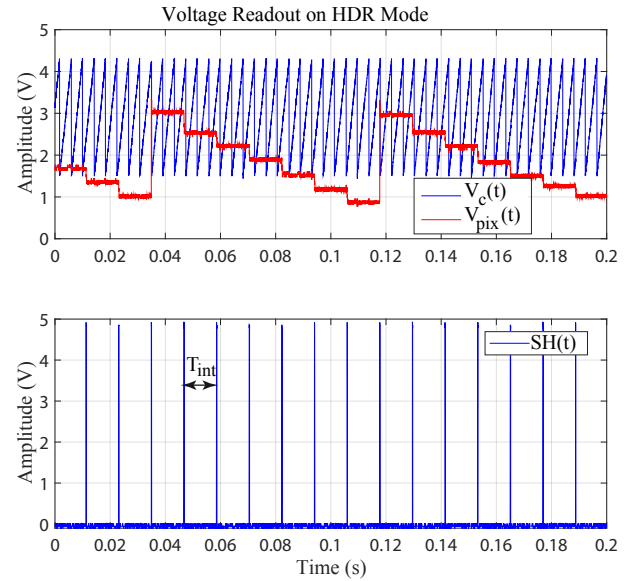

Fig. 14. Test of the pixel analog readout in the HDR mode. Pixel analog voltage V_{pix} is stored on the diffusion capacitance FD_2 at the end of an integration time, T_{int}, by enabling the signal SH. In the experiment, V_{ref} =1.5V and V_{reset} =4.3V.

F. System scalability considerations

In terms of scalability, the main limitation of event-based luminance sensors is the arbitration speed of the AER logic. As it is shown in Fig. 12, the pixel spiking frequency increases linearly with illumination. If the global event rate in a pixel array exceeds the maximum event rate that can be handled by the arbitration logic, random delays are introduced in the pixel spiking period [8]. This limits the dynamic range and, hence, the maximum illumination value that can be measured. Furthermore, spiking frequency variations increase noise (σ_{arb} contribution in Fig. 13). Thus, the proposed technique to adapt locally the sensitivity to light benefits scalability. Further, by reducing the sensitivity of highly illuminated regions, the data load to be processed by the AER logic is minimized.

VI. FAST PIXEL LUMINANCE ESTIMATION

One relevant question is how to conveniently set the local V_{ref} voltages in the pixel array, the first time the sensor is initiated. On the one hand, if a low illuminated pixel stores initially a very low value of V_{ref}, its response latency will be very slow and transient illumination changes might be undetected because of the low pixel sensitivity. On the other, if the V_{ref} values are set initially close to V_{reset}, the pixel sensitivity will be high and the pixel response will be fast, however, the global event rate may saturate the arbitration logic [8] and the power consumption of the sensor will be very large until the algorithm steps down the V_{ref} voltages for the higher illuminated pixels. This suggests the convenience to count on a fast procedure for estimating the pixel illumination and, eventually, reprogram the V_{ref} voltages. In particular, it could be useful in environments where the illumination levels within the visual scene change at high speed. If the illumination levels are not known, it is difficult to achieve a
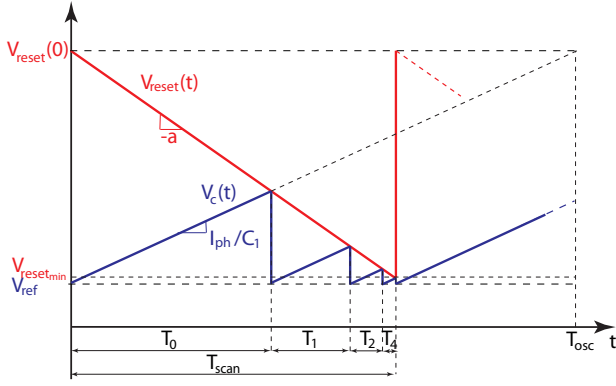
Fig. 15. Proposed method to gauge the illumination levels. The analog voltage V_{reset} (red trace), shared by all the pixels, is swept between two values during a time interval of duration T_{scan}. The transient V_c voltage at the integration capacitance is shown in blue. Pixel spiking frequency increases when the V_{reset} voltage is close to V_{ref}. By determining the ratio between two time intervals associated to the reception of two consecutive spikes, T_n/T_{n-s}, the photocurrent value can be determined.

good balance between sensitivity and data throughput if the V_{ref} values are arbitrarily defined.

To program the pixel sensitivity to light in such situations, the authors advanced in a prior publication [18] a procedure to obtain a fast estimation of the pixel luminance without increasing the global event rate significantly. The idea is to force a response (at least two spikes) for all the pixels within a user-defined time interval, T_{scan}. Initially, all the pixels store the same value of V_{ref} and are reset. Then, the V_{reset} voltage, that is shared by all the pixels of the array, is swept as it is depicted in Fig. 15. It starts from the value V_{reset_0}. Then, it decreases with a slope, $-a$, until it reaches the final value $V_{reset_{min}}$. Whenever the V_{reset} value is close to V_{ref}, pixels exposed to low illumination will be forced to fire during T_{scan}. By processing the events received during this interval, it is possible to gauge pixels illumination levels.

Before receiving the first spike, $t < T_0$, we can express the transient voltages $V_{reset}(t)$ and $V_c(t)$ as follows:

$$V_c(t) = V_{ref} + \frac{I_{ph} \cdot t}{C_1} \qquad (8)$$

$$V_{reset}(t) = V_{reset_0} - a \cdot t \qquad (9)$$

Using (8) and (9), the first spike time stamp, T_0, and the voltage value $V_c(T_0) = V_{reset}(T_0)$ can be determined as

$$T_0 = \frac{V_{reset_0} - V_{ref}}{a + \frac{I_{ph}}{C_1}} \qquad (10)$$

$$V_{reset}(T_0) = V_{reset_0} - a \cdot T_0 \qquad (11)$$

Similarly, T_1 and $V_{ref}(T_1)$ are given by

$$T_1 = \frac{V_{reset}(T_0) - V_{ref}}{a + \frac{I_{ph}}{C_1}} \qquad (12)$$

$$V_{reset}(T_1) = V_{reset_0} - a \cdot (T_0 + T_1) \qquad (13)$$

These equations can be generalized to obtain $V_{reset}(T_n)$ and T_n, for $n > 1$, as

$$
\begin{aligned}
T_n &= \frac{V_{reset}(T_{n-1}) - V_{ref}}{a + \frac{I_{ph}}{C_1}} = \\
&= T_0 - \frac{a(T_0 + T_1 + ... + T_{n-1})}{a + \frac{I_{ph}}{C_1}} = \\
&= T_0 - A \cdot (T_0 + T_1 + ... + T_{n-1})
\end{aligned}
\qquad (14)
$$

$$V_{reset}(T_n) = V_{reset_0} - a \cdot (T_0 + T_1 + ... + T_n) \qquad (15)$$

where $A = \frac{a}{a + I_{ph}/C_1} < 1$. From (14), a general expression for T_n, as a function of T_0 can be derived:

$$
\begin{aligned}
T_0 &= T_0 \\
T_1 &= T_0 - AT_0 = (1 - A)T_0 \\
T_2 &= A(T_0 + T_1) = (1 - A)^2 T_0 \\
&\vdots \quad = \quad \vdots \\
T_n &= (1 - A)^n \cdot T_0
\end{aligned}
\qquad (16)
$$

where $0 < 1 - A < 1$ and

$$\lim_{n \to \infty} T_n = T_0 \lim_{n \to \infty} (1 - A)^n = 0 \qquad (17)$$

Hence, from (16), we can state that the ratio between two consecutive time intervals is constant and depends on I_{ph}:

$$\frac{T_n}{T_{n-1}} = (1 - A) \qquad (18)$$

The proposed method is mainly targeted for a fast measurement of low illuminated regions. For these pixels, the slope of $V_{reset}(t)$ is much higher than the slope of $V_c(t)$, i.e. $a >> I_{ph}/C_1$, with $I_{ph}/C_1 < 1$. Thus, the ratio between two consecutive time intervals is approximately constant and depends on the photocurrent value, I_{ph}:

$$A = \frac{a}{a + I_{ph}/C_1} \approx 1 - \frac{I_{ph}}{a \cdot C_1} \qquad (19)$$

$$\frac{T_n}{T_{n-1}} = (1 - A) \approx \frac{I_{ph}}{a \cdot C_1} \qquad (20)$$

Therefore, only two spikes fired by a pixel are required to estimate its illumination. The proposed method achieves a good balance between the amount of time required for the measurement and bandwidth consumption. Pixels sensitivity is increased progressively to avoid saturating the arbitration logic. The duration of the time interval T_{scan} can be adjusted varying the value of the slope, $-a$.

In Fig. 16, measurements taken with one pixel after sweeping the V_{reset} voltage are shown. The pixel has been exposed to uniform and constant illumination. On top, transient voltages $V_{reset}(t)$ and $V_C(t)$ are displayed. In the middle plot, the time stamps that correspond to each spike are plotted. At time instant T_n, $V_{reset}(T_n) = V_C(T_n)$ and the pixel fires. As expected, the ratio between consecutive time intervals T_n/T_{n-1} is approximately constant and lower than one. Variations are mainly due to the arbitrary delays introduced
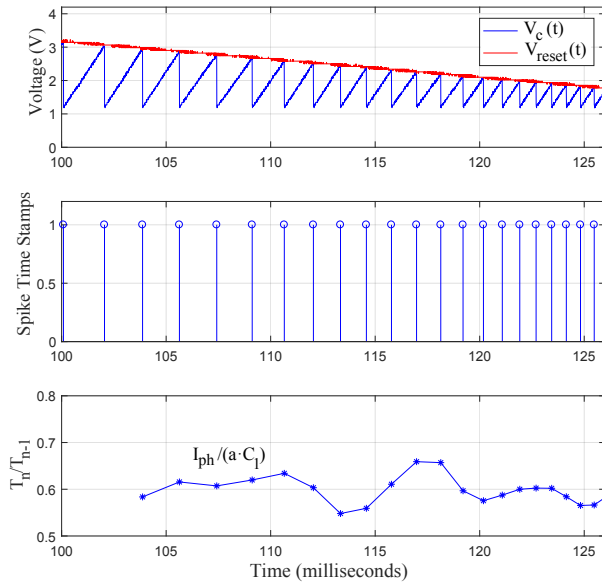
Fig. 16. Estimation of the pixel photocurrent sweeping the V_{ref} voltage. Top: Transient voltages $V_{reset}(t)$ and $V_c(t)$ are plotted. Middle plot: Time stamps of the different spikes fired by the pixel. Every time that $V_{reset}(t)$ voltage reaches the voltage value at the pixel integration capacitance $V_c(t)$, the pixel spikes and resets the $V_c(t)$ voltage. Bottom plot: Ratio between consecutive spikes time stamps. The ratio should be constant and proportional to the photocurrent value.

by the asynchronous communication logic. The reception of two spikes is required to determine the photocurrent value. If a pixel fires more than twice during T_{scan}, results can be improved by averaging the ratios, T_n/T_{n-1}. In the example, T_{scan} is set to 25ms. This value can be programmed depending on the latency requirements.

VII. CONCLUSIONS

The capabilities of a new spiking pixel prototype have been presented and analyzed. It implements both global and local control of the pixel sensitivity to light. Thus, the proposal overcomes a classic limitation of asynchronous sensors based on a light-to-frequency conversion: local adaptation to light is not available for increasing the sensitivity to light in poorly illuminated pixels or regions. Local adaptation is implemented by storing a voltage threshold parameter on an in-pixel diffusion capacitance. The technique increases the dynamic range when a time limit to render images is established. The proposed pixel is compatible with the mixed frame-based and event-based pixel HDR operation previously proposed by the authors. As future work, a whole pixel array, together with the required external control circuitry, will be fabricated and tested.

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