Real-Time Inter-Frame Histogram Builder for SPAD Image Sensors

Ion Vornicu, Ricardo Carmona-Galán, *Senior Member, IEEE*, and Ángel Rodríguez-Vázquez, *Fellow, IEEE*

***Abstract*— CMOS image sensors based on single-photon avalanche-diodes (SPAD) are suitable for 2D and 3D vision. Limited by uncorrelated noise and/or low illumination conditions, image capturing becomes nearly impossible in a single-shot exposure time. Moreover, the depth accuracy is affected by jitter. Therefore, many frames need to be taken to reconstruct the final accurate image. The proposed reconstruction algorithm is based on pixel-wise histogram building. Specifically, a histogram is built on the fly for each pixel of the array from the ongoing acquired frames. This paper presents the design and implementation on FPGA of a real-time pixel-wise inter-frame histogram builder at 1 kfps. The design has been proven with a 64 × 64-pixels SPAD camera. Its remarkable robustness has been demonstrated in harsh conditions, such as 42 kHz of dark count rate (DCR) and high background illumination up to 20 times larger than the DCR. The system has a graphic user interface for 2D/3D imager configuration, image streaming, and pixel-wise histogram streaming.**

***Index Terms*— 2D/3D SPAD image sensor, 2D/3D real-time inter-frame histogram builder, in-pixel TDC, direct ToF.**

I. Introduction

CMOS image sensors based on **S**ingle-**P**hoton **A**valanche-**D**iodes (SPAD) have been proved for photon counting and **T**ime-**o**f-**F**light (ToF) [1]. CMOS technologies for SPADs experienced a remarkable improvement in the last years [2], [3]. Comparing to the integration photodiodes of a conventional CMOS or CDD image sensor, SPADs are able to work in very low illumination conditions with small integration times. This feature makes them suitable for very high frame rate imagers [4].

Due to limited **P**hoton **D**etection **E**fficiency (PDE) and large amount of uncorrelated noise such as **D**ark **C**ount **R**ate (DCR) and background illumination, accurate image capturing in a single shot exposition time is hardly possible especially in low illumination conditions. The solution is to take more measurements to build the final image (frame). From now on, these measurements will be addressed as *inter-frames*.

Although simple to implement, averaging the inter-frames is not a good option when the detectors have a large amount of uncorrelated noise [5]. Instead, the temporal histogram approach based on ripple counters is more suitable [6], [7]. However it cannot be scaled for larger pixel value depth and array sizes. Our proposal is to build a histogram for each pixel of the array directly into a **S**ynchronous **D**ynamic **R**andom-**A**ccess **M**emory (SDRAM) (see Fig. 1).

The inter-frames in raw format could be acquired at the imager's full speed and sent to PC through a fast USB-link. Later on the histograms are built off-line in software. This would require a huge amount of data transfer and storage and a quite large processing time. For instance, let us consider a 64 × 64-pixels SPAD image sensor with in-pixel TDC on 11bits [8]. The number of inter-frames used to build the histograms is 100k. The memory footprint on the computer's hard drive is about 2.4GB. In this case, the total time-lapse to reconstruct the final image in Matlab is about 8 minutes. The computer's physical memory occupation is 6GB and 8 cores at 2.7GHz processor usage is 12%. These figures are not acceptable for a video frame rate. Therefore the inter-frames histogram building becomes a challenge.

This work presents a real-time pixel-wise **i**nter-**f**rame **H**istogram **B**uilder (ifHB) at 1kfps. Therefore the image reconstruction takes place on the fly, simultaneously with pixel-by-pixel inter-frames reading. The proposed circuit has no time penalty for the reconstructed images and decreases the required frame memory footprint by 1000 times. The circuit is implemented on FPGA, also containing the control signals of the SPAD imager and fast USB-link data reading.

The paper is organized as follows: Section II describes the design of the ifHB implemented on FPGA. Section III proves the reliability of the proposed design by testing it with a SPAD camera (SPADCAM). It has a graphical user interface (GUI) built in Matlab for 2D/3D image and inter-frame histogram streaming. Section IV concentrates on the extrapolation and portability of the design for ultra-high frame rate SPAD imagers. Section V is dedicated to conclusions and future work.

II. ifHB Building Blocks

The design of the real-time ifHB includes: SPAD imager controller, clock generator, image acquisition controller, histogram controller, 16MB of SDRAM, SDRAM controller

Manuscript received October 13, 2017; revised November 23, 2017; accepted December 12, 2017. Date of publication December 18, 2017; date of current version January 18, 2018. This work was supported in part by the Office of Naval Research, USA, under Grant N000141410355, in part by the Spanish Ministry of Economy under Project TEC2015-66878-C3-1-R (European Region Development Fund, ERDF/FEDER), and in part by the Junta de Andalucía, Consejería de Economía, Innovación, Ciencia y Empleo under Grant P12-TIC 2338. The associate editor coordinating the review of this paper and approving it for publication was Prof. Y. T. Liao. *(Corresponding author: Ion Vornicu.)*

The authors are with the Instituto de Microelectrónica de Sevilla, Consejo Superior de Investigaciones Cientficas-Universidad de Sevilla, 41092 Sevilla, Spain (e-mail: ivornicu@imse-cnm.csic.es; rcarmona@imse-cnm.csic.es; angel@imse-cnm.csic.es).

Digital Object Identifier 10.1109/JSEN.2017.2784484

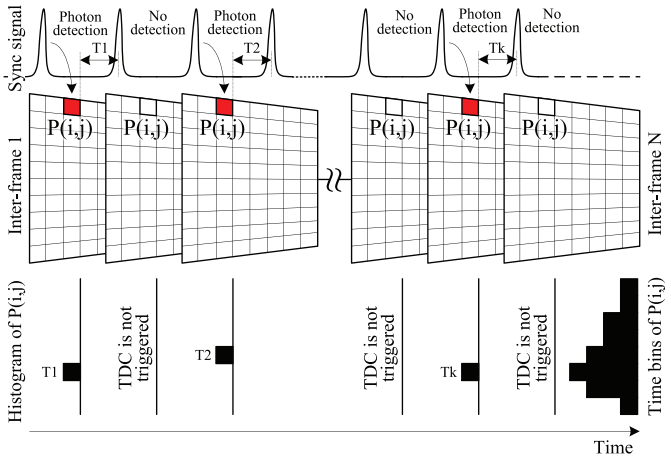

Fig. 1. Block diagram of inter-frame histogram building.

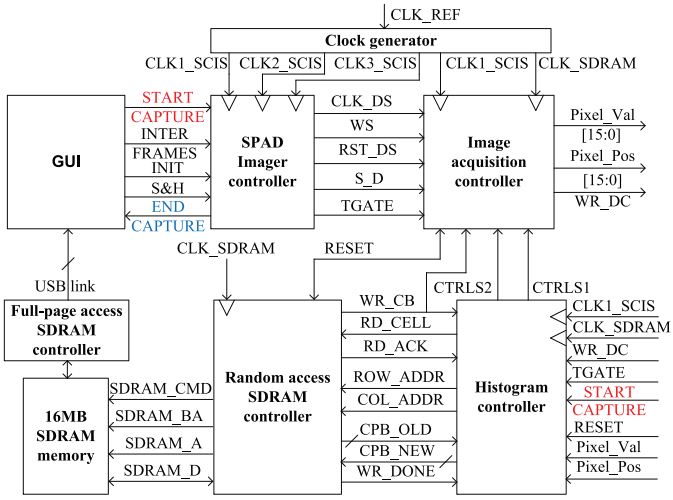

Fig. 2. Block diagram of the ifHB.

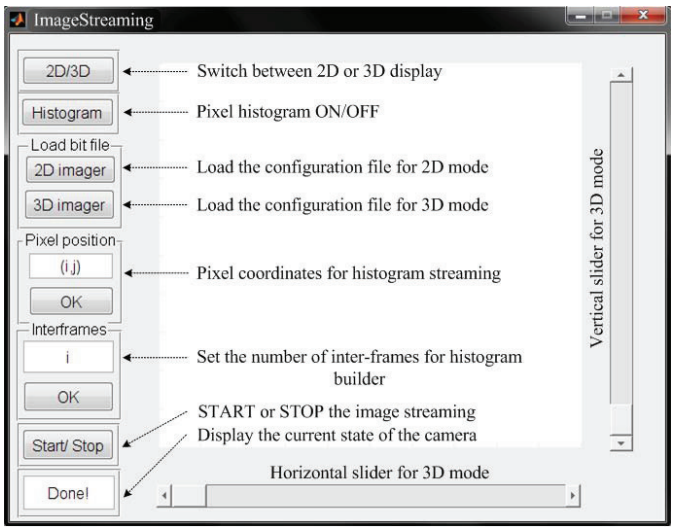

Fig. 3. GUI.

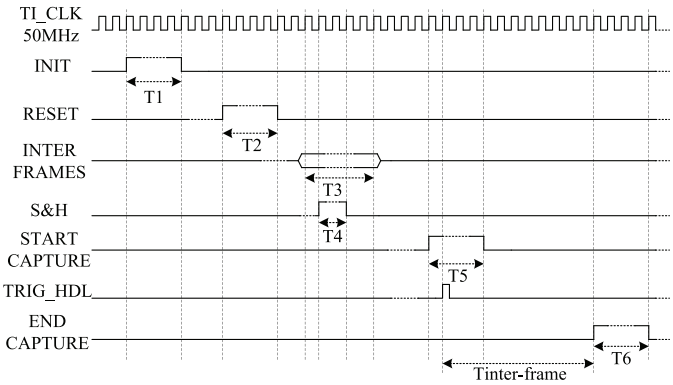

Fig. 4. Signals chronogram of GUI.

for **S**ingle **M**emory **C**ell **F**ully **R**andom **A**ccess (SMC-FRA), SDRAM controller for full-page readout and fast USB-link. The block diagram is depicted in Fig. 2. The histograms of all the pixels of the sensor array are built on the fly in a Micron SDR SDRAM of 32MB [9]. It is integrated with a Spartan3 FPGA on the same XEM3010 board [10]. The controller of the SPAD imager used to test the proposed design is implemented on the same FPGA, along with the USB data readout.

A. Graphic User Interface for Control Signals

A user friendly GUI has been built in Matlab (see Fig. 3). First of all the interface has to be set to display either brightness or depth images by pushing the 2D/3D button. Note that for 3D vision, the angle of view can be changed by the horizontal and vertical sliders. Subsequently, the camera has to be configured in the proper mode by loading the bit file into the FPGA board. The number of inter-frames has to be loaded as well. At this point, image streaming can start. Later on it can be stopped by the same *Start/Stop* button.

In order to communicate with the SPADCAM through the FPGA board, **A**pplication **P**rogrammer's **I**nterface (API) components such as WireIn, WireOut, TriggerIn and PipeOut have been used [11].

The signals chronogram exchanged between GUI and FPGA HDL is depicted in Fig. 4. Control signals as INIT, RESET and START CAPTURE and configuration signals as INTER-FRAMES are sent to the FPGA by WireIns. Conditioning signals as END CAPTURE are received from camera by WireOut. A Trigger component, S&H is used to latch the number of inter-frames on the FPGA. A PipeOut component is called to send the 2D/3D images built in the SDRAM memory to PC.

TI_CLK is the clock of the USB interface. The signal END CAPTURE flags when the histograms can be read.

The number of inter-frames used to build the pixel-wise histograms for 2D/3D images is set into the GUI.

B. Image Acquisition Controller

The image acquisition controller (see Fig. 5) downloads the inter-frames pixel-by-pixel from the SPAD imager to the *Pixel value* FIFO. These values represent either the brightness for 2D images or the direct ToF for 3D images. At the same time, the pixel position in the current inter-frame is downloaded into the *Pixel position* FIFO.

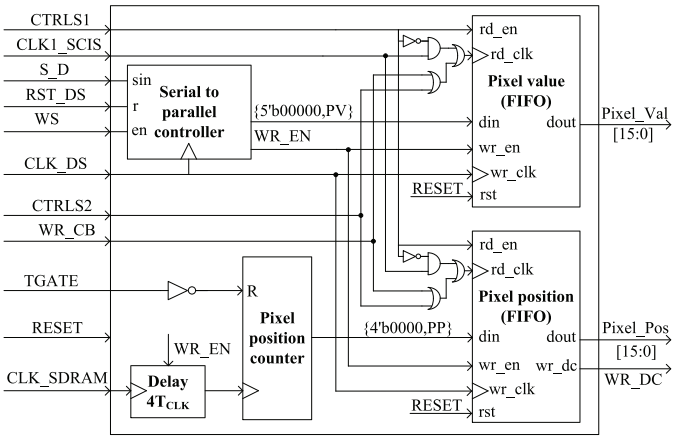

Fig. 5. Image acquisition controller.

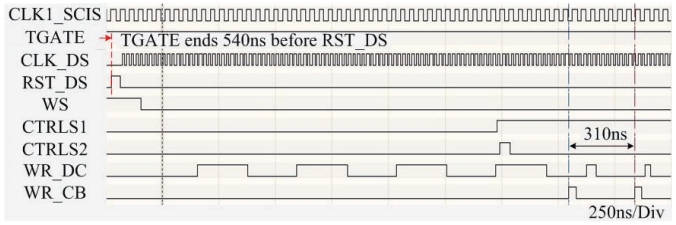

Fig. 6. Chronogram of image acquisition controller.

In the case of the SPAD camera used for our proof, each FIFO has 2048 memory locations on 16bits depth, which is half of the SPAD imager's size. However the FIFOs do not have time to get full during the acquisition phase. The pixel position is automatically incremented by the *Pixel position counter*.

This module is driven by 3 clock signals: CLK_SCIS (25MHz), CLK_DS (50MHz) and CLK_SDRAM (100MHz).

The control signals acquired by a logic analyzer are shown in Fig. 6. A reset is issued before the reconstruction of a frame starts. Every inter-frame is captured into a programmable time gate by the SPAD imager upon a global shutter scheme. The control signals of the SPAD imager, such as the time gate signal, TGATE, the global reset signal of the pixel-array and the control signals of the readout pipeline are generated by the *SPAD imager controller*. TGATE lasts 87µs or 307ns for 2D or 3D mode respectively. Note that in the former case the time gate is actually the integration time. Later on the inter-frame is sent off-chip line-by-line by the readout pipeline which has the same clock signal like the *Serial to parallel controller* module. The prototyped SPAD imager has a serial output, S_D at 50MHz. The control signals RST_DS and WS are used to load the inter-frame in the image acquisition controller module. Whenever a pixel value on 11 bits is acquired, it is loaded into the FIFOs by the WR_EN signal. When each FIFO contains 8 words, i.e. WR_DC equals 8, the FIFOs reading begin. It is instructed by the histogram controller module by the signals CTRLS1 and CTRLS2. It happens whenever a histogram bin is ready to be written at the corresponding location into the histogram memory.

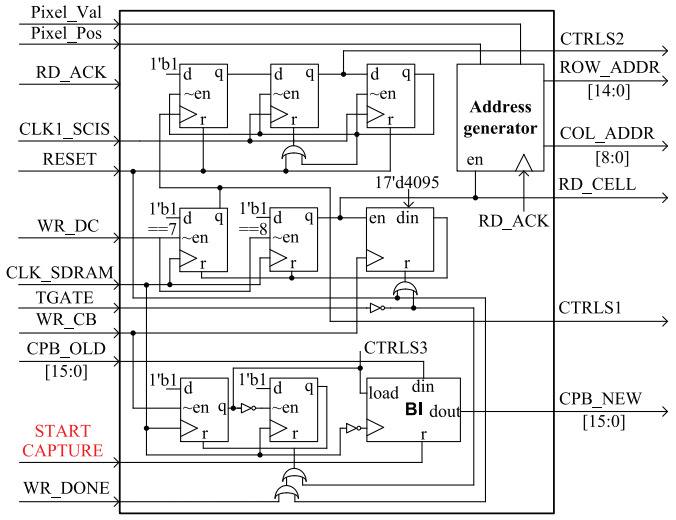

Fig. 7. Histogram controller.

C. Histogram Controller

This block distributes the ongoing inter-frames into the right bin of the corresponding histograms pixel-by-pixel. When WR_DC equals 8, the FIFOs reading is enabled when CTRLS1 is set high.

Right after enabling the read, a single pulse of CTRLS2 is sent to the read clock ports to get the value and position of the first pixel of the frame. On the positive edge of RD_ACK signal, the value and position of the pixel are sampled by *Address generator* module to compute the location in the corresponding histogram.

The location of the pixel in the histogram is ready before CTRLS3 is set high. The row and column address are computed by the *Address generator* and fed into the SMC-FRA controller. The selected bin is read on the first edge of CLK_SDRAM when CTRLS3 is high, incremented by 1 unit in *BI* (Bin Increment) block and written back at the same location.

Right at the end of the acquisition time, all per-pixel inter-frame histograms are ready. The accurate ToF measurement of each pixel is represented by the peak value of the corresponding histogram.

D. SMC-FRA Controller

The pixel-wise inter-frame histograms are built into a SDRAM memory [9]. It has 256Mb distributed in 4 banks. Each bank has 8192 rows and 512 columns of memory locations on 16bits depth. The organization chart of the inter-frame histograms is presented in Fig. 8. Each memory location represents a histogram bin, allowing 65536 hits per bin. Therefore the inter-frame histogram of the pixel P(1, 1) is stored in the first 4 rows of the first bank and so one until the histogram of the pixel P(64, 64) is stored in the last 4 rows of the second bank.

In the case of 3D images, ToF is represented at pixel level on 11bits.

This means that the histogram needs to have 4×512 bins. Thus, only half on the memory it is required for a

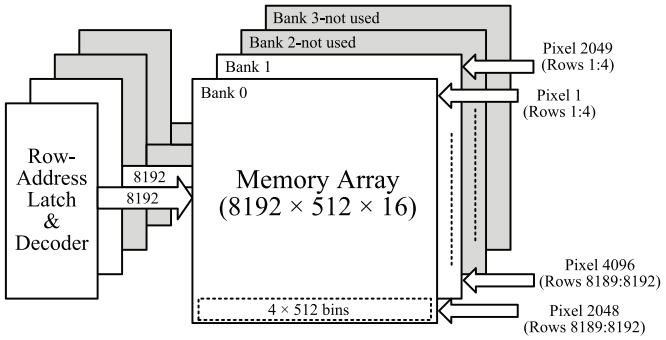

Fig. 8. Organization chart of 64 × 64 inter-frame histograms.

64 × 64-pixels array. Note that 2D images are represented on 8 bits such that the histogram has only 256 bins.

The inter-frame histogram of each pixel is built as follows: the pixel number represents the location of the 4×512 memory block while the pixel value is used to compute the position of the bin inside the memory block.

The memory controller is designed for SMC-FRA, taking into account the electrical characteristics of the SDRAM module [9]. The FSM and experimental signals chronogram are depicted in Fig. 9 and Fig. 10 respectively.

After a proper reset is performed, the operation mode has to be loaded in the mode register. Once the memory gets in the "idle" state, the building of the histograms starts by setting high the signal RD_CELL. It is requested by the histogram controller which computes the histogram bin location represented by the ROW_ADDR and COL_ADDR signals. The computation of the histogram bin location is based on Pixel_Val and Pixel_Pos values which are retrieved from FIFOs by the *Address generator* module on the positive edge of RD_ACK signal. The computed memory location is read. The content of this memory location represents the number of counts per bin, CPB_OLD which is available in "srd5" state. The signal CPB_OLD is sampled by the *BI* block on the negative edge of CLK_SDRAM when CTRLS3 signal is set high. CPB_OLD is automatically incremented by 1 unit to count in the value of the current pixel. The new value of the bin, CPB_NEW is written back to the same location in "swr3" state.

On the edge of WR_CB, the value and position of the next pixel are read from FIFOs. The signal WR_DONE sends the memory in the "idle" state, and so one for all the pixels of the current inter-frame. The measured bin-to-bin period is of 306ns.

When the acquisition ends, the inter-frame histograms over a programmable inter-frames number is ready. The reconstructed frame is available at the very end of the inter-frame acquisition phase. Therefore it is sent to PC through an USB link. In this phase the SDRAM controller is instructed to perform full-page transfer using a read FIFO.

III. SPAD Camera Experimental Results

The SPADCAM used to prove the design of the proposed ifHB is presented in Fig. 11 [8]. It is built by the following

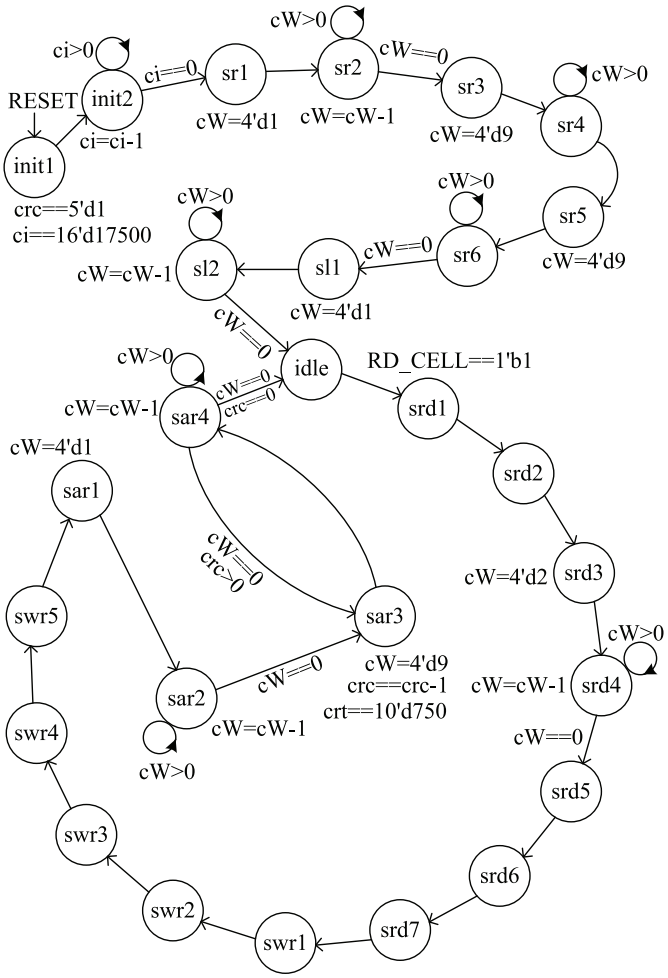

Fig. 9. SMC-FRA controller.

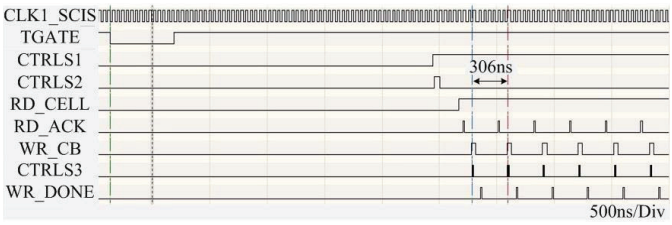

Fig. 10. Chronogram of random access SDRAM controller.

parts: i) a 64 × 64-pixels SPAD imager containing the following in-pixel modules: a p+/n−well SPAD detector with active quenching/recharge circuit, 8bits **T**rue **S**ingle **P**hase **C**lock (TSPC) counter and 11bits TDC for photon counting and ToF; ii) an 8mm F1.2 lens; iii) a band-pass filter centered on the laser wavelength (required only for 3D imaging); iv) a power supply module to provide a variable bias voltage for SPADs from 10.8V to 12V and a 3.3V voltage supply for the sensor chip pad ring; iv) a XEM3010 FPGA board.

The PDE at 640nm and average DCR at 1V excess voltage (V_E) are of 5% and 42kHz respectively. Moreover, the background light could cause an additional uncorrelated noise up to 20 times the average DCR. Under these circum-

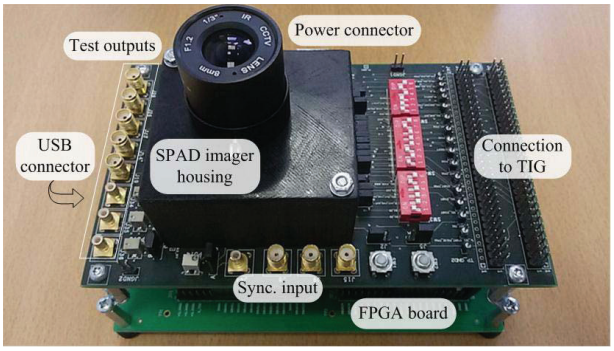

Fig. 11. SPADCAM prototype.

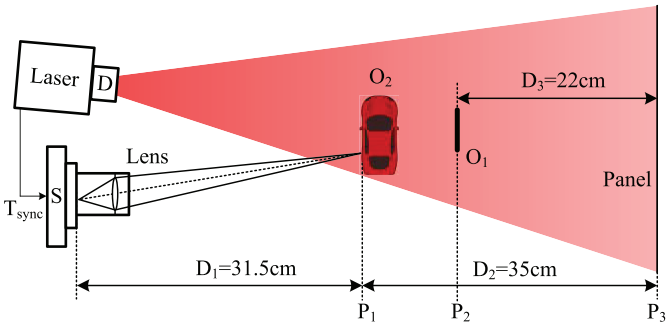

Fig. 12. Top view of the 3D image reconstruction setup: O_1 and O_2 are a geometric shape and a toy car placed in front of a panel.

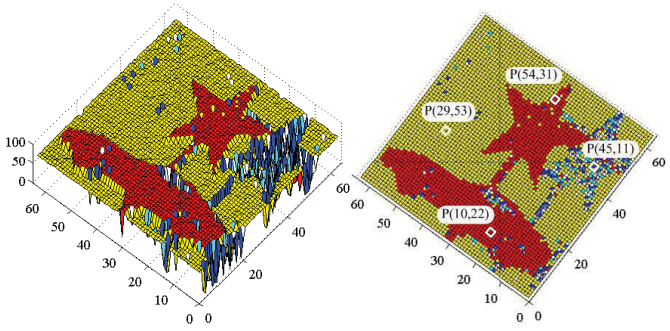

Fig. 13. 3D image: Star and Toy car (raw image); V_E is 1.1V.

stances most of the time the imager is triggered by noise. Therefore only averaging multiple inter-frames is not enough. Instead we propose to build an inter-frame histogram for each pixel.

The final ToF stamp for each pixel is extracted from the peak of the histogram.

The SPADCAM prototype has a serial output running at 50MHz, meaning a top frame rate of 1.1kfps. Each pixel of every inter-frame takes a single measurement.

The proposed ifHB has been tested with the SPAD imager both for 3D and 2D vision.

A. 3D Vision (Depth Map)

The top view of the experimental setup is presented in Fig. 12. The scene is represented by 2 objects, O_1 and O_2 placed in front of a white panel. It is illuminated by a picosecond laser through a square pattern diffuser [12]. The laser has 640nm wavelength. The average output irradiance measured after diffuser is of 2.5W/m^2. It decreases to 3mW/m^2 at 0.5m from the laser. The repetition rate (f_{sync}) is set to 2.5MHz [13] and gated to 1.1kHz such that only one stop pulse occurs every inter-frame.

The display of the GUI (see Fig. 3) has been set to 3D view. The 3D image is obtained after acquiring 65536 inter-frames which limits the overall frame rate in this prototype. However, considerable improvements can be achieved by enhancing the PDE of the SPAD detector and the readout throughput. The capability of capturing 3D images in single photon detection conditions with reflected light irradiance below 10nW/mm^2 suggests that SPADCAM can potentially be used also in other applications such as fluorescence life-time imaging microscopy.

Besides, a more powerful pulsed light source can be employed also to increase the depth range. In this case the jitter of the sensing chain could increase requiring more inter-frames to keep the same precision. Eye safety regulations have to be taken into account as well.

The obtained depth image is shown in Fig. 13 from 2 angles of view.

Note that the illumination source is on the left side, leaving a shadow on the right side of the scene. It means that the laser light does not reach the shaded area. Consequently no laser light bounces back to the SPAD imager. In this case the corresponding pixels are triggered only by noise.

The histograms of some representative pixels are presented in Fig. 14. The pixels P(10, 22), P(54, 31) and P(29, 53) belong to the plans P_1, P_2 and P_3 respectively (see Fig. 12). Note that the pixel P(45, 11) is located in the shaded area therefore it is triggered only by uncorrelated noise. Moreover, the histogram peak of the pixel from P_3 plane is smaller. It happens because of the inverse square law of the reflected light. The characteristics of the reflected object surface counts as well. The irradiance of the reflected laser light measured at the sensor surface is below 10nW/mm^2. The photon timing SNR of the inter-frame histogram of P(29, 53) (see Fig. 14) is of 30dB. By considering the background light, the photon timing SNR drops to about 24dB.

The average power consumption of the SPADCAM is highly dependent on the frame rate. It is mainly due to the in-pixel TDCs which use a voltage controlled ring oscillator as time interpolator. It means that the closer is the target, the longer the time interpolator works and the larger is the power consumption. Moreover the power consumption of the in-pixel TDC depends on its time bin, as it is shown in Fig. 15.

B. 2D Vision (Brightness Map)

The display of the GUI is switched to 2D view. The proper configuration of the camera is loaded. The number of inter-frames is set to 900. The same scene has been captured with a bridge camera Fig. 16. The only difference is that instead of the low light pulsed laser, the scene is illuminated only by a conventional 2 $\times$ 26W fluorescent light source. An irradiance of 2W/m^2 has been measured by a Newport 918-SL photodetector, selecting a wavelength of 555nm. The distance between the light source and the target is 0.5m. Note

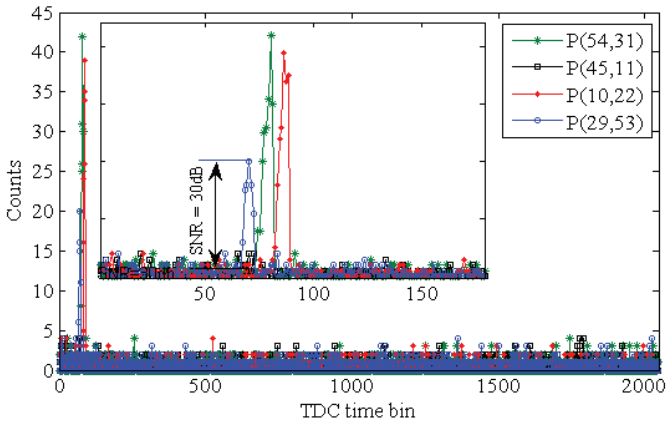

Fig. 14. ToF inter-frame histograms of the pixels P(54, 31), P(45, 11), P(10, 22) and P(29, 53).

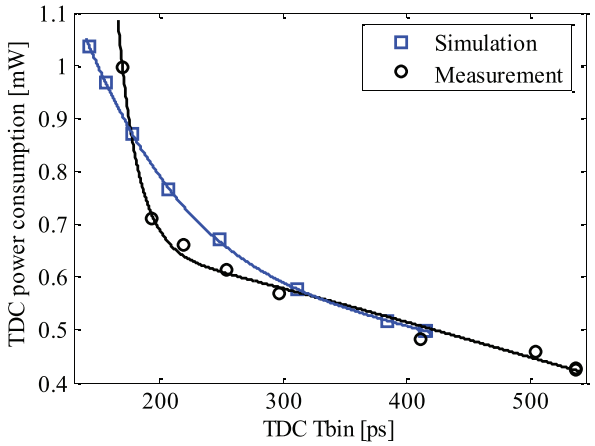

Fig. 15. In-pixel TDC power consumption.

that this illumination source is more powerful compared to the 3mW/m^2 of the pulsed laser measured at the same distance. This explains the much lower number of inter-frames than the one required for 3D vision.

The 2D image captured by the SPADCAM based on ifHB is shown in Fig. 17(left). Although the ifHB proved to offer an outstanding advantage of accurately extracting the ToF, it also can improve 2D images. It applies for low area/low power in-pixel TSPC counters with limited minimum input frequency in low illumination conditions and small inter-frame integration time. Under these circumstances, the counters take false measurements which could scatter from the true measurements. In this case ifHB disregards these faults. Note that ifHB uses the same hardware as for 3D images. The image obtained by merely averaging the inter-frames is presented as well in Fig. 17(right). The proposed method slightly enhances the contrast producing a sharper image (R1 region when P2 is the focusing plan) with less artifacts (R2 region). The rest of the black and white pixels are caused by faulty pixels due to technology defects.

C. 2D Vision (Slow Motion)

The prototype of the SPADCAM can be also used to continuously record videos in slow motion. In this experiment a propeller is rotating at 2850 RPM (see Fig. 18a). The red

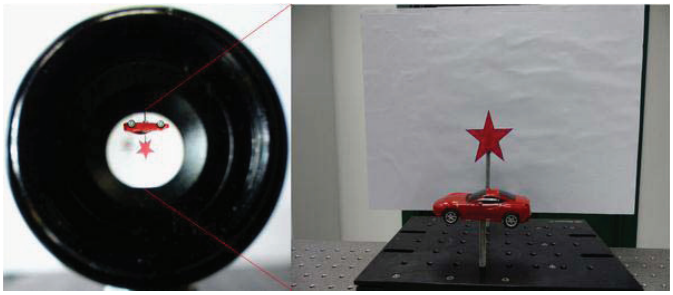

Fig. 16. The scene taken with a conventional camera.

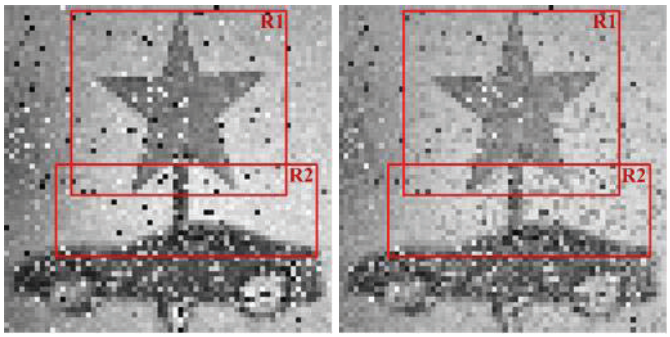

Fig. 17. 2D image built from inter-frames histograms (left) and inter-frames average (right).

circles are only to separate different regions of the image. A video is recorded at 1kfps and played back at 50fps being able to see the propeller blades (see Fig. 18b). A command line interface has been designed for this purpose. The inter-frame histograms built in real-time along 500 inter-frames are able to extract fast moving objects from the scene. Each pixel from Fig. 18c and Fig. 18d represents the peak and the average of the corresponding inter-frame histogram, respectively.

In the former case, only the stationary part of the scene is extracted. The latter case is equivalent to taking a single picture with a larger exposure time. For this reason Fig. 18d is similar to Fig. 18a.

The explanation of this kind of background subtraction is given by the inter-frame histogram of pixels located in two different regions named R1 and R4 (see Fig. 18a, b and Fig. 19). On one hand, P(15, 15) is sampling the background most of the time (higher peak) while the blades are sampled less times (middle peak). On the other hand, P(32, 31) samples all the time the middle of the propeller which is a steady part of the image.

IV. Ultra-High Frame Rate SPAD Image Sensors

The prototyped SPADCAM has a serial output at 50MHz leading to a frame rate of 1.1kfps. The pixel period is 220ns. Every time a pixel is ready at the output of the image acquisition controller, the following operations need to be performed: i) to compute the location of the bin in the memory based on the pixel value and index; ii) read the value of the histogram bin from the particular location; iii) increment the value of the bin by 1 unit; iv) write back the new value of the bin. The SMC-FRA controller (see Fig. 9) incorporated in this work fulfills the speed requirements such that the

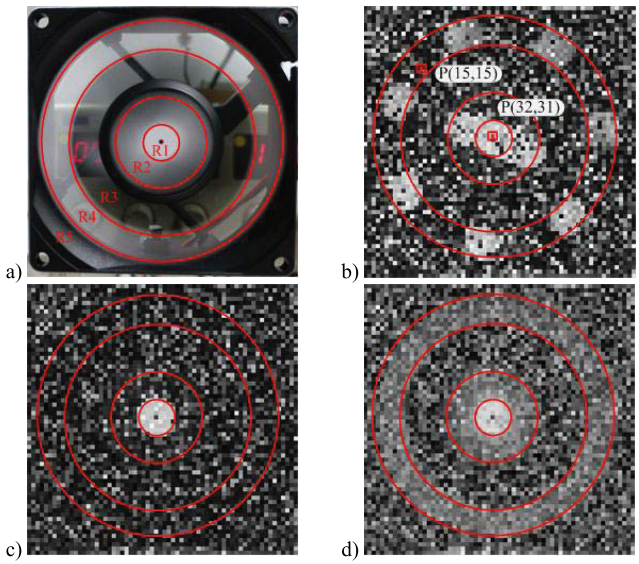

Fig. 18. Slow motion video of propeller rotating at 2850 RPM: a) Snapshot with commercial camera; b) Snapshot of the video recorded by SPADCAM at 1kfps and played back at 50fps; c) 2D image obtained from the peak-histogram; d) 2D image obtained from the average-histogram.

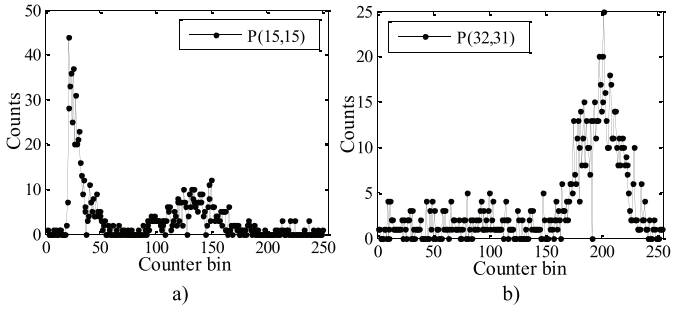

Fig. 19. Histogram of pixel P(15, 15) and P(32, 31) along 500 inter-frames.

inter-frame histograms are built in real-time at approximately SPADCAM's frame rate.

It is worth to mention that the speed of the ifHB is strictly related to the fully random memory access time lapse. Seeking to increase the memory access time with the same SDR SDRAM memory, we changed the representation of the histograms as shown in Fig. 20.

We evaluated the histogram building period by interleaving between the 4 memory banks.

The signal chronogram is shown in Fig. 21. In this case 4 pixels are resolved in 158ns. Therefore the maximum frame rate of the ifHB is more than 6kfps at 133MHz and 64×64-pixels.

In the following, we evaluate whether this design can be scaled for ultra-high frame rate SPAD imagers. This kind of image sensors is based on in-pixel counter/TDC architecture for photon counting/ToF. Under these circumstances, the frame rate limitation is usually given by the readout electronics. Parallel readout is the key but aspects related to the power budget and signal integrity has to be carefully contemplated. According to our calculations, 32 outputs at 50MHz can fit into a 144 PGA package. This means a throughput of 1.6Gb/s leading to a frame rate of 32kfps for 64×64-pixels array which stands in the state-of-the-art specifications [1]. In this

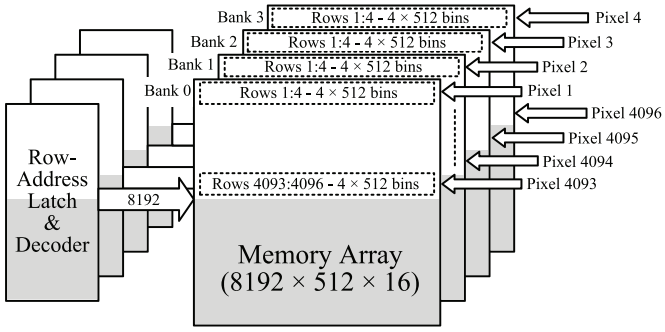

Fig. 20. Organization chart of 64×64 inter-frame histograms.

case, the ifHB has to work 8 times faster than the maximum speed evaluated in the previous case. Thus every pixel has to be counted in the corresponding histogram bin in 6.875ns.

Choosing faster technologies than SDR SDRAM, such as DDR2 SDRAM or DDR3 SDRAM is not necessarily a solution. This happens because these memory modules are optimized in burst mode and contiguous access. The latency for single random Read/Write operations is given by the following timing characteristics: Column Address Strobe latency (CAS), Active-to-Active delay (tRC), Active-to-Read or Write delay (tRCD), Active bank a to Active bank b delay (tRRD), Write Recovery time (tWR), Precharge period (tRP) and Auto Refresh time (tRFC). Indeed, evaluating different memory modules, it seems that these parameters are pretty much the same [9], [14] and [15] because they do not depend on the clock frequency (tCK). Instead, the aforementioned parameters are related to the current capability of the column sense amplifier and the total capacitance of the bit line driven by it. Therefore smaller memory capacity has smaller latency.

A SRAM memory is more adequate for the proposed ifHB which mainly requires ultrafast SMC-FRA. Before evaluating some of the fastest devices on the shelf, it is worth to seek for the minimum memory capacity that can fit our application. According to the histogram from Fig. 14, we can have 8 instead of 16 bits per bin, without losing any inter-frames. Therefore 64Mb memory is enough to store the histograms. The Read-Write cycle time for one of the fastest memory IC is 20ns [16]. Four modules of 16Mb can cover the above mentioned 6.875ns by running in parallel. In order to have a safer timing margin, more parallelization is required. For instance 8 modules of 8Mb have an equivalent Read-Write cycle time of 2.5ns [17]. However this solution is quite bulky and requires a lot of connections and control signals.

These considerations led us to the conclusion that the proposed design is suitable to be implemented in ASIC. Thus 32 fully-parallel SRAM memory channels of 256kB have the bandwidth up to 6.4Gb/s. These specifications easily fulfill the timing requirements of an ultra-high frame rate SPAD imager. Notice that the proposed ifHB design can be integrated on the same chip having only 32 serial inputs, several control signals from the sensor and a serial output.

At the end of the inter-frames acquisition time, the final frame in raw format is ready to be sent to PC. It contains 64×64 inter-frames histograms. In order to get the brightness or depth map of the scene, we display the peak of each histogram. In the prototype SPADCAM, we have

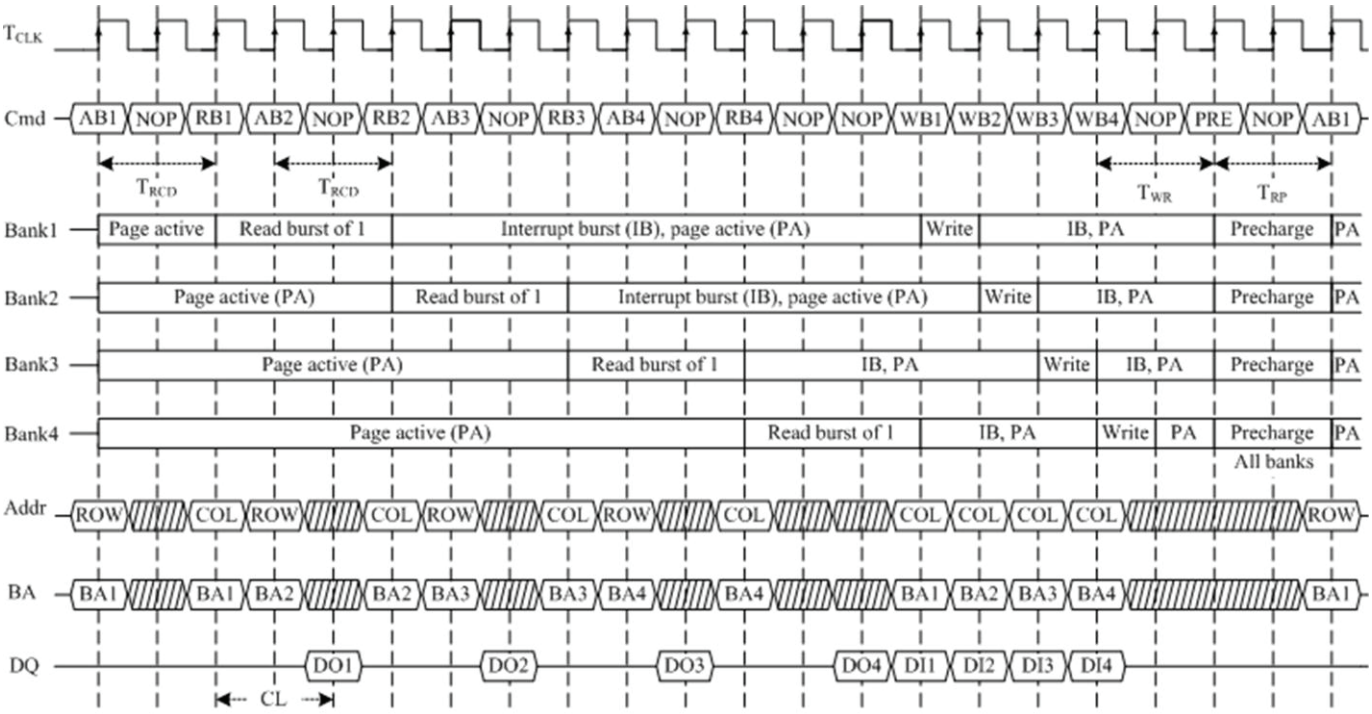

Fig. 21. Signal chronogram for interleaved memory internal banks access.

computed the peak histogram in software. It was easily done because the overall frame rate is limited by the SPAD imager's serial output.

V. Conclusion

This paper presents the design of an ifHB for noise reduction in SPAD imagers for direct ToF estimation. The design has been tested on FPGA with a 64×64-pixels SPAD imager to extract the ToF. We proved that the current design is very efficient for 3D vision to remove a large amount of uncorrelated noise such as DCR or background light. Moreover, the potential use of the proposed ifHB for background subtraction and image enhancement in 2D images has been contemplated. The design works in real-time at almost 1kfps. This limitation is mainly given by the single memory location access time. By scaling the figures we obtained with the prototyped camera, we estimate that, on ASIC, the proposed design could reach a frame rate of 142kfps. In this way the overall frame rate of the camera is given only by the required number of inter-frames. As future work, we are planning to implement the proposed design on ASIC aimed for SPAD imagers with large uncorrelated noise.

References

[1] A. Tosi and F. Zappa, "MiSPiA: Microelectronic single-photon 3D imaging arrays for low-light high-speed safety and security applications," *Proc. SPIE*, vol. 8899, p. 88990D, Nov. 2013.

[2] G.-F. D. Betta, L. Pancheri, D. Stoppa, R. Henderson, and J. Richardson, *Avalanche Photodiodes in Submicron CMOS Technologies for High-Sensitivity Imaging* (Advances in Photodiodes). Rijeka, Croatia: InTech, 2011, pp. 225–248. [Online]. Available: http://www.intechopen.com/books/advances-in-photodiodes/avalanche-photodiodes-in-submicron-cmos-technologies-for-high-sensitivity-imaging, doi: 10.5772/15178.

[3] D. P. Palubiak and M. J. Deen, "CMOS SPADs: Design issues and research challenges for detectors, circuits, and arrays," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 6, Nov./Dec. 2014, Art. no. 6000718.

[4] D. Bronzi *et al.*, "100 000 frames/s 64 × 32 single-photon detector array for 2-D imaging and 3-D ranging," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 6, Nov. 2014, Art. no. 3804310.

[5] I. Vornicu, R. Carmona-Galán, and Á. Rodríguez-Vázquez, "Live demonstration: Photon counting and direct ToF camera prototype based on CMOS SPADs," in *Proc. IEEE Int. Symp. Circuits Syst.*, Baltimore, MD, USA, May 2017, pp. 28–31, doi: 10.1109/ISCAS.2017.8050392.

[6] N. A. W. Dutton *et al.*, "A time-correlated single-photon-counting sensor with 14GS/S histogramming time-to-digital converter," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2005, pp. 1–3.

[7] N. Dutton *et al.*, "Multiple-event direct to histogram TDC in 65 nm FPGA technology," in *Proc. 10th Conf. Ph.D. Res. Microelectron. Electron.*, Jun./Jul. 2014, pp. 1–5, doi: 10.1109/PRIME.2014.6872727.2014.

[8] I. Vornicu, R. Carmona-Galán, Á. Rodríguez-Vázquez, "Photon counting and direct ToF camera prototype based on CMOS SPADs," in *Proc. IEEE Int. Symp. Circuits Syst.*, Baltimore, MD, USA, May 2017, pp. 28–31, doi: 10.1109/ISCAS.2017.8050410.

[9] Micron. *MT48LC16M16A2BG-7E:D Datasheet*. Accessed: Dec. 25, 2017. [Online]. Available: https://www.micron.com/resource-details/de1c0096-e648-45b1-a17c-000e74fa7269

[10] Opal Kelly. *XEM3010 User's Manual*. Accessed: Dec. 25, 2017. [Online]. Available: http://assets00.opalkelly.com/library/XEM3010-UM.pdf

[11] Opal Kelly. *FrontPanel User's Manual*. Accessed: Dec. 25, 2017. [Online]. Available: http://assets00.opalkelly.com/library/FrontPanel-UM.pdf

[12] *Thorlabs ED1-S50 Diffuser*. Accessed: Dec. 25, 2017. [Online]. Available: https://www.thorlabs.com/thorproduct.cfm?partnumber=ED1-S50

[13] PicoQuant GmbH. *PicoQuant D-C-640 Pulsed Laser Data Sheet*. Accessed: Dec. 25, 2017. [Online]. Available: https://www.picoquant.com/products/category/picosecond-pulsed-sources/ldh-series-picosecond-pulsed-diode-laser-heads

[14] Micron. *MT47H64M16HR-25E Datasheet*. Accessed: Dec. 25, 2017. [Online]. Available: https://www.micron.com/parts/dram/ddr2-sdram/mt47h64m16hr-25e

[15] Micron. *MT41K256M16HA-107 Datasheet*. Accessed: Dec. 25, 2017. [Online]. Available: https://www.micron.com/resource-details/7b9a378c-8ca7-49c4-9c96-53b777a38810

[16] Cypress. *CY7C1069GN*. Accessed: Dec. 25, 2017. [Online]. Available: http://www.cypress.com/file/317266/download

[17] Cypress. *CY62158EV30*. Accessed: Dec. 25, 2017. [Online]. Available: http://www.cypress.com/file/43811/download

Ion Vornicu received the degree in electronics engineering (specialization in microtechnologies) in 2008, the M.Sc. degree in modern signal processing techniques, and the Ph.D. degree in microelectronics in 2011, all from the Faculty of Electronics and Telecommunications, Gheorghe Asachi Technical University of Iasi, Romania. During the Ph.D. degree, his main research focus has been on CMOS implementation of a type of cellular neural networks for spatio-temporal analog image processing, log-domain circuits, and smart CMOS imagers. Since 2011, he has been a Post-Doctoral Researcher with the Institute of Microelectronics of Seville, Spain. His current research interests include in the design and test of CMOS sensors based on single-photon avalanche diodes used for 3-D vision and nuclear medicine imaging such as positron emission tomography. He received a Best Paper Award from the Sensory System Technical Committee of the IEEE Circuits and Systems Society.

Ricardo Carmona-Galán received the degree in physics in 1993 and the Ph.D. degree in microelectronics in 2002 from the University of Seville, Spain. From 1996 to 1998, he was a Research Assistant with Prof. Chua's Laboratory, EECS Department, University of California at Berkeley, Berkeley, CA, USA. From 1999 to 2005, he was an Assistant Professor with the Department of Electronics, University of Seville. He held a post-doctoral position at the University of Notre Dame, Notre Dame, IN, USA, from 2006 to 2007, where he worked on interfaces for CMOS compatible nanostructures for multispectral light sensing. He has collaborated with start-up companies in Anafocus, Seville, and Eutecus, Berkeley. He has designed several vision chips implementing different focal plane operators for early vision processing. Since 2005, he has been a Tenured Scientist with the Institute of Microelectronics of Seville His main research focus has been on VLSI implementation of concurrent sensor/processor arrays for real time image processing and vision. He has co-authored more than 120 papers in refereed journals and conferences and several book chapters. His current research interests lie in the design of low-power smart image sensors and 3-D integrated circuits for autonomous vision systems. He was a recipient of the Best Paper Award from the *International Journal of Circuit Theory and Applications*. He was a co-recipient of the Award of the ACET and a Certificate of Teaching Excellence from the University of Seville.

Ángel Rodríguez-Vázquez is currently a Full Professor of Electronics with the University of Seville, Seville, Spain, and was appointed for research at the Centro Nacional de Microelectrónica, Institute of Microelectronics of Seville, Consejo Superior de Investigaciones Cientficas-University of Seville. He has authored eight books, approximately 50 chapters in edited books, including original tutorials on chaotic integrated circuits, design of data converters, and design of chips for vision, and some 500 articles in peer-reviewed specialized publications. His research work is widely quoted, and he has an h-index of 35. His current research interests are in the areas of imagers and vision systems using 3-D integration technologies and of ultra-low-power medical electronic devices. He was a recipient of a number of international awards for his research work, including the IEEE Guillemin Cauer Best Paper Award and two Best Paper Awards from *Wileys International Journal of Circuit Theory and Applications* the IEEE European Conference on Circuit Theory and Design Best Paper Award, and the IEEE International Symposium on Circuits and Systems Best Demo-Paper Award. He is on the committee of many international journals and conferences and has chaired different international IEEE and Society of Photo-Optical Instrumentation Engineers conferences. He has been serving as an Editor, an Associate Editor, and a Guest Editor for different IEEE and non-IEEE journals.