A 2.5-V ΣΔ MODULATOR IN 0.25-μm CMOS FOR ADSL

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ABSTRACT

This paper presents a dual-quantization cascade SC ΣΔ modulator intended for A/D conversion in ADSL applications. The modulator combines a low oversampling ratio with 3-bit resolution in the last stage, to achieve 14bit@4.4MS/s (16x) and 15bit@2.2MS/s (32x) with no need of correction/calibration mechanisms. It consumes 66mW from a single 2.5-V supply and has been implemented in 0.25-μm CMOS technology.

1. INTRODUCTION

Nowadays industry is demanding high-performance ADCs for broadband access to the internet over phone twisted-pair (*x*DSL). These ADCs must achieve 12- to 16-bit accuracy for signal bandwidths higher than 1MHz, and must be implemented in standard CMOS technologies. In this scenario, Sigma-Delta modulators (ΣΔM) are especially attractive, due to their robustness and low-complexity circuitry. However, for broadband applications, increasing the signal bandwidth while maintaining a feasible sampling frequency constrains designers to use a moderate oversampling ratio. Modulators employing high-order filtering and/or multi-bit quantization are commonly used in order to achieve the required resolution, but both strategies degrade the original robustness of the ΣΔ conversion. Therefore, the designer is often forced to include correction/calibration mechanisms to circumvent the problem, in exchange for a higher complexity and increased power consumption.

The ΣΔ modulator presented in this paper targets 14-bit effective resolution at 4.4MS/s, with no need of correction techniques. These specifications pose a significant design challenge when compared to the current state-of-the-art on CMOS high-speed ΣΔMs [1]-[9]. On the one hand, both resolution and speed are at the top edge of the reported designs [2]-[8]. On the other, high resolution is attained with a single 2.5-V supply, whereas most of recent designs still use a 3.3-V supply in the modulator analog core [5]-[7].

This performance is achieved using a multi-bit cascade modulator, implemented in 0.25-μm CMOS technology. The paper first presents the modulator architecture and discusses considerations related to its sizing. Then, the details of the design of its main blocks are presented.

2. MODULATOR SIZING

The architecture selected is the 211*mb* ΣΔM, a 4th-order 3-stage dual-quantization cascade using multi-bit quantization only in the last stage of the cascade [2] [7]. Fig.1 shows its block diagram, where the integrators weights used are $g_1 = g_1' = 0.25$, $g_2 = 1$, $g_2' = 0.5$, $g_3 = 1$, $g_3' = g_3'' = 0.5$, $g_4 = 2$, and $g_4' = g_4'' = 1$.

The modulator oversampling ratio *OSR* and the resolution *B* of the multi-bit quantizer have been selected considering the main technological limitations (mismatches in capacitors and resistors, and feasible gain for amplifiers) affecting this topology. Fig.2 shows the modulator effective resolution as a function of *B*, with *OSR* acting as a parameter and in the presence of non-idealities. The targeted resolution can be achieved with different (*OSR*, *B*) sets, depicted on the plot. We have selected ($OSR = 16$, $B = 3$), because it trades *OSR* (and hence reduced power consumption) for a small increase of the last-quantizer complexity. Given the 2.2-MHz signal band, this leads to a nominal sampling frequency $f_s = 70.4\text{MHz}$. Operating with a higher oversampling (20x or above) will push f_s up to 100MHz, which can considerably complicate the design.

The proposed architecture can be implemented in robust manner with no need of calibration or correction, because the errors in the last-stage multi-bit quantizer and DAC are noise-shaped in cascade architectures [2].

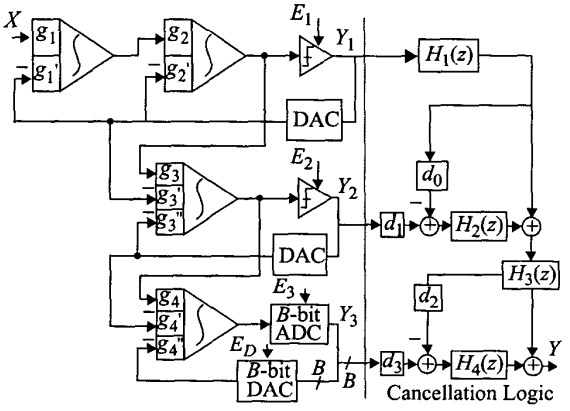

Fig. 1: Block diagram of the 211*mb* ΣΔM.

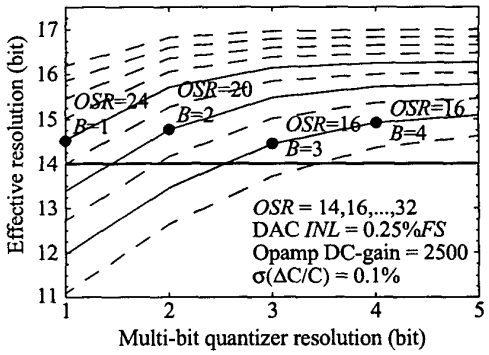

Fig. 2: ΣΔM resolution vs. multi-bit quantizer resolution.

2.1. Switched-capacitor implementation

The fully-differential schematic of the 211*mb* ΣΔM is shown in Fig.3. The first stage is formed by two SC integrators – the first one with a single input branch and the second with two input branches –, and switches controlled by the comparator outputs are employed to feed the quantized signal back. The 2nd stage incorporates an integrator with only two input branches, because weight $g_3 = 1$ can be distributed between the two integrator branches $g_3' = 0.5$ and $g_3'' = 0.5$. The same applies for g_4 in the 4th integrator, requiring only two input branches. This last integrator drives the 3-bit ADC and the 3rd-stage loop is closed through a 3-bit DAC. The 1-of-8 output code of the ADC is converted into binary using a ROM.

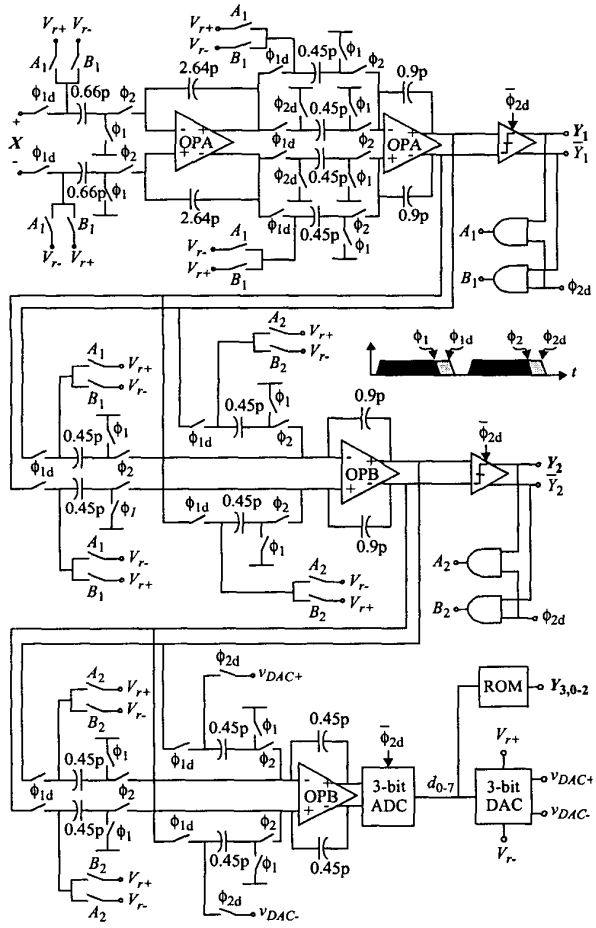

Fig. 3: SC implementation of the 211*mb* ΣΔM.

The modulator operation is controlled by two non-overlapped clock-phases: ϕ_1 for sampling and ϕ_2 for integration. In order to attenuate the signal-dependent clock-feedthrough, delayed versions ϕ_{1d}, ϕ_{2d} of the two phases are also provided. As shown in Fig.3, the delay is incorporated only to the falling edges of the clock-phases, while the rising edges are synchronized in order to increase the effective time-slot for the modulator operations [1].

2.2. Building blocks specifications

The modulator specifications have been mapped onto requirements for its building blocks using SDOPT [10], a synthesis tool for ΣΔMs that combines a statistical optimizer and an equation database that covers integrator/opamp and quantizer errors, passive component errors, analog switch errors, etc.

Table I summarizes the sizing results for the modulator blocks achieving 14bit@4.4MS/s and the most significant in-band errors. For this sizing the main error source is quantization noise (–88.5dB), while the contributions of the other error mechanisms are well below (e.g., –94.2dB for thermal noise).

Reference voltages are ±1.5V; this implies that V_{r+} and V_{r-} are +0.75V and –0.75V, respectively, in the fully-differential implementation. A 0.66-pF unitary capacitor has been selected, because it trades kT/C noise and mismatch for feasible amplifier dynamic requirements ($GBW \sim 350$MHz). The amplifier output

Table 1: Sizing of the 211*mb* ΣΔ modulator.

Modulator	*OSR*	16
	Multi-bit quantization	3bit
	f_s	70.4MHz
	V_r	±1.5V
Integrators	Unitary capacitor	0.66pF
	σ(Δ*C*/*C*)	0.1%
	Capacitor non-linearity	15ppm/V
	Switch R_{on}	150Ω
Opamps	DC-gain	3000
	DC-gain non-linearity	20%V^{-2}
	GBW (C_L = 1.5pF)	335MHz
	SR (C_L = 1.5pF)	835V/μs
	Differential *OS*	±2.0V
Comparators	Hysteresis	20mV
A/D/A Converter	Resolution	3bit
	DAC *INL*	0.25%*FS*
Dynamic range		87.7dB (14.3bit)
Quantization noise		-88.5dB
Thermal noise		-94.2dB
Incomplete settling noise		-100.1dB
Harmonic distortion		-109.0dB

swing is especially critical at 2.5-V supply, but the set of weights used reduces it to only ±2V, feasible in differential mode. The switch on-resistance is limited to 150Ω, due to its influence on thermal noise and defective settling.

Some of these specifications can be relaxed, given that the modulator is less sensitive to errors at the back-end of the cascade. This fine-tuning, shown in Table 2, is done using a more accurate time-domain behavioral simulator (ASIDES [10]).

Table 2: Fine-tuning of the building blocks specifications.

	Initial	Tuned integrators			
		1st	2nd	3rd	4th
Unitary capacitor	0.66pF	0.66pF	0.45pF	0.45pF	
GBW (C_L = 1.5pF)	335MHz	315MHz		210MHz	
SR (C_L = 1.5pF)	835V/µs	750V/µs		350V/µs	
Open-loop DC-gain	3000	3000		600	
Differential *OS*	±2.0V	±1.8V		±1.6V	

3. MODULATOR IMPLEMENTATION

3.1. Design of the building blocks

3.1.1. Operational amplifiers

Two amplifiers have been designed: a high DC-gain, high-speed amplifier for the 1st and the 2nd integrators (OPA), and a modest DC-gain, high-speed amplifier for the 3rd and 4th integrators (OPB). OPA uses a 2-stage 2-path compensated architecture (Fig.4), with a telescopic 1st-stage and both Miller and Ahuja compensation. OPB is a simple folded-cascode amplifier. The common-mode feedback nets are dynamic.

The circuit-level sizing tool FRIDGE [10] was used for the amplifier design. Amplifier DC-gain non-linearity and non-linear settling were carefully considered, because they are clearly manifested in low-voltage implementations and can severely degrade the modulator operation.

3.1.2. Comparators

Comparators at the end of the modulator 1st and 2nd stage demand a low resolution time (~ 3ns) and a hysteresis lower than 20mV. A regenerative latch including a pre-amplifying stage has been used [11].

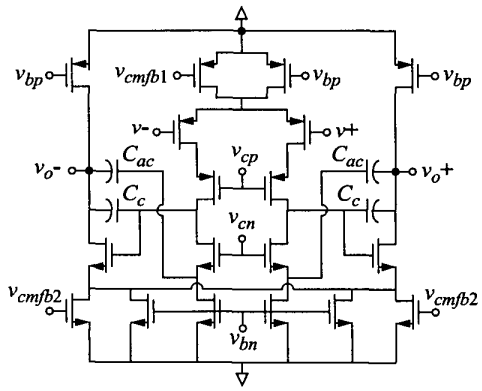

Fig. 4: Fully-differential 2-stage 2-path compensated ampli-

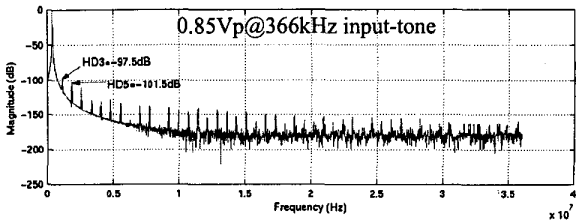

Fig. 5: Harmonic distortion due to non-linear sampling.

3.1.3. Analog switches

The value of R_{on} ~ 150Ω can be obtained using CMOS switches with 2.5-V supply and no need of clock-bootstrapping. Nevertheless, in low-voltage technologies the switch DC-characteristic is highly non-linear, causing a dynamic distortion, the more evident the larger the signal frequency [12]. The sampling process in the integrators has been analyzed using electrical simulations for sine-wave and DMT signals. With the analog switch used, *THD* is always lower than -96dB for sine-wave signals (see Fig.5) and has no practical influence on the multi-tone power ratio *MTPR* of DMT signals.

3.1.4. Capacitors

With the set of integrator weights used only 2x16 unitary capacitors are required. They have been implemented using metal-insulator-metal (MiM) structures available in the intended technology. The estimated mismatch is $\sigma(\Delta C/C)$ = 0.1% for 1-pF capacitances, low enough to avoid calibration.

3.1.5. Multi-bit quantizer

The 3-bit A/D/A converter consists of a simple fully-differential flash ADC and a resistive-ladder DAC, implemented using unsalicided *n*+ poly. The comparators in the ADC are of the same type as the ones at the end of the 1st and 2nd stages of the ΣΔM.

3.1.6. Auxiliary analog blocks

The prototype includes the following on-chip blocks:

- *Reference voltages generator:* It generates internally the voltage references V_{r+} and V_{r-} (+0.75V and −0.75V, respectively) and the analog ground. A low output impedance and in-band noise must be achieved for these references in order to avoid the degradation of the modulator performance.
- *Master current generator*: A single external resistor generates the master current, that is mirrored and scaled internally to provide the bias currents to the analog blocks.
- *Anti-aliasing filter*: It is a simple 2nd-order *RC* filter, with bandwidth higher than the modulator input band, in order to avoid distortion caused by the filter roll-off.

3.2. Modulator features

The layout of the prototype is shown in Fig.6. The substrate is non-epi and hence the layout relies in physical separation to attenuate the impact of switching noise. It uses separate analog, mixed, and digital power supplies. Guard-rings and on-chip decoupling have been included in the different sections, and the clock phases have been routed with shielding to reduce cross-talk. The prototype includes control signals for the power-down of

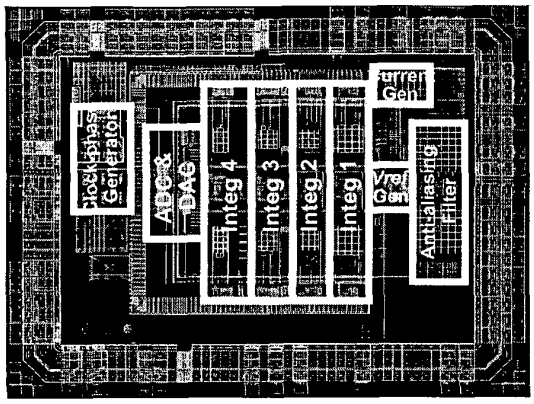

Fig. 6: Layout of the prototype.

analog blocks during the test.

The complete modulator occupies an area of 2.78mm^2 (pads excluded), and is encapsulated in 44-pin PQFP. Double-bonding techniques and multiple pins are used for the power supplies, in order to reduce supply bounce.

The modulator has been validated through behavioral and electrical simulations at nominal clock frequency. Fig.7 shows the modulator operation for a -15dB DMT input signal in the ADSL-band, with several inactive channels. The maximum *MTPR* is only -74dB, and no clipping at large input voltages is observed in time domain.

Fig.8 shows the baseband part of the modulator output spectrum obtained by electrical simulation for a -9.5dB input tone at 275kHz. It achieves a 86.7-dB dynamic range (14.1-bit effective resolution) in the 2.2-MHz band, and 94.5-dB dynamic range (15.4bit) in the 1.1-MHz band.

The overall power consumption is 65.8mW, from which 55mW correspond to analog blocks, 3mW to the mixed part, and 7.8mW to the digital section. The auxiliary analog blocks account for 10mW out of the total 55-mW analog part dissipation.

Full experimental characterization of the prototype is expected to be available for the final paper submission and at the Conference.

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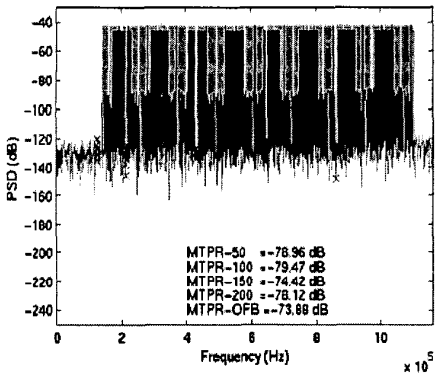

Fig. 7: Output spectrum for a -15dB DMT input signal.

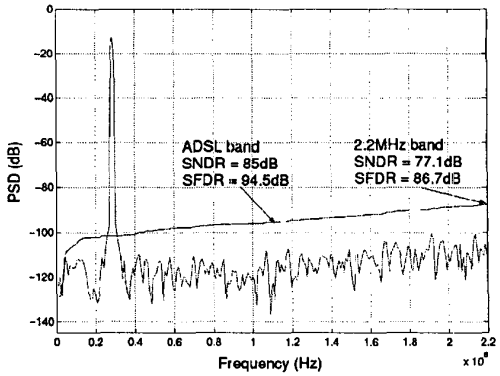

Fig. 8: Output spectrum obtained by electrical simulation.

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