Live Demonstration: Photon Counting and Direct ToF Camera Prototype Based on CMOS SPADs

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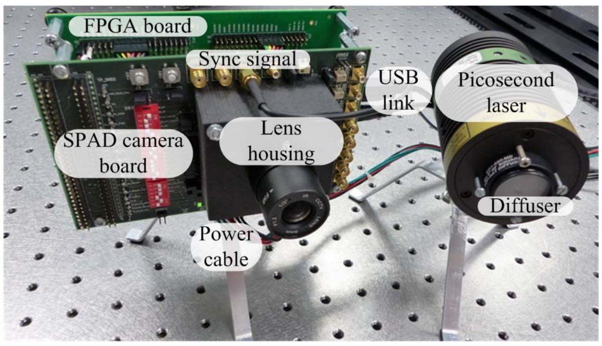
*Abstract***— This demonstrator reveals the performance and features of a single photon avalanche diode (SPAD) camera prototype. It is aimed to 2D/3D vision by photon counting and direct time-of-flight (d-ToF), respectively. The imager is built on a standard CMOS technology without any opto flavor or high voltage option. The camera module consists of a 64×64 SPAD imager and a FPGA board for real time image reconstruction at 1kfps.**

Track selection—7.1 Imagers and Vision Sensors

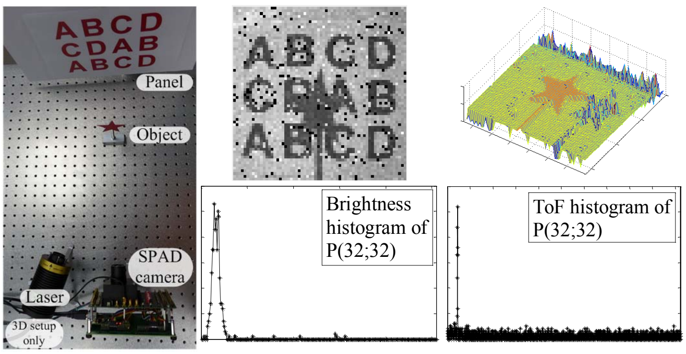
I. Introduction

Luminous intensity (2D) images are captured under high illumination conditions. The depth (3D) images are captured under very low active illumination conditions, compliant to single photon detection requirements. All images are streamed to the computer through a USB link. A user-friendly graphical user interface (GUI) has been designed in Matlab and C++.

Highly efficient circuit and system level design techniques have been employed such as: time-gated front-end; low-power in-pixel time-to-digital converter (TDC); reverse start-stop; high-speed image reconstruction. Therefore the camera is able to handle a large amount of uncorrelated noise.



a) SPAD camera prototype for direct ToF



b) 2D/3D setup c) 2D snapshot d) 3D snapshot

Fig. 1 Demonstrator equipment and SPAD camera snapshot

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The SPAD camera prototype along with the calibration of the low illumination setup and snapshots of the reconstructed 2D and 3D images are reported in [1].

II. Demonstration Setup

The demonstration setup contains the following items: the prototype of the SPAD camera, a picosecond laser for d-ToF (Fig. 1 a)), a power supply module, a laptop PC and a light shielding box accommodating the demonstrator for single photon detection conditions.

III. Visitor Experience

Visitors can experience the performance of a SPAD camera prototype for 2D/3D image streaming and real time temporal histogram building. They can interact with the demonstrator in order to understand the advantages and limitations of this technology. The visitors can see the dependence of the uncorrelated noise of the time-gated SPAD imager on the excess voltage. They can play with the number of inter-frames and excess voltage to have a better insight of the trade-off between image quality/accuracy and overall frame rate. Also they can monitor the inter-frame histogram of any pixel of the array while the reconstructed 2D or 3D images are displayed (Figs. 1 b), c) and d) respectively). Moreover, the visitors can choose to save a 2D video in raw format at 1kfps and play it in slow motion. The camera capabilities and the experiments that visitors can perform are shown by a video (verified with Media Player 12.0) available at:

https://www.dropbox.com/s/353rstcldqdmxy7/Demo_iscas2017_5min.wmv?dl=0

Earlier publication concentrates on different aspects of the design: the architecture of the SPAD imager and optical measurements of the SPAD and TDC ensemble along with measurements of the TDC array time resolution programmability are presented in [2]. The voltage reference is implemented by a PLL. It is globally compensated for process parameter, voltage supply and temperature variations. The design and characterization of the voltage-controlled ring-oscillator is reported in [3]. The calibration of the sensor with the characterization of the SPAD detectors is presented in [4].

References

[1] I. Vornicu, R. Carmona-Galan, A. Rodriguez-Vazquez, “Photon counting and direct ToF camera prototype based on CMOS SPADs”, *Int. Symp. on Circ. and Syst.*, to be published, 2017

[2] I. Vornicu, R. Carmona-Galan, A. Rodriguez-Vazquez, “A SPAD-based 3D imager with in-pixel TDC for 145ps-accuracy ToF measurement”, *IS&T/SPIE Electr. Imag.: Image Sens. and Imag. Syst., Proc. of SPIE*, San Francisco, California (USA), Vol. 9403, pp. 94030I.1-6, Feb. 2015

[3] I. Vornicu, R. Carmona-Galan, A. Rodriguez-Vazquez, “In-pixel voltage-controlled ring-oscillator for phase interpolation in ToF image sensors”, *Int. Symp. on Circ. and Syst.*, pp. 1906-1909 , May 2016

[4] I. Vornicu, R. Carmona-Galan, A. Rodriguez-Vazquez, “On the calibration of a SPAD-based 3D imager with in-pixel TDC using a time-gated technique”, *Int. Symp. on Circ. and Syst.*, pp. 1102-1105, May 2015