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ABSTRACT

The design and measurements of a CMOS 64×64 Single-Photon Avalanche-Diode (SPAD) array with in-pixel Time-to-Digital Converter (TDC) are presented. This paper thoroughly describes the imager at architectural and circuit level with particular emphasis on the characterization of the SPAD-detector ensemble. It is aimed to 2D imaging and 3D image reconstruction in low light environments. It has been fabricated in a standard 0.18μm CMOS process, i. e. without high voltage or low noise features. In these circumstances, we are facing a high number of dark counts and low photon detection efficiency. Several techniques have been applied to ensure proper functionality, namely: i) time-gated SPAD front-end with fast active-quenching/recharge circuit featuring tunable dead-time, ii) reverse start-stop scheme, iii) programmable time resolution of the TDC based on a novel pseudo-differential voltage controlled ring oscillator with fast start-up, iv) a global calibration scheme against temperature and process variation. Measurements results of individual SPAD-TDC ensemble jitter, array uniformity and time resolution programmability are also provided.

Keywords: 3D vision, time-to-digital converter, time interpolation, time gating, time-of-flight, single-photon avalanche diode, PVT calibration, reverse start-stop

1. INTRODUCTION

Single-photon avalanche-diodes can be employed to detect the arrival of a reflected pulse of light, thus emerging as a feasible alternative for generating a depth map of the scene[1]. SPADs arranged in a bi-dimensional array can effectively associate an estimation of the ToF[2] to each point in the image. Apart from this, ToF measurement can be also applied to Positron Emission Tomography (PET)[3],[4] and to other biomedical techniques using a faint light source like Fluorescence Lifetime Imaging (FLIM)[5]. Amongst the major limitations for ToF estimation are *background illumination*, and the *time resolution* of the detection. In this paper, we are dealing with both problems. In order to cancel the influence of background illumination, we will make use of time-gating techniques. For an accurate time stamping of the detected events we have incorporated in-pixel 11b-resolution TDCs. The sensor chip, containing 64×64 pixels, has been designed in a 0.18μm standard CMOS technology, with a pixel pitch of 64μm (Fig. 1). Each pixel contains a SPAD, an active quenching and recharge circuit with adjustable dead time and a TDC based on a ripple counter and the interpolation of the phases of a Voltage-Controlled Ring Oscillator (VCRO). The counter generates the coarser bits of the time stamp, while the finer 3b are determined by properly encoding the phases of the VCRO. The resulting timestamp is stored in an in-pixel 11b static RAM for further readout. By interpolating the 8 phases of the VCRO, a minimum time bin of 145ps can be detected, with a power consumption of only 9μW per TDC, amongst the smallest reported and certainly the best time resolution/power consumption trade-off reported in this technology, to the best of our knowledge. The in-pixel TDC occupies a total of 1740μm² which is smaller than the state-of-the-art[2],[6]. In order to overcome global drift of process parameters, supply voltage and temperature variations, there is a PLL integrated on-chip that allows tuning the reference voltage for the array of VCROs. The measured standard deviation of the TDCs across the array is 19 codes, i. e. 1%. This figure has been evaluated at 90% of the full dynamic range, without applying any pixel-to-pixel calibration[7].

The rest of the paper is organized as follows. The next section thoroughly describes the operation of the single-photon avalanche diode and its quenching/recharge circuits. The third section describes the in-pixel TDC and the PLL-based global calibration scheme. The fourth section reports several experimental results.
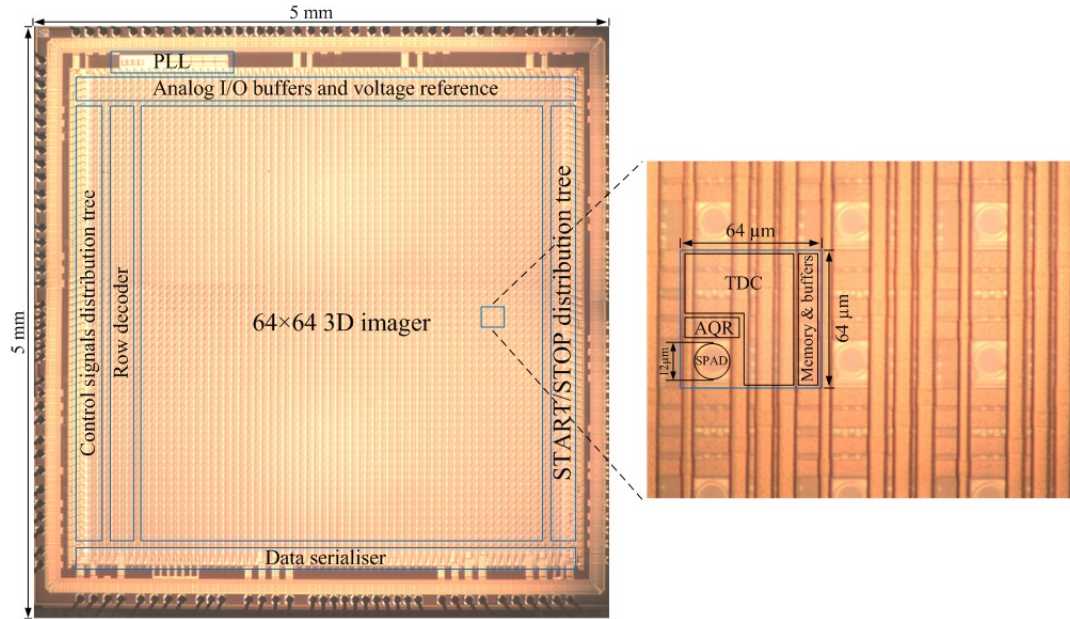
Fig. 1   Chip microphotograph

2.   SINGLE-PHOTON AVALANCHE DIODE AND ACTIVE QUENCHING CIRCUIT

A single-photon avalanche-diode is a *pn*-junction reversed biased beyond its break down voltage (V_{BD})[8]. The proper biasing and the principle of operation are explained in Fig. 2. Before any photon is detected no current flows through the *pn*-junction. This is indicated by label ① in the I-V characteristic of the diode (Fig. 2(b)). At this point, the detector is sensitive to any influence that can trigger an avalanche, e. g. an impinging photon or thermal agitation. The bias voltage at the cathode of the diode, V_{SPAD}, exceeds V_{BD} by an amount V_E, precisely named excess voltage. When a photon hits the diode surface, it will be detected with a probability that depends on the impact ionization coefficient and the absorption region[9]. At the space-charge region, the photon detection probability (PDP) is the product of the photon absorption probability and the avalanche triggering probability. At the neutral region the PDP depends also on the collection efficiency. These carriers give a slow component in the temporal response, known as diffusion tail.
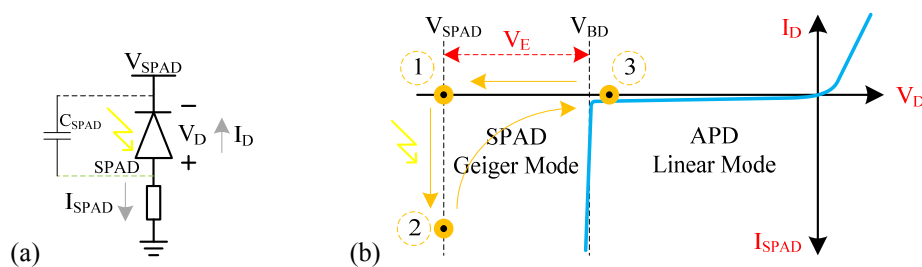

Fig. 2   Principle of operation of a single photon avalanche diode

The detected photon triggers an avalanche current, I_{SPAD}, which is almost instantaneously built up through the SPAD junction, point ②. In order to avoid any damage to the device, the avalanche current must be quenched. This is done by the quenching resistor illustrated in Fig. 2(a). The voltage drop on the diode starts to decrease down to below V_{BD}, reaching ③. When I_{SPAD} goes below the latching current[10], the avalanche is turned-off. Further, the voltage at the cathode starts building up in the recharge phase until it reaches ① again. Besides photons, avalanche currents can be also triggered by spurious factors which constitute the noise of a SPAD, e.g. dark counts or afterpulsing[10].

An active quenching/recharge circuit (AQC) (Fig. 3) —already reported[7]—, has been incorporated to each pixel, substituting the ballast resistor of Fig. 2(a). This circuit permits minimizing the time in which the SPAD is inoperative

by reducing the recharge time. It limits the magnitude of the avalanche current, reducing the power consumption of the detector. It can also help reducing afterpulsing events by selecting the appropriate dead-time. Another capability incorporated is the possibility to implement time-gating, thus reducing the influence of dark counts. The characteristics of the AQC are an area of $12 \times 22 \mu m^2$; a time delay between the arrival time of a detected photon and the positive edge of the output pulse of 100ps; a tunable dead time ranging from 5 to 540ns; and an average dynamic power consumption of 2.5μW drawn from the 1.8V supply at 1MHz count rate. The detector does not consume static power. Very low average current is drawn from V_{SPAD+} thanks to the quenching circuit that limits effectively the avalanche current.
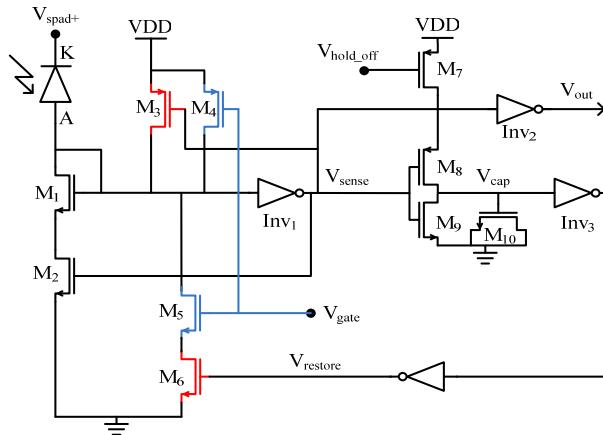

Fig. 3   Schematic of the time-gated active quenching/recharge circuit

Gating the front-end of the detector is implemented by transistors M_4 and M_5. This is a power efficient approach because the SPADs are enabled just for a short time window during the measurement. The SPAD array is turned-off most of the time required for readout.

3.   IN-PIXEL TIME-TO-DIGITAL CONVERTER

In order to determine the time interval delimited by the synchronization signal of the pulsed laser driver and the output pulse of the SPAD, a time-to-digital converter (TDC) is incorporated to each pixel. In order to efficiently save power, a reverse start-stop scheme is employed. In this case the in-pixel TDC is triggered by the detection of a photon and stopped by the synchronization signal. The actual ToF is directly computed by subtracting the measured time interval from the laser diode period. In order to achieve sub-nanosecond accuracy, the counter needs to be combined with time interpolation techniques. Each TDC (Fig. 4) is built by a control logic unit, a ring oscillator (RO), a coarse 8b ripple counter and an encoder that obtains the finer 3b from the phases of the RO. The first block implements the start/stop logic. It permits using the TDC in two different modes: ToF estimation and photon counting. In the first mode, the oscillator is started by the first positive edge of Vout, and stopped by the positive edge of the Ext_Stop synchronization signal. An external start signal, Ext_Start, is also provided for testing purposes. In the photon counting mode, the oscillator is by-passed and the output pulses of the SPAD directly feed the counter.
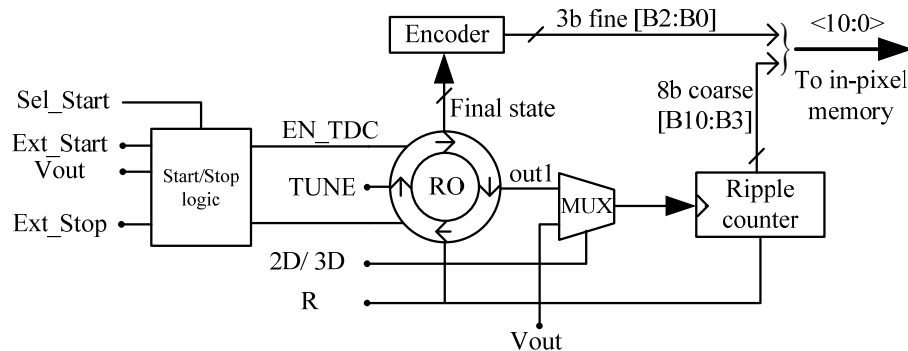

Fig. 4   In-pixel TDC block diagram

The RO is a pseudo-differential voltage-controlled ring-oscillator (VCRO)[11]. It provides fine time-to-digital conversion by applying phase interpolation. As long as the signal EN_TDC is active, the VCRO works at the frequency defined by the TUNE signal. This voltage reference is provided by an on-chip phase locked-loop (PLL). The finest time bin of the converter is given by the maximum oscillation frequency. Thus, the best time resolution of 145ps that has been measured is achieved with an oscillation frequency of 862MHz. The full range of the TDC is 297ns. Due to the reverse start-stop scheme, the maximum resolved distance is limited by the oscillator start-up. In this particular design, it is very fast, negligibly affecting the overall accuracy of the converter. The minimum measured distance is affected by the cumulative jitter of the oscillator which has been evaluated to be 15ps over 400 periods. On the positive edge of the Ext_Stop signal the oscillator is frozen. The digits at the ripple counter represent the eight most significant bits of the ToF estimation. The eight phases of the oscillator are passed through a thermometric-to-binary code converter to provide the three least significant bits.

The oscillation frequency of the VCROs in the array is controlled by a global calibration scheme (Fig. 5). A master VCRO is inserted into a PLL. The synthesized frequencies range from 400MHz to 850MHz with a step of 50MHz. The output voltage of the filter is used as a reference voltage for rest of the VCROs of the array, which are slaves in this sense of the master VCRO in the tuning loop. Therefore one of the most critical parts of the PLL design is to achieve a small ripple at the output of the loop filter. The impact of this ripple of the reference voltage on the time bin of the TDC can be evaluated from this expression:

$$V_\varepsilon = \frac{8KT_\varepsilon V_{ref}^2}{1 + 8KT_\varepsilon V_{ref}} \tag{1}$$

where V_ε, is the ripple of the output of the loop filter, T_ε is the error in the TDC time bin, K is the VCRO gain and V_{ref} is the output of the loop filter. In order to keep the time resolution error in picosecond range, for an oscillator gain of 440MHz/V, the voltage ripple at the slave oscillators control input needs to be smaller than 50mV.
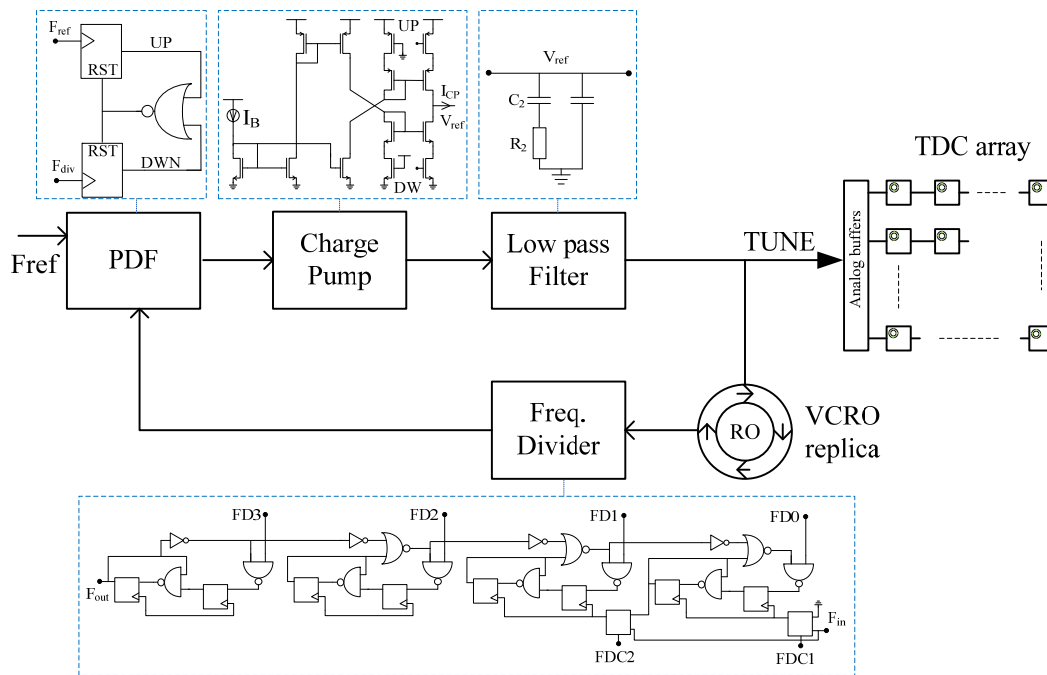

Fig. 5 Calibration block diagram against process and temperature variations

4. EXPERIMENTAL RESULTS

The experimental verification of the imager starts with the characterization of the SPAD as a single-photon detector. For this we have measured the photon detection efficiency (PDE) as the total count rate minus the DCR, divided by the expected arrival rate of the incoming photons[12]. In order to comply with the single photon detection conditions, the irradiance has to be set in the range of nW/mm². The average PDE is 6.5% at 520nm wavelength and 900mV excess

voltage. The excess voltage has been chosen to have the best time resolution and PDE while the dark count rate (DCR) is kept under a reasonable limit. Concerning DCR, in this technology we have a large doping concentration of the well implant. This is the origin of a reduced V_{BD}, 10.3V in our case. However, the contribution of the band-to-band tunneling becomes significant[13]. This measurement has been performed at 1V excess voltage. We have found that 70% of the pixels exhibits a DCR lower than 23kHz whilst the average DCR is 42kHz. Some of the pixels have an abnormal behavior, showing a DCR much larger than the rest of the array. These pixels represent about 1% of the imager. Accurate ToF estimation is successfully performed under these circumstances by 99.3% of the array, by applying a 420ns time-gating. The time resolution of the SPAD itself is given by the avalanche jitter which relies on the avalanche growth dynamics. Also the avalanche injection position statistics contribute to the photon-timing jitter. Its average value is about 224ps at 950mV excess voltage.

In order to demonstrate the efficiency of the time-gated operation of the sensor, the overall jitter of the SPAD-TDC ensemble and array uniformity have been measured (Fig. 6). The time resolution of the TDC is set to 160ps. The array of TDCs has been characterized using a picosecond time interval generator designed in-house[14]. The laser irradiance at 447nm is about 8nW/mm^2. The background light is about 15lux, meaning an equivalent irradiance of 30nW/mm^2 at the laser's wavelength. Therefore the amount of the uncorrelated light is much higher than the one provided by the illumination source. The aforementioned parameters are evaluated over 50kframes. The gating time is set to 420ns. As a design practice, most of the time it is easier to gate just the in-pixel counter and TDC. In this design, considering the high spurious count rate, the decision was to gate also the SPAD detector. This approach helps to drain significant less power from V_{SPAD+}.
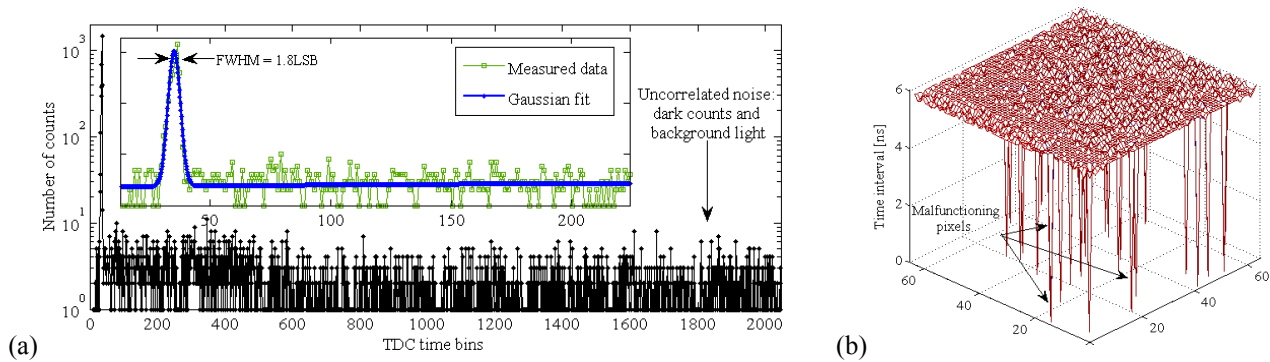

Fig. 6 (a) Jitter of the SPAD-TDC ensemble and (b) array uniformity with background light

As it was mentioned before in the previous section, the reference voltage of the array of VCROs is provided by an on-chip PLL. It can be employed as well to change the time resolution of the sensor by changing the loop division factor. Therefore, the time resolution range of the array of TDCs is between 147ps and 357ps (Fig. 7). The oscillation frequency of the TDC's core oscillator varies between 850MHz and 350MHz. The frequency divider of the PLL takes about 15.5μs to change its configuration, then the locking time is less than 3μs. Fig. 7(b) shows the change in frequency of the VCRO from the pixel (64, 64) when the loop division factor is changed from 15 to 8. Therefore the oscillation frequency jumps from 711MHz to 355MHz.
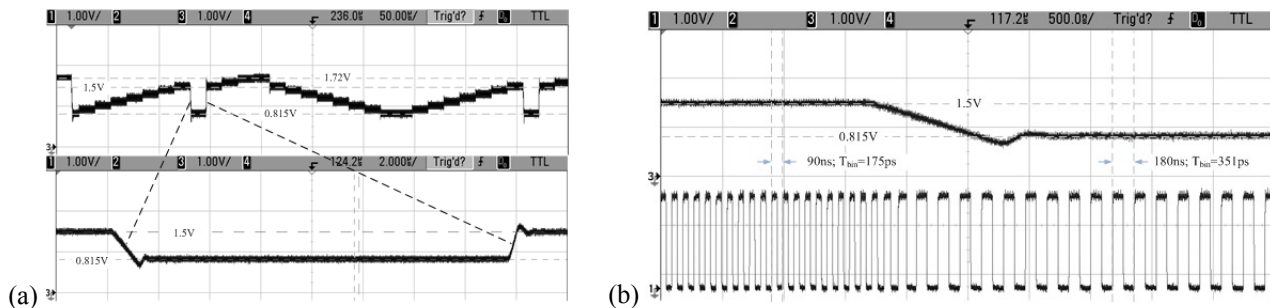

Fig. 7 Time resolution programmability (a) reference voltage (b) in-pixel VCRO frequency control

5. CONCLUSIONS

The functional description of a SPAD-based CMOS imager is presented together with some experimental results. It is able to capture either 2D images by merely counting photons or 3D images by measuring the ToF at pixel level. The core of the sensor is represented by 64×64 array of SPAD cells. Each cell contains the SPAD detector with an active quenching/recharge circuit, and a TDC. It has been fabricated in a standard 0.18μm CMOS process. Under these circumstances, the average DCR is about 42kHz. The minimum time resolution of a single TDC is about 145ps. The SPAD-TDC jitter is less than 290ps. Gating the front-end of the sensor, the power drained from V_{SPAD+} drops from 330mW to less than 10mW. Moreover, according to the measurement results, thanks to the time gating mechanism, the imager is able to properly operate even with a quite high DCR and 15lux background light.

ACKNOWLEDGMENTS

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