

# Conventional Space-Vector Modulation Techniques versus the Single-Phase Modulator for Multilevel Converters

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**Abstract**—Space-vector modulation is a well-suited technique to be applied to multilevel converters and is an important research focus in the last 25 years. Recently, a single-phase multilevel modulator has been introduced showing its conceptual simplicity and its very low computational cost. In this paper, some of the most conventional multilevel space-vector modulation techniques have been chosen to compare their results with those obtained with single-phase multilevel modulators. The obtained results demonstrate that the single-phase multilevel modulators applied to each phase are equivalent with the chosen well-known multilevel space-vector modulation techniques. In this way, single-phase multilevel modulators can be applied to a converter with any number of levels and phases avoiding the use of conceptually and mathematically complex space-vector modulation strategies. Analytical calculations and experimental results are shown validating the proposed concepts.

## I. INTRODUCTION

A GOOD design of the modulation strategy is needed in order to obtain high quality output waveforms in power converters. Pulse width modulation (PWM) and space-vector modulation (SVM) are the most important modulation techniques for power converters. In the last 25 years, a large number of PWM and SVM techniques reducing the computational complexity and achieving good results have been presented [1], [2]. PWM and SVM techniques have been compared demonstrating that both methods achieve high performance [3]–[6]. In fact, the design of new simple SVM techniques is an important research topic in last years.

The SVM techniques are based on the generation of the reference voltage as an average voltage between the possible discrete output voltages of the power converter over a switching period. In order to do it, the control region of a converter is plotted taking into account their output voltages locating the switching states (usually called state vectors) of the converter as can be observed in Fig. 1. The determination of the switching sequence and the switching times is usually reduced to a geometrical search of the nearest state vectors to the reference vector in this control region every switching

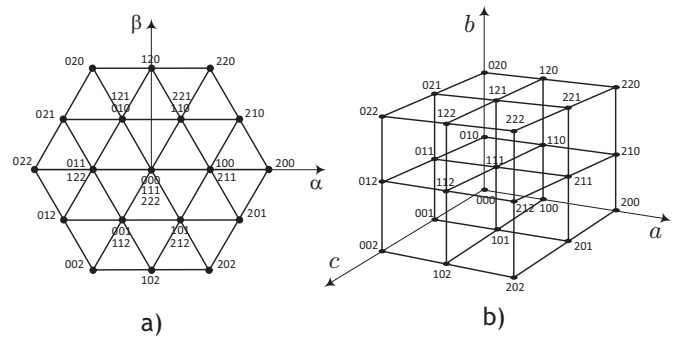


Fig. 1. Conventional control regions representations using a) two-dimensional SVM techniques b) three-dimensional SVM techniques

period. Several SVM techniques improve the mathematical calculations needed to determine these nearest state vectors and the switching times. When the converter has a higher number of levels or a higher number of phases, the representation of the control region becomes more complex and the SVM strategies have to consider a large number of switching states. In these cases, recent SVM techniques have achieved good experimental results without increasing the computational cost significantly [7]–[13].

This paper uses the simple single-phase multilevel modulators, (called 1DM in this paper and summarized in section III), introduced in [14] for power converters with any number of phases and levels per phase. In this paper, a comparison between the 1DM technique and the most conventional multilevel SVM methods is carried out. The aim of this paper is to demonstrate that the 1DM technique is equivalent to all those conventional SVM methods. In this way, simple single-phase multilevel modulators such as the 1DM method can be used to carry out the modulation for each phase of the converter avoiding the use of conceptually complex modulators which work with the complete power converter. The equivalence between the 1DM technique and the most conventional SVM methods makes that all the comparisons of these well-known SVM techniques with the classical multi-carrier PWM methods can be directly applied to evaluate the 1DM technique performance. Finally, as an additional advantage, it can be noticed that each phase of the converter could have any topology and any number of levels without introducing extra complexity in the modulation calculations.

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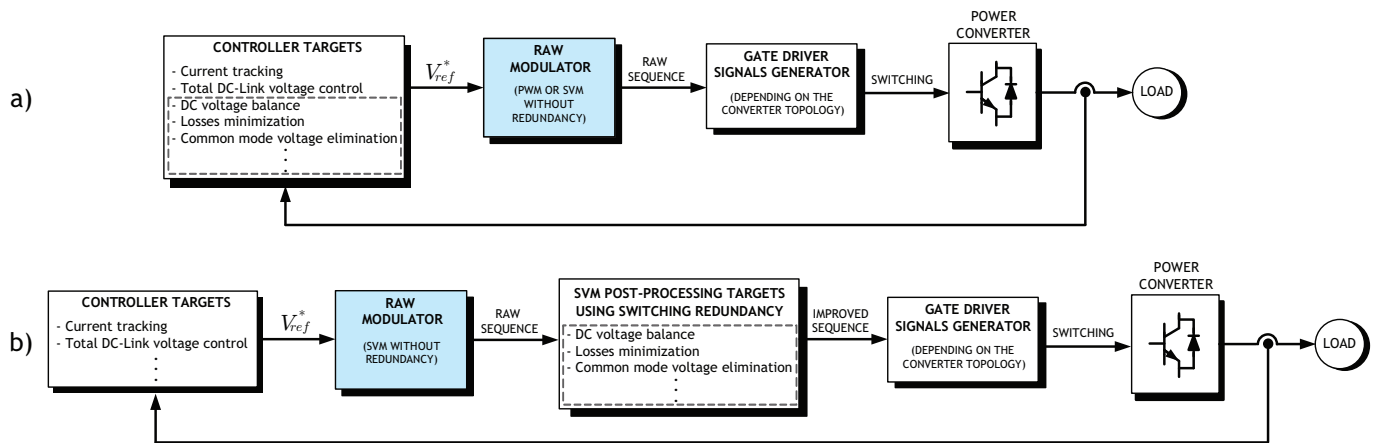


Fig. 2. Different solutions to design an indirect controller plus a modulator. From top to bottom: a) Controller dealing with many control targets plus a simple modulator b) Controller dealing with only primary targets plus a SVM modulator including the redundancy property in a post-processing block to achieve some secondary control targets.

Two different options can be considered when a digital indirect controller plus modulator system is designed to be applied to a power converter. Firstly, as shown in Fig. 2a, a possible option is to design an indirect controller that deals with issues such as the total dc voltage regulation, current tracking, common mode voltage elimination, dc voltage balancing, losses minimization, etcetera. The output of this indirect controller is the desired reference voltage  $V_{ref}^*$  that is sent to the modulator. PWM modulators or SVM techniques without using the redundancy properties can be used obtaining a switching sequence with similar results [4]. Finally, this switching sequence is the input of a gate driver generator block where the switching of the power semiconductors is obtained depending on the power converter topology. An example of this solution shown in Fig. 2a was introduced in [15] where an overview of PI solutions to control the dc voltages of single-phase multilevel cascaded converters is addressed. In this reference, the PI controllers generate the desired reference voltage achieving the dc voltage control and conventional PWM is used as modulation technique to generate the gate driver signals.

A second option is illustrated in Fig. 2b where the indirect controller delegates some secondary control issues to the modulator. Usually, the modulator can deal with the dc voltage balancing, the losses minimization or the common mode voltage elimination [16]–[18]. In this case, the simplified controller also generates a desired reference voltage  $V_{ref}^*$  what is the input of a SVM modulator where the redundancy property is exploited in order to achieve the secondary control objectives. This is represented in Fig. 2b using two consecutive blocks (a raw SVM modulator without the redundancy and a post-processing block where the redundancy is exploited in order to achieve the control targets) but usually in the literature these two blocks are presented as a unique new SVM modulation technique. Finally the improved switching sequence, where all the control objectives have been considered, is again the input of the gate driver generator block to obtain the power semiconductors switching depending on the converter topology. An example of this solution shown

in Fig. 2b was introduced in [18] where a SVM modulator controls the dc voltage balance of a three-level neutral-point-clamped converter using the redundancy property. The external controller would take care of the current tracking, the total dc voltage regulation, etcetera.

This paper is focused on a comparison of raw SVM techniques painted blue in both Fig. 2a and Fig. 2b. Raw modulation techniques means that the switching sequence and the switching times are determined without adding any post-processing in order to achieve secondary control targets such as the dc voltage balancing, the losses minimization or the common mode voltage elimination, etcetera. In this paper, the post-processing of the switching sequence using the redundancy property is not exploited. Anyway, it should be noticed that in this paper it will be demonstrated that the IDM technique is a raw modulation technique that naturally achieves the common mode voltage elimination without any post-processing.

This paper is organized as follows: In section II the most common SVM techniques for multilevel multiphase converters are summarized. These converter topologies can be modulated using the single-phase multilevel modulator summarized in section III and called IDM in this paper. A comparison between the IDM technique and the conventional SVM techniques is studied in section IV. The experimental results of all the studied SVM techniques is presented in section V showing the exact equivalence between the IDM technique and the previous well-known modulation methods. Finally, the conclusions of this work are addressed in section VI.

## II. COMMON SPACE-VECTOR MODULATION TECHNIQUES FOR MULTILEVEL MULTIPHASE CONVERTERS

In general, SVM techniques can be classified in three main groups depending on the number of phases of the converter and depending on the coordinates used to plot the control region of the converter.

### A. SVM techniques based on two-dimensional control regions

The conventional way to introduce a SVM technique for a three-phase converter is based on a two-dimensional (2D) representation of the control region of the converter using the  $\alpha$ - $\beta$  plane [19]. As an example, the 2D control region of a three-phase three-level converter is represented in Fig. 1a. In these SVM techniques, the calculations lead to determine the switching sequence formed by three state vectors with their corresponding switching times.

In [20], a good summary of the most used two-dimensional SVM techniques is carried out. Among these strategies, one of the most cited SVM techniques using a 2D control region was introduced in [21]. This technique is called 2D-SVM in this work and will be used for comparison purposes in next sections. In the 2D-SVM technique, a simple mathematical frame transformation to a new  $h$ - $g$  frame is carried out in order to simplify the calculations of the SVM technique. After that, a geometrical search is carried out to determine the triangle where the reference vector is located. The final switching sequence and the switching times are easily calculated.

### B. SVM techniques based on three-dimensional control regions

SVM techniques designed taking into account the control region represented in the  $\alpha$ - $\beta$  plane are well suited for converter topologies where the zero sequence voltage and the zero sequence current are zero and therefore their  $\gamma$  components are zero. However, some converter topologies such as the three-phase four-wire [22], [23] and four-phase four-wire topologies [24], [25] present zero sequence voltages and zero sequence currents in general different to zero. In these cases, SVM techniques have to consider the three components  $\alpha$ ,  $\beta$  and  $\gamma$  to carry out the modulation without errors. The easiest way to design a SVM technique using three components is to use the natural coordinates  $abc$  because, in this case, the control region is formed by regular volumes simplifying the necessary calculations. This concept is shown in Fig. 1b where the control region of a three-phase three-level converter is shown. It can be noticed that the three-dimensional based SVM techniques are an extension of the 2D based SVM techniques and they can be applied without restrictions to any power converter topology with or without zero sequence components.

As an example, the well known three-dimensional SVM using  $abc$  coordinates introduced in [26] (and called 3D-SVM in this work) will be used for comparison purposes in next sections. This 3D-SVM technique is based on a normalization of the reference voltage and a simple geometrical search of the tetrahedron where the normalized reference vector is located. The final switching sequence formed by the four nearest state vectors and their corresponding switching times are calculated with simple mathematical expressions.

### C. SVM techniques for multilevel multiphase converters

The previous SVM techniques including the 2D-SVM and the 3D-SVM can be only applied to three-phase multilevel converters. The graphical representation of the control region,

present on three-phase converters, is lost when the number of phases increases. For a higher number of phases, new modulation techniques have been designed in last years [7]–[13]. For instance, an interesting method is the generalized SVM technique for multiphase multilevel converters introduced in [13] and called M-SVM in this paper. The M-SVM method solves the modulation problem of multiphase multilevel converters by using matrix calculations in order to determine the switching sequence and the switching times to generate the reference voltage for each phase.

Summarizing the M-SVM method concepts, it solves a system of linear equations in order to generate the reference voltage of each phase average over a switching period. In the first step, a normalization of the reference voltage is done and all the calculations are written in matrix format. Using the M-SVM technique, the multiphase multilevel modulation problem is reduced to a multiphase two-level problem using simple calculations determining a normalized two-level reference vector. Depending on the number of phases of the converter, a specific number of cases have to be studied (6 cases for three-phase systems, 24 cases for four-phase systems, etc). In order to determine the case to apply, the magnitude of components of the normalized two-level reference vectors has to be compared leading to determine a two-level sorted normalized reference vector. Matrix  $\mathbf{D}$  is the coefficient matrix that is the solution of the switching sequence of the two-level modulation. A simple addition is used to determine the final switching sequence formed by  $M+1$  vectors for a  $M$ -phase converter. The corresponding switching times are calculated by means of the sorted two-level reference vector. The M-SVM is simple but it should be noticed that the number of cases highly increases when the number of phases is increased.

## III. SIMPLE MODULATION TECHNIQUE FOR SINGLE-PHASE MULTILEVEL CONVERTERS

In this paper, the single-phase multilevel modulation technique introduced in [14], and called IDM in this paper, has been chosen to compare its results with the most common multilevel modulation techniques introduced in the previous section. The IDM technique can be applied to any single-phase multilevel converter and only the final trigger signals depend on the multilevel converter topology. The IDM technique is based on the generation of the reference phase voltage as an average of the nearest voltage levels of the phase. The single-phase modulation problem is reduced to very simple calculations determining easily the switching sequence (formed by two switching states) and the corresponding switching times.

In order to briefly introduce the IDM technique, the flow diagram to determine the switching sequence and the switching times for a phase  $p$  is shown in Fig. 3 [14]. The reference voltage of phase  $p$  is defined as  $V_{ref}^p$  and is normalized using the dc voltage step of the phase  $E_p$  determining the positive normalized reference voltage  $a_p$ .  $E_p$  is defined as the voltage between two consecutive voltage levels assuming that it is constant. The maximum voltage that can be obtained in phase  $p$  is called  $V_{max}^p$ . Using factor  $a_p$  and its integer part  $a_{pi}$ , the IDM technique easily calculates the switching sequence and

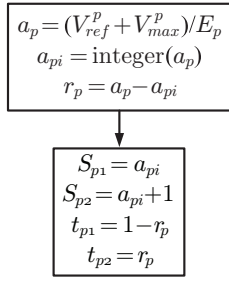


Fig. 3. Flow diagram of the generalized IDM technique for single-phase multilevel converters

TABLE I  
SWITCHING SEQUENCE AND SWITCHING TIMES DETERMINED BY THE IDM TECHNIQUE FOR A THREE-PHASE SYSTEM

Phase 1	Phase 2	Phase 3
$S_{11} = a_{1i}$	$S_{21} = a_{2i}$	$S_{31} = a_{3i}$
$S_{12} = a_{1i} + 1$	$S_{22} = a_{2i} + 1$	$S_{32} = a_{3i} + 1$
$t_{11} = 1 - r_1$	$t_{21} = 1 - r_2$	$t_{31} = 1 - r_3$
$t_{12} = r_1$	$t_{22} = r_2$	$t_{32} = r_3$

the switching times. The final switching sequence of phase  $p$  is formed by two switching states  $S_{p1}$  and  $S_{p2}$  with normalized switching times  $t_{p1}$  and  $t_{p2}$  respectively fulfilling that  $t_{p1} + t_{p2} = 1$ . As a summary, it can be noticed that the switching sequence is always formed by two switching states equal to  $a_{pi}$  and  $a_{pi} + 1$  with switching times  $1 - r_p$  and  $r_p$  respectively where  $r_p$  is determined as  $a_p - a_{pi}$ . The results of these calculations are summarized in Table I. The computational cost of the IDM technique is independent of the number of levels and the necessary calculations are extremely simple.

#### IV. COMPARISON BETWEEN THE IDM AND OTHER WELL-KNOWN SVM TECHNIQUES FOR MULTILEVEL CONVERTERS

A comparison between the IDM and some of the most well-known SVM techniques for multilevel converters is presented in this section. The study is based on the comparison of the resulting switching sequence and the switching times of the previous SVM techniques with those obtained using the IDM technique. Different SVM techniques have been chosen to carry out the comparison with the IDM technique. Some of them are focused on three-phase systems [21], [26] and others are especially designed for a higher number of phases [13].

##### A. Comparison with the 2D-SVM technique

The 2D-SVM technique introduced in [21] is compared with the IDM using the example presented by its authors. In the example reported in [21], the line-to-line voltage of a three-phase three-level converter is the reference vector to be modulated by the 2D-SVM technique. In the example, it is considered the instantaneous reference

$$V_{ref} = 1.8V_{dc} \begin{bmatrix} 0.643 \\ 0.342 \\ -0.985 \end{bmatrix}. \quad (1)$$

The 2D-SVM technique determines the switching sequence formed by three state vectors  $S_1$ ,  $S_2$  and  $S_3$  (one of them is a redundant state vector) and their corresponding switching times  $t_1$ ,  $t_2$  and  $t_3$  [21].

$$\begin{aligned} S_1, S_2, S_3 &= 100/211, 200, 210 \\ t_1 &= 0.227 \\ t_2 &= 0.157 \\ t_3 &= 0.616 \end{aligned} \quad (2)$$

The same example can be applied to the IDM technique considering each phase independently. The IDM technique uses the phase-to-neutral voltages as the reference voltages to be generated by the single-phase systems. The corresponding phase-to-neutral reference vector  $V_{refn}$  of the example is

$$V_{refn} = \begin{bmatrix} V_{ref}^1 \\ V_{ref}^2 \\ V_{ref}^3 \end{bmatrix} = V_{dc} \begin{bmatrix} 0.9768 \\ -0.1806 \\ -0.7962 \end{bmatrix}. \quad (3)$$

Each component of the  $V_{refn}$  vector is applied as the reference voltage to be modulated for the IDM technique using the flow diagram shown in Fig. 3. In this case,  $E_p$  and  $V_{max}^p$  are equal to  $V_{dc}$  volts because the example considers a three-level converter which can generate output voltages  $-V_{dc}$ , 0 and  $V_{dc}$ . The resulting switching sequences determined by the IDM technique for each phase are summarized in Table II.

The switching sequence determined by the 2D-SVM technique is formed by the switching states of the three phases. On the other hand, the switching sequence obtained by using the IDM is a single-phase switching sequence. The corresponding three-phase switching sequence can be obtained using the data summarized in Table II determined by the IDM method but considering the three independent phases together. In this way, the switching sequence described in Table II can be rewritten in three-phase format as follows:

$$\begin{aligned} S_1, S_2, S_3, S_4 &= 100, 200, 210, 211 \\ t_1 &= 0.0232 \\ t_2 &= 0.1086 - 0.0232 = 0.1574 \\ t_3 &= 0.7962 - 0.1086 = 0.6156 \\ t_4 &= 1 - t_1 - t_2 - t_3 = 0.2038 \end{aligned} \quad (4)$$

As can be observed, switching sequences calculated using the 2D-SVM technique (2) and determined by the IDM

TABLE II  
SWITCHING SEQUENCE AND SWITCHING TIMES DETERMINED BY THE IDM TECHNIQUE FOR THE EXAMPLE INTRODUCED IN [21]

Phase 1	Phase 2	Phase 3
$S_{11} = 1$	$S_{21} = 0$	$S_{31} = 0$
$S_{12} = 2$	$S_{22} = 1$	$S_{32} = 1$
$t_{11} = 0.0232$	$t_{21} = 0.1806$	$t_{31} = 0.7962$
$t_{12} = 0.9768$	$t_{22} = 0.8194$	$t_{32} = 0.2038$

technique (4) do not coincide apparently. In the 2D-SVM technique, the switching sequence has a redundant vector (100/211) and the corresponding switching time can be shared between both redundant vectors as desired. The 2D-SVM technique does not impose any restriction in the sharing of the time between both vectors. On the other hand, from the 1DM technique results, the switching times corresponding to states 100 and 211 is equal to  $t_1$  and  $t_4$  respectively. If these two switching times are added, the resulting time is  $t_1 + t_4 = 0.227$  what exactly coincides with the switching time of the state  $S_1$  determined by the 2D-SVM technique in (2). So, the 1DM technique is equivalent to the 2D-SVM method but the resulting switching sequence intrinsically achieves an objective: the common mode voltage elimination.

1) *Analysis of the Resulting Switching Sequence of the 1DM Technique:* As has been explained above, the 1DM technique determines the switching states using the flow diagram shown in Fig. 3 for each phase of the converter. In the 1DM technique, as the phase-to-neutral voltage is applied as the reference voltage to be generated, the common mode voltage is zero because the voltage from the neutral point of the load to the middle point of the dc-link voltage is inherently imposed to be zero. This common mode voltage can be calculated as

$$V_{no} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) \quad (5)$$

and in the example case, the common mode voltage of the switching sequence described in (4) is

$$\begin{aligned} V_{no} &= \frac{1}{3}(t_{11} * 0 + t_{12} * V_{dc}) + \\ &+ \frac{1}{3}(t_{21} * (-V_{dc}) + t_{22} * 0) + \\ &+ \frac{1}{3}(t_{31} * (-V_{dc}) + t_{32} * 0) = \\ &= 0.9768 * V_{dc} - 0.1806 * V_{dc} - 0.7962 * V_{dc} = 0 \quad (6) \end{aligned}$$

As has been commented above, the time of the redundant vectors 100 and 211 using the 1DM technique summarized in (4) is  $t_1 + t_4 = 0.227$  what coincides with the time of the redundant vectors using the 2D-SVM technique written in (2). So, the 1DM technique achieves the same switching sequence determined by the 2D-SVM technique but using both redundant vectors properly to eliminate the common mode voltage. Anyway, if this condition were not required, the times of the redundant vectors determined by the 1DM technique could be shared as desired. For instance, using the SVM technique introduced in [27], the redundancy property is exploited in order to form symmetrical switching sequences where the switching times of the first and last switching vectors are the same.

### B. Comparison with the 3D-SVM technique

In [26], a generalized and simple 3D-SVM technique is presented for three-phase multilevel converters. The results of this modulation technique are summarized in Table III where the possible switching sequences and the corresponding

switching times are written depending on six different types of tetrahedrons where the reference vector is located.

The switching sequence determined by the 3D-SVM technique is formed by four switching states  $S_1, S_2, S_3$  and  $S_4$  with switching times  $t_1, t_2, t_3$  and  $t_4$  respectively. The integer parts of the normalized reference voltage defined in [26] as  $a, b$  and  $c$  for the three phases coincide with factors  $a_{1i}, a_{2i}$  and  $a_{3i}$  of the 1DM technique. On the other hand,  $r_a, r_b$  and  $r_c$  coincide with factors  $r_1, r_2$  and  $r_3$  of the 1DM technique.

In order to make a comparison between the 3D-SVM and the 1DM techniques, each phase of the three-phase multilevel converter is studied depending on the tetrahedron case. For instance, for the tetrahedron case 1 from Table III and studying phase 1, the switching sequence is composed of switching states  $a$  and  $a+1$ . The switching time of switching state  $a$  is  $t_1 = 1 - r_a$  and the switching time for switching state  $a+1$  is  $t_2 + t_3 + t_4 = r_a$ . It can be noticed that this switching sequence and the switching times for phase 1 exactly coincide with the result obtained using the 1DM technique for phase 1 shown in Table I. This calculation can be repeated considering phases 1, 2 or 3 and all the tetrahedron cases achieving the same conclusion. In all cases, the switching sequence and the switching times determined by the 3D-SVM technique are the same than those obtained using the 1DM technique for each phase.

### C. Comparison with the M-SVM technique

In [28] it is demonstrated that the M-SVM technique is an extended SVM method from the 3D-SVM technique introduced in [26] obtaining the same results for three-phase

TABLE III  
SWITCHING SEQUENCE AND SWITCHING TIMES DEPENDING ON THE TETRAHEDRON CASE USING THE 3D-SVM TECHNIQUE [26]

Case	Switching sequence	Switching times
1	$S_1 = (a, b, c)$	$t_1 = 1 - r_a$
	$S_2 = (a + 1, b, c)$	$t_2 = r_a - r_c$
	$S_3 = (a + 1, b, c + 1)$	$t_3 = r_c - r_b$
	$S_4 = (a + 1, b + 1, c + 1)$	$t_4 = r_b$
2	$S_1 = (a, b, c)$	$t_1 = 1 - r_b$
	$S_2 = (a, b + 1, c)$	$t_2 = r_b - r_c$
	$S_3 = (a, b + 1, c + 1)$	$t_3 = r_c - r_a$
	$S_4 = (a + 1, b + 1, c + 1)$	$t_4 = r_a$
3	$S_1 = (a, b, c)$	$t_1 = 1 - r_c$
	$S_2 = (a, b, c + 1)$	$t_2 = r_c - r_a$
	$S_3 = (a + 1, b, c + 1)$	$t_3 = r_a - r_b$
	$S_4 = (a + 1, b + 1, c + 1)$	$t_4 = r_b$
4	$S_1 = (a, b, c)$	$t_1 = 1 - r_b$
	$S_2 = (a, b + 1, c)$	$t_2 = r_b - r_a$
	$S_3 = (a + 1, b + 1, c)$	$t_3 = r_a - r_c$
	$S_4 = (a + 1, b + 1, c + 1)$	$t_4 = r_a$
5	$S_1 = (a, b, c)$	$t_1 = 1 - r_c$
	$S_2 = (a, b, c + 1)$	$t_2 = r_c - r_b$
	$S_3 = (a, b + 1, c + 1)$	$t_3 = r_b - r_a$
	$S_4 = (a + 1, b + 1, c + 1)$	$t_4 = r_a$
6	$S_1 = (a, b, c)$	$t_1 = 1 - r_a$
	$S_2 = (a + 1, b, c)$	$t_2 = r_a - r_b$
	$S_3 = (a + 1, b + 1, c)$	$t_3 = r_b - r_c$
	$S_4 = (a + 1, b + 1, c + 1)$	$t_4 = r_c$

multilevel systems. In fact, Table III is introduced in both papers [26], [28] in order to show the equivalence between both SVM strategies when they are applied to three-phase converters. In [13], the generalized version of the M-SVM technique is introduced for any number of phases. In this section of the paper, a comparison between the M-SVM and the IDM techniques with more than three phases is done.

An example of the M-SVM technique is shown in [13] considering a five-phase five-level cascaded H-bridge converter. Each phase of the converter is formed by two H-bridges connected in series with the same value of dc voltage (20 volts). The reference voltage is a sinusoidal waveform for each phase between -40V and 40V. In [13], the following reference voltage is applied as the input of the M-SVM technique as an example:

$$V_r^p = [28.6, 22.6, -14.6, -31.6, -5.0]V \quad (7)$$

The obtained results from the M-SVM technique are shown in [13] and the switching sequence and the switching times are summarized in Table IV. In order to compare the results of the M-SVM and the IDM techniques, it should be noticed that phase state  $j$  in M-SVM technique is equivalent to phase state  $j+(N-1)/2$  in the IDM technique where  $N$  is the number of levels of each phase of the converter. This change has been already applied in Table IV. In the example case, the converter is composed by five-level phases and therefore  $N$  is equal to 5. In this way, phase states -2,-1,0,1,2 of M-SVM technique are equivalent to 0,1,2,3,4 in the IDM strategy.

The IDM technique is applied independently to each phase of the converter to obtain the switching sequence and the switching times for each phase using the same example. The summary of the calculations carried out by the IDM technique using the flow diagram represented in Fig. 3 is shown in Table V. In this case,  $E_p$  is equal to 20 volts and  $V_{max}^p$  is 40 volts.

At this point, results from Table IV can be considered studying each individual phase. For instance considering phase 1, the switching sequence is formed by phase states 3 and 4 and the switching times are  $t_1+t_2=0.57$  and  $t_3+t_4+t_5+t_6=0.43$  respectively. As can be seen from Table V, this result is identical to the obtained using the IDM technique for phase 1. Similar calculations can be done for all the phases and it can be seen that results from Table IV using the M-SVM and results from Table V using the IDM technique are the same.

TABLE IV  
SWITCHING SEQUENCE AND SWITCHING TIMES FOR THE FIVE-PHASE FIVE-LEVEL USING THE M-SVM TECHNIQUE. EXAMPLE SHOWN IN [13]

Switching state vector	Switching time
$S_1 = (3, 3, 1, 0, 1)$	$t_1 = 0.25$
$S_2 = (3, 3, 1, 0, 2)$	$t_2 = 0.32$
$S_3 = (4, 3, 1, 0, 2)$	$t_3 = 0.01$
$S_4 = (4, 3, 1, 1, 2)$	$t_4 = 0.15$
$S_5 = (4, 3, 0, 1, 2)$	$t_5 = 0.14$
$S_6 = (4, 4, 0, 1, 2)$	$t_6 = 0.13$

TABLE V  
SUMMARY OF THE CALCULATIONS USING THE IDM TECHNIQUE TO DETERMINE THE SWITCHING SEQUENCE AND THE SWITCHING TIMES FOR THE FIVE-PHASE FIVE-LEVEL EXAMPLE SHOWN IN [13]

Phase	1	2	3	4	5
$V_r^p(V)$	28.6	22.6	-14.6	-31.6	-5.0
$a_p$	3.43	3.13	1.27	0.42	1.75
$a_{pi}$	3	3	1	0	1
$S_{p1}$	3	3	1	0	1
$S_{p2}$	4	4	2	1	2
$t_{p1} = 1 - r_p$	0.57	0.87	0.73	0.58	0.25
$t_{p2} = r_p$	0.43	0.13	0.27	0.42	0.75

TABLE VI  
LABORATORY PROTOTYPE DETAILS

Half DC-Link capacitance ( $C_1, C_2$ )	3.3 mF
DC-Link voltage ( $V_{dc}=V_{C1}+V_{C2}$ )	50 V
Power semiconductors	SKM300GB123
Gate drivers	SKHI10/17
FPGA device	XC2S30-5TQ144C
DSP device	TMS320VC33

## V. EXPERIMENTAL COMPARISON BETWEEN THE SVM TECHNIQUES

The IDM technique applied to multiphase multilevel converters has been tested in a laboratory prototype in order to compare its results with those obtained using the most common multilevel SVM techniques. The details of the prototype are summarized in Table VI. As has been introduced above, applying the IDM to each phase of a power converter the obtained results are equivalent to those achieved by SVM techniques such as 2D-SVM, 3D-SVM and M-SVM.

In the experiments, the three-phase three-level diode-clamped converter represented in Fig. 4 is used as the experimental setup. Three pure 50 Hz sinusoidal references with a phase shift of  $120^\circ$  are applied as the reference voltage to be generated by the converter with modulation index equal to 0.78. The total dc-link voltage is 50 volts.

Firstly, the 2D-SVM and the IDM techniques are applied to determine the switching sequence and the switching times. The redundant switching vectors have been chosen in the same way using both modulation techniques. The experimental results are shown in Fig. 5 where the output modulated phase-to-phase voltage is represented using each modulation technique. The results show that the waveforms are identical demonstrating that both modulation techniques are equivalent. The switching frequency is 500 Hz in order to highlight the exact equivalence between both modulation techniques. This fact can be clearly observed from Fig. 6 where the harmonic spectrum of the phase-to-phase voltages using both techniques are represented using a switching frequency equal to 2 kHz. The total harmonic distortion (THD) of the obtained waveforms is equal to 20.2% taking into account the first 40 harmonics as defined in code EN50160. All the THD values present in this paper are calculated in the same way.

The same experiment has been carried out applying the 3D-SVM technique considering a low switching frequency equal to 500 Hz. The obtained results are shown in Fig. 7

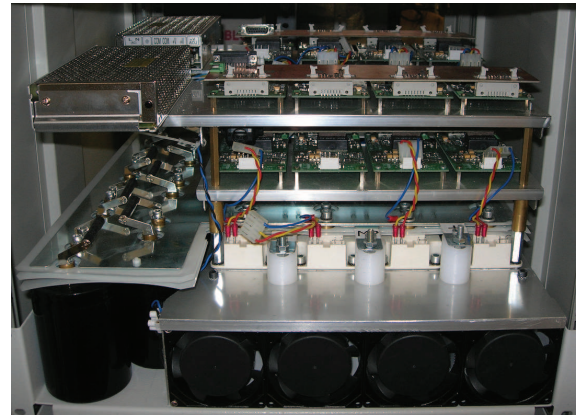
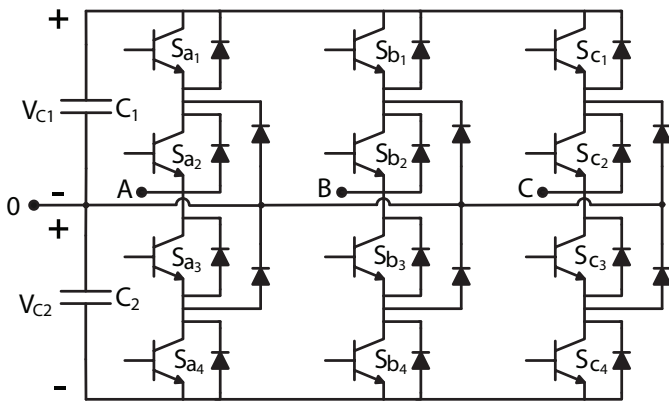
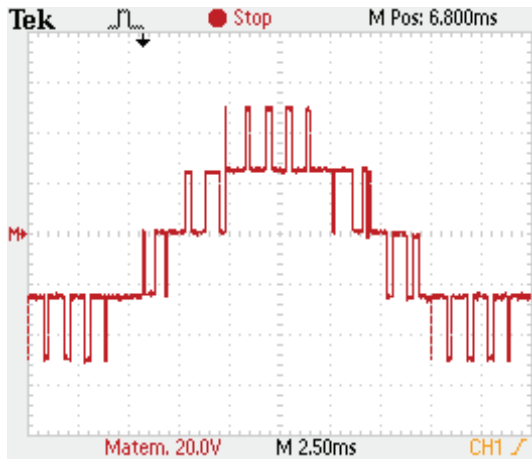
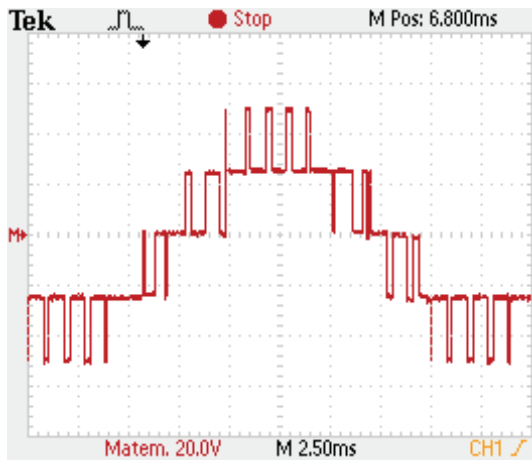


Fig. 4. Diagram and picture of the three-phase three-level diode-clamped converter experimental setup used to validate the proposed concepts.



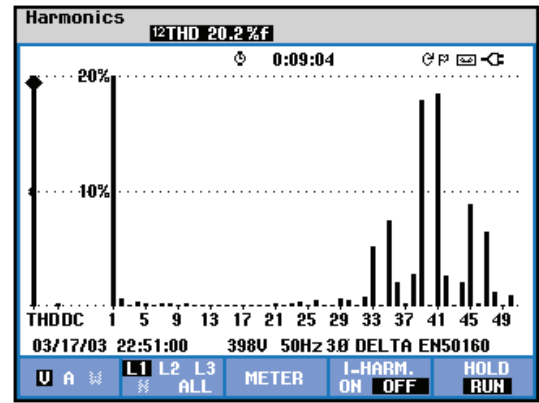
(a)



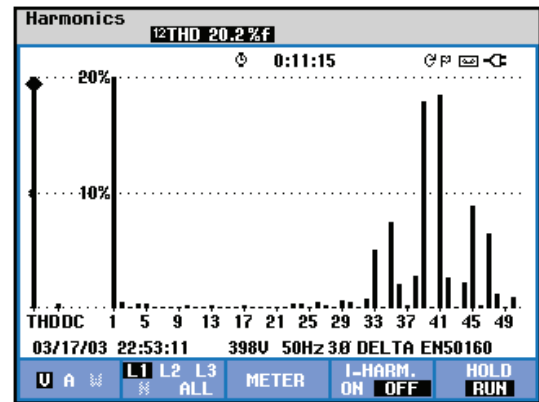
(b)

Fig. 5. From top to bottom: Phase-to-phase voltage achieved by the a) 2D-SVM technique b) IDM technique applied independently to the three phases

where it can be observed that the 3D-SVM and the IDM achieve the same results and therefore they are equivalent as expected. In this case, the redundant vectors are directly imposed by the modulation techniques. As a consequence, an exact equivalence of the harmonic spectrum using both techniques is achieved as well.



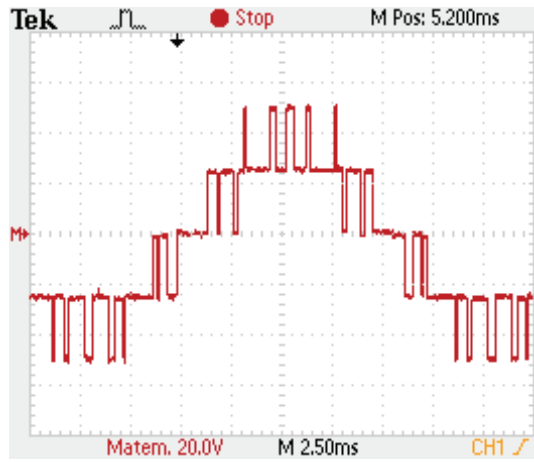
(a)



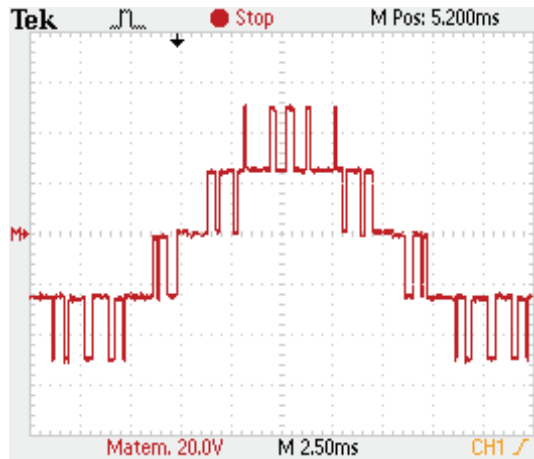
(b)

Fig. 6. From top to bottom: Harmonic Spectrum of the phase-to-phase voltage achieved by the a) 2D-SVM technique b) IDM technique applied independently to the three phases

Finally, in a new experiment, three pure 50 Hz sinusoidal references with a phase shift equal to  $2\pi/5$  and modulation index equal to 0.86 are used in order to emulate the operation of a five-phase three-level converter. In this case, the switching frequency is 2.5 kHz. The phase voltages using the IDM technique and these voltages filtered using a low pass filter are shown in Fig. 8. It can be seen that the IDM strategy applied to each phase of the converter achieves high quality results



(a)



(b)

Fig. 7. From top to bottom: Phase-to-phase voltage achieved by the a) 3D-SVM technique b) 1DM technique applied independently to the three phases

with very low conceptual complexity. The harmonic spectrum of a phase voltage is represented in Fig. 9 achieving a THD equal to 3.22%. In addition, as the reference of each phase can be modulated independently using the 1DM technique, in a second experiment, a 60% of third harmonic content is added to the voltage reference of phase  $a$ . The obtained results are shown in Fig 10 where it can be observed that the phase voltages are generated with high quality as well. This experiment also highlights the good performance of the 1DM technique when the reference voltages are not purely sinusoidal. Therefore, the 1DM technique can be applied to power converters with or without neutral connection and with balanced or imbalanced loading conditions. This cannot be achieved by the 2D-SVM where the  $\gamma$  component of the reference voltage is not controlled.

## VI. CONCLUSIONS

In the last 25 years, a lot of space vector modulation techniques have been designed improving step by step its computational cost and simplicity. A simple modulation technique called 1DM published in [14] has been recently introduced for single-phase multilevel converters (two-level ones as well)

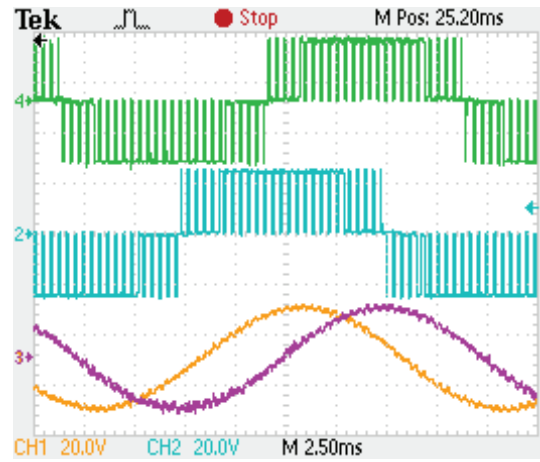


Fig. 8. Phase voltages achieved by the 1DM technique applied independently to each phase. The references are purely 50 Hz sinusoidal with modulation index equal to 0.86 and phase shift equal to  $2\pi/5$ .

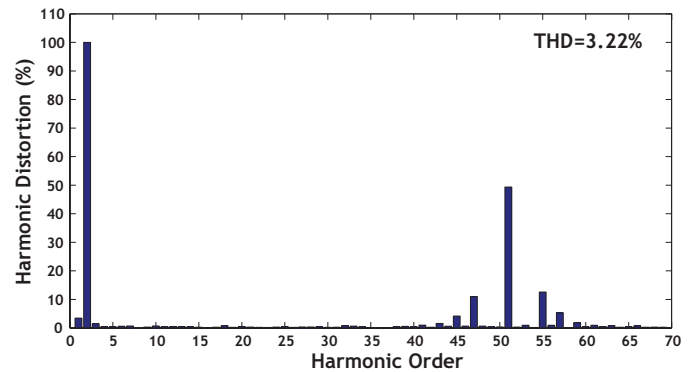


Fig. 9. Experimental harmonic spectrum of the phase voltage of experiment shown in Fig. 8.

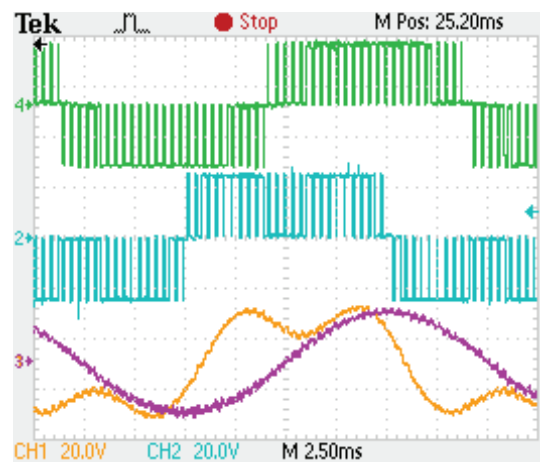


Fig. 10. Phase voltages achieved by the 1DM technique applied independently to each phase. The references are 50 Hz sinusoidal, modulation index equal to 0.86, phase shift equal to  $2\pi/5$  (to emulate a five-phase converter) and 60% of third harmonic content in phase  $a$ .

outstanding its conceptual and mathematical simplicity. In this paper, it is demonstrated that this 1DM technique achieves the same results compared with some of the most conventional and well-known multilevel SVM techniques for three-phase systems and for multiphase converters in general. The 1DM



technique is applied to each phase independently while the conventional SVM techniques consider the converter as a complete system. The IDM technique is fully equivalent to these previous SVM strategies for multilevel converters achieving the same results. Besides, the equivalence between the IDM technique and the most conventional SVM methods makes that all the comparisons of these well-known SVM techniques with the classical multi-carrier PWM methods can be directly applied to evaluate the IDM technique performance. Analytical calculations and experimental results are shown validating the proposed approach.

Nowadays very powerful and cheap processors are available for industrial applications. Having this fact in mind, all the space-vector modulation strategies studied in this paper can be successfully implemented in current hardware systems obtaining great results. Taking into account this fact, the computational cost of the single-phase modulation technique (IDM) has very similar computational cost compared with the previous conventional two-dimensional SVM technique (2D-SVM). On the other hand, compared with the well-known three-dimensional SVM technique (3D-SVM) a slightly lower number of calculations have to be done thanks to avoiding the tetrahedron determination [26]. Finally, compared with the M-dimensional SVM technique (M-SVM) applied to multilevel multiphase converters, it can be noticed that the computational cost of the IDM technique becomes significantly lower when the number of phases increases because the M-SVM technique uses matrix calculations leading to a medium-high computational cost.

However, it has to be noticed that the simplicity is the main feature of the IDM. Simplicity in terms of conceptually simple concepts. This is the main advantage of the IDM compared with previous SVM techniques. Complex graphical representations and complex mathematical descriptions present on 2D-SVM, 3D-SVM and M-SVM techniques are reduced to very simple calculations and, most important, easy to understand using the IDM method. The IDM technique modulates the reference phase voltage as an average of the nearest voltage levels in a really simple way.

In addition, another conclusion of the comparison is that each previous SVM technique was designed to be applied to a particular multilevel converter (three-phase multilevel converters without neutral connection for 2D-SVM, three-phase multilevel converters with neutral connection for 3D-SVM and multiphase multilevel converters for the M-SVM technique). However, the IDM technique can be applied to any multilevel converter with any number of phases and levels. This fact represents an advantage compared with previous SVM methods.

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#### REFERENCES

[1] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[2] L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo and M. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Magazine*, vol. 2, no. 2, pp. 28–39, June 2008.

[3] Wenxi Yao, Haibing Hu and Zhengyu Lu, "Comparisons of Space-Vector Modulation and Carrier-Based Modulation of Multilevel Inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 45–51, Jan. 2008.

[4] D. G. Holmes and T. A. Lipo, "Pulse Width Modulation for Power Converters - Principles and Practice," IEEE Press, 2003.

[5] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Trans. Ind. Applicat.*, vol. 38, no. 2, pp. 500–506, March/April 2002.

[6] N. V. Nho and M. -J. Youn, "Comprehensive study on space-vector-PWM and carrier-based-PWM correlation in multilevel inverters," *IEE Proc. Electric Power Applicat.*, vol. 153, no. 1, pp. 149–158, Jan. 2006.

[7] D. Casadei, D. Dujic, E. Levi, G. Serra, A. Tani and L. Zari, "General Modulation Strategy for Seven-Phase Inverters With Independent Control of Multiple Voltage Space Vectors," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1921–1932, May 2008.

[8] D. Dujic, G. Grandi, M. Jones and E. Levi, "A Space Vector PWM Scheme for Multifrequency Output Voltage Generation With Multiphase Voltage-Source Inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1943–1955, May 2008.

[9] J. W. Kelly, E. G. Strangas and J. M. Miller, "Multiphase space vector pulse width modulation," *IEEE Trans. Energy Conversion*, vol. 18, no. 2, pp. 259–264, June 2003.

[10] Hyung-Min Ryu, Jang-Hwan Kim and Seung-Ki Sul, "Analysis of multiphase space vector pulse-width modulation based on multiple d-q spaces concept," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1364–1371, Nov. 2005.

[11] D. Casadei, F. Milanese, G. Serra, A. Tani and L. Zari, "Space vector modulation based on a multidimensional approach for multiphase inverters with an odd number of phases," in *IEEE Power Electronics Specialists Conference (PESC 2008)*, pp. 1351–1357, 15–19 June 2008.

[12] G. Grandi, G. Serra and A. Tani, "General Analysis of Multi-Phase Systems Based on Space Vector Approach," in *IEEE 12<sup>th</sup> International Power Electronics and Motion Control Conference (EPE-PEMC 2006)*, pp. 834–840, Aug. 2006.

[13] O. Lopez, J. Alvarez, J. Doval-Gandoy and F. D. Freijedo, "Multilevel Multiphase Space Vector PWM Algorithm," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, May 2008.

[14] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo and J. M. Carrasco, "Simple Unified Approach to Develop a Time Domain Modulation Strategy for Single-Phase Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3239–3248, Sept. 2008.

[15] A. Dell'Aquila, M. Liserre, V. G. Monopoli and P. Rotondo, "Overview of PI-Based Solutions for the Control of DC Buses of a Single-Phase H-Bridge Multilevel Active Rectifier," *IEEE Trans. Ind. Applicat.*, vol. 44, no. 3, pp. 857–866, May-June 2008.

[16] F. A. B. Batista and I. Barbi, "Space Vector Modulation Applied to Three-Phase Three-Switch Two-Level Unidirectional PWM Rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2245–2252, Nov. 2007.

[17] A. K. Gupta and A. M. Khambadkone, "A Space Vector Modulation Scheme to Reduce Common Mode Voltage for Cascaded Multilevel Inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672–1681, Sept. 2007.

[18] S. Busquets-Monge, S. Somavilla, J. Bordonau and D. Boroyevich, "Capacitor Voltage Balance for the Neutral-Point- Clamped Converter using the Virtual Space Vector Concept With Optimized Spectral Performance," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1128–1135, July 2007.

[19] K. E. Bornhardt, "Novel modulation techniques for DC-side commutated inverters," in *Fourth International Conference on Power Electronics and Variable-Speed Drives*, pp. 92–97, 17–19 July 1990.

[20] A. M. Massoud, S. J. Finney and B. W. Williams, "Systematic analytical-based generalised algorithm for multilevel space vector modulation with a fixed execution time," *IET Power Electron.*, vol. 1, no. 2, pp. 175–193, June 2008.

[21] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Applicat.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

[22] Ning-Yi Dai, Man-Chung Wong and Ying-Duo Han, "Application of a three-level NPC inverter as a three-phase four-wire power quality compensator by generalized 3DSVM," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 440–449, March 2006.

[23] C. Zhan, A. Arulampalam and N. Jenkins, "Four-wire dynamic voltage restorer based on a three-dimensional voltage space vector PWM algo-

rithm," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 1093–1102, July 2003.

- [24] R. Zhang, V. H. Prasad, D. Boroyevich and F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converters," *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 314–326, May 2002.
- [25] L. G. Franquelo, M. M. Prats, R. Portillo, J. I. Leon, M. A. Perales, J. M. Carrasco, E. Galvan and J. L. Mora, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 458–466, April 2006.
- [26] M. M. Prats, L. G. Franquelo, R. Portillo, J. I. Leon, E. Galvan and J. M. Carrasco, "A 3-D space vector modulation generalized algorithm for multilevel converters," *IEEE Power Electron. Letters*, vol. 1, no. 4, pp. 110–114, Dec. 2003.
- [27] R. S. Kanchan, K. Gopakumar and R. Kennel, "Synchronised carrier based SVPWM signal generation scheme for the entire modulation range extending up to six-step mode using the sampled amplitudes of reference phase voltages," *IET Electric Power Applicat.*, vol. 1, no. 3, pp. 407–415, May 2007.
- [28] O. Lopez, J. Alvarez, J. Doval-Gandoy, F. D. Freijedo, A. Nogueiras and C. M. Peñalver, "Multilevel Multiphase Space Vector PWM Algorithm Applied to Three-Phase Converters," in the 34<sup>th</sup> IEEE Annual Conference of the Industrial Electronics Society (IECON'08), pp. 3290–3295, 10–13 Nov. 2008, Orlando (USA).



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