

The Age of Multilevel Converters Arrives

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I. INTRODUCTION

Current energy arena is changing. The feeling of dependence on fossil fuels and the progressive increase of its cost is leading to the investment of huge amount of resources, economical and human, to develop new cheaper and cleaner energy resources not related to fossil fuels. In fact since decades, renewable energy resources have been the focus for researchers and different families of power converters have been designed to make the integration of this type of systems into the distribution grid a current reality. Besides, in the transmission lines, high power electronic systems are needed to assure the power distribution and the energy quality. Therefore, power electronic converters have the responsibility to carry out these tasks with high efficiency.

The increase of the world energy demand has entailed the apparition of new power converter topologies and new semiconductors technology capable to drive all needed power. A continuous race to develop higher voltage and current power semiconductors to drive high power systems still goes on. In this way, the last generation devices are suitable to support high voltages and currents (around 6.5 kV and 2.5 kA). However, currently there is a tough competition between the use of classic power converter topologies using high voltage semiconductors and new converter topologies using medium voltage devices. This idea is shown in Fig. 1, where multilevel converters built using mature medium power semiconductors are fighting in a development race with classic power converters using high power semiconductors which are under continuous development and are not mature. Nowadays, multilevel converters are a good solution for power applications due to the fact that they can achieve high power using mature medium power semiconductors technology [1][2].

Multilevel converters present great advantages compared with typical and very well known two-level converters [1],[3]. These advantages are fundamentally focused on improvements in the output signals quality and a nominal power increase in the converter. In order to show the improved quality of the output voltages of a multilevel converter, the output voltages of a single-phase two level converter is compared to a 3 and 9 level multilevel waveform in Fig. 2. The power converter output voltage improves its quality as the number of levels increases reducing the Total Harmonic Distortion of the system.

These properties make multilevel converters very attractive to the industry and nowadays, researchers all over the world are spending great efforts trying to improve multilevel converter performances such as the control simplification [4][5] and the performance of different optimization algorithms in order to enhance the Total Harmonic Distortion (THD) of the output signals [6][7], the balancing of the DC capacitors voltage [8][9], the ripple of the currents [10][11]. For instance, nowadays researchers are focused on the harmonic elimination using pre-calculated switching functions [12], harmonic mitigation to fulfill specific grid codes [13], the development of new multilevel converter topologies (hybrid or new ones) [14] and new control strategies

[15][16].

The most common multilevel converter topologies are: Neutral-Point-Clamped Converter (NPC) [17], Flying Capacitor Converter (FC) [18], and Cascaded H-Bridge Converter (CHB) [19]. These converters can be classified among the power converters for high power applications according to Fig. 3. Several surveys on multilevel converters have been published to introduce these topologies [1][2]. In 1980s, power electronics concerns were focused on the converters power increase (increasing voltage or current). In fact, current source inverters were the main focus for researchers in order to increase the current. However, other authors began to work on the idea of increasing the voltage instead the current. In order to achieve this objective, authors were developing new converter topologies and in 1981, A. Nabae, I. Takahashi and H. Akagi presented the first Neutral-Point-Clamped PWM converter (NPC) also named diode-clamped converter [17]. This converter was based on a modification of the classic two-level converter topology adding two new power semiconductors per phase (see Fig. 1). Using this new topology, each power device has to tolerate at the most half voltage compared with the two-level case with the same DC-Link voltage. So, if these power semiconductors have the same characteristics than the two-level case, the voltage can be doubled. The NPC converter was generalized in [21],[22] in order to increase the number of output levels, and was referred as multi-point clamped converter (MPC), although it has not reached the medium voltage market jet.

Years later, other multilevel converter topologies as the FC [18] or CHB [19],[20] appeared. These multilevel converters present different characteristics compared with NPC as the number of components, modularity, control complexity, efficiency and fault tolerance. Depending on the application, the multilevel converter topology can be chosen taking into account these factors as it is shown in Table I.

TABLE I
COMPARISON OF MULTILEVEL CONVERTER TOPOLOGIES DEPENDING ON IMPLEMENTATION FACTORS

	NPC	FC	CHB
Number of components	↑switches ↑diodes	↑switches ↑capacitors ↓diodes	↓switches ↓diodes isolated DC sources
Modularity	Low	High	High
Control complexity	Medium	High	High
Control concerns	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy

Nowadays, there are several commercial multilevel converter topologies which are sold as industrial products for high power applications [23]-[25]. However, although the advantages of using multilevel converters have been demonstrated, there has not been an industrial boom in the application of these power systems in the electrical grid in spite of their demonstrated good features to be used as medium voltage drives. Maybe, technological problems as reliability, efficiency, the increase of the control complexity and the design of simple and fast modulation methods have been the barrier that has slowed down the application of multilevel converters all over the world. Finally, the effort of researchers has overcome this technical barrier and it can be affirmed that multilevel converters are prepared to be applied as a mature power system in the electric energy arena.

This work is devoted to review and analyze the most relevant characteristics of multilevel converters, to motivate possible solutions, and to show that we are in a decisive instant in which energy companies have to bet for these converters as a good solution compared with classic two-level converters. The paper is organized as follows. In section II, a brief overview of the actual applications of multilevel converters is presented. An introduction of the modeling techniques and the most common modulation strategies is respectively presented in sections III and IV. Finally, the operational and technological issues have been addressed in section V and some conclusions are presented in last section.

II. MULTILEVEL CONVERTER DRIVEN APPLICATIONS

Multilevel converters are considered today as a very attractive solution for medium voltage high power applications. In fact, several major manufacturers commercialize NPC, FC or CHB topologies with a wide variety of control methods, each one strongly depending on the application. Particularly the NPC has found an important market in more conventional high power ac motor drives applications like conveyors, pumps, fans and mills among others, which offer solutions for industries including oil and gas, metals, power, mining, water, marine and chemistry [26][27].

The back to back configuration for regenerative applications has been also a major hit of this topology, used for example in regenerative conveyors for the mining industry [28], or grid interfacing of renewable energy sources, like wind power [29][30]. On the other hand FC converters have found particular applications for high bandwidth – high switching frequency applications such as medium voltage traction drives [31]. Finally the cascaded H-bridge has been successfully commercialized for very high power and power quality demanding applications up to a range of 31MVA, due to its series expansion capability. This topology has also been reported for active filter and reactive power compensation applications [32], electric and hybrid vehicles [33][34], photovoltaic power conversion [35]-[37], uninterruptible power supplies [38], and Magnetic Resonance Imaging [39]. As an example of a commercial multilevel power converter a 34kV-15MW three-phase six-cell CHB converter from SIEMENS for regenerative drives is shown in Fig. 4. A summary of multilevel converter driven applications is illustrated in Fig. 5.

III. MODELS: A TOOL TO ENHANCE MULTILEVEL CONVERTER POSSIBILITIES

The simulation and the determination of “Input to Output (I/O)” relations are a fundamental task in the study and design process of the multilevel converters. These I/O relations become essential for the development of suitable models which allow to obtain all the necessary information about the converter previously to the implementation stage. The modeling of multilevel converters is not a trivial task since they are made up of linear and non linear components. Historically, modeling techniques applied to DC power electronics converters have been adapted to be used in the study of AC ones, giving place to different approximations that achieve, according to their objectives, snubber circuits design, control schemes and controllers development, steady state study, dynamic and transient response study, stability analysis, etc. The operation of the multilevel converter is a periodic sequencing of its possible states corresponding to discrete states of the switches. Fig. 6 shows a three-level NPC phase has and the two possible modeling techniques. Taken these remarks into account, two types of models can be developed: equivalent circuit simulation or state-space averaged.

A. Circuit Simulation Modeling of Multilevel Converters

A model of the converter can be obtained with the help of powerful simulation tools as SPICE-based simulators. In this case, the modeling of the multilevel converters is reduced to the generation of an adequate electric circuit model that fully includes the non-linearities of the switches allowing the complete characterization of the system dynamic. Considering ideal switches, a linear description of the converter can be obtained for every switching state of the power converter. Fig. 6 shows a phase of the three-level diode-clamped converter where the switches have been replaced by an ideal switch and can be easily seen that the phase acts like a voltage source for every switch position so a linear equivalent circuit description of the converter phase can be obtained for each one. With this model, a linear piecewise simulation can be carried out. If the integration method for the model equations is properly chosen [40], the simulation time and results accuracy are good enough. However, this modeling approach often leads to large simulation times and possible unreliable results due to convergence problems. The main drawbacks of this modeling technique are that the integration of advanced control techniques with the model is almost impossible [40] and that the

model is usually complex being its use for control design often troublesome [41][42]. These models can be used in the tuning process of the control loops and to evaluate the high order harmonics due to switching that can be easily seen on currents shown in Fig. 6.

B. State-Space Averaged Modeling of Multilevel Converters

State-space averaged models can be easily obtained from the discrete ones when varying quantities are assumed as their averaged value over a switching period, remaining the DC value of those quantities. Since in AC converters these quantities are time varying even in the steady state, it is necessary to make a change of coordinates to convert AC sinusoidal quantities to DC quantities previously to the averaging process [43][44]. Time invariant systems controller design techniques can be used with these models when important components other than the fundamental harmonic are not present in the system. With the transformation to this “Rotating Reference Frame” DC quantities corresponds to the fundamental harmonic of the signals, but some multilevel converter topologies are not completely characterized by only the first harmonic and it is necessary to draw on to “Harmonic models” where a greater number of harmonics are taken into account obtaining an adequate modeling of the converter [41]. These “Harmonic models” are complex and only some advanced complex control techniques are suitable to be applied to them [42].

Recently a new state-space averaging modeling technique has been introduced based on approximations over the exact averaged linear piecewise characteristics of the converter [30]. In the phase of the three-level diode-clamped converter shown in Fig. 6, the ideal switch will be switching between the three possible states so an average model can be deduced considering δ_a as the averaged value of the switch position. Fig. 6 shows the graphic representation of the exact averaged linear piecewise approximation and the proposed quadratic approximation [29]. This technique provides simple enough models to be used in the controller design [45] and carries out fast simulations without convergence problems due to the continuous nature of the obtained equations. Therefore, the use of these models overcomes one of the technological handicaps in which the multilevel converters are involved, making the design stage of multilevel power systems a more accessible task. Fig. 6 shows the currents obtained with this kind of model and when compared with those obtained with the equivalent circuit simulation it can be seen that the results are almost the same except for the high order harmonics.

IV. MULTILEVEL MODULATION METHODS

Multilevel inverter modulation and control methods have attracted much research and development attention over the last decade [1][2][46][47]. Among the reasons are: the challenge to extend traditional modulation methods to the multilevel case, the inherent additional complexity of having more power electronics devices to control, and the possibility to take advantage of the extra degrees of freedom provided by the additional switching states generated by these topologies. As consequence, a large number of different modulation algorithms have been developed, each one with unique features and drawbacks, depending on the application.

A classification of the modulation methods for multilevel inverters is presented in Fig. 7. The modulation algorithms are divided into two main groups depending on the domain in which they operate: the state space vector domain in which the operating principle is based on the voltage vector generation, and the time domain in which the method is based on the voltage level generation over a time frame. In addition, in Fig. 7 the different methods are labeled depending on the switching frequency they produce. In general, low switching frequency methods are preferred for high power applications due to the reduction of switching losses, while the better output power quality and higher bandwidth of high switching frequency algorithms are more

suitable for high dynamic range applications.

A. Multilevel Converters PWM strategies

Traditional Pulse Width Modulation (PWM) techniques [48] have been successfully extended for multilevel converter topologies, by using multiple carriers to control each power switch of the converter. Therefore, they are known as Multicarrier PWM methods as shown in Fig. 7. For multicell topologies, like FC and CHB, each carrier can be associated to a particular power cell to be modulated independently using sinusoidal bipolar PWM and unipolar PWM respectively, providing an even power distribution among the cells. For a converter with m cells, a carrier phase shift of $180^\circ/m$ for the CHB and of $360^\circ/m$ for the FC is introduced across the cells to generate the stepped multilevel output waveform with low distortion [23]. Therefore this method is known as Phase Shifted PWM (PS-PWM). The difference between the phase shifts and the type of PWM (unipolar or bipolar) is because one CHB cell generates 3-level outputs, while one FC cell generates two level outputs. This method naturally balances the capacitor voltages for the FC, and also mitigates input current harmonics for the CHB.

The carriers can also be arranged with shifts in amplitude relating each carrier with each possible output voltage level generated by the inverter. This strategy is known as Level Sifted PWM (LS-PWM), and depending on the disposition of the carriers, they can be in Phase Disposition (PD-PWM), Phase Opposition Disposition (POD-PWM) and Alternate Phase Opposition Disposition (APOD-PWM) [49], all shown in Fig. 7.

A in depth assessment between these PWM methods can be found in [50]. LS-PWM methods can be implemented for any multilevel topology, however, they are more suited for the NPC, since each carrier signal can be easily related to each power semiconductor. Particularly LS-PWM methods are not very attractive for CHB inverters, since the vertical shifts relate each carrier and output level to a particular cell, producing an uneven power distribution among the cells. This power unbalance disables the input current harmonic mitigation that can be achieved with the multipulse input isolation transformer, reducing the power quality.

Finally, the hybrid modulation is in part a PWM based method which is specially conceived for the CHB with unequal dc sources [14],[51]-[53]. The basic idea is to take advantage of the different power rates among the cells of the converters to reduce switching losses and improve the converter efficiency. This is achieved by controlling the high power cells at fundamental switching frequency by turning on and off each switch of each cell only one time per cycle, while the low power cell is controlled using unipolar PWM. Also asymmetric or hybrid topologies have been proposed based on the MPC structure [54].

B. Space Vector Modulation techniques

Space Vector Modulation (SVM) is a technique where the reference voltage is represented as a reference vector to be generated by the power converter. All the discrete possible switching states of the converter lead to discrete output voltages and they can be also represented as the possible voltage vectors (usually named state vectors) that can be achieved. SVM technique generates the voltage reference vector as a linear combination of the state vectors obtaining an averaged output voltage equal to the reference over one switching period [55].

In the last years, several space vector algorithms extended to multilevel converters have been found in bibliography. Most of them are particularly designed for a specific number of levels of the converter and the computational cost and the algorithm complexity are increased with the number of levels. Besides, these general modulation techniques for multilevel converters involve trigonometric function calculations, look-up tables or coordinated system transformations which increases the computational load.

Recent SVM strategies have drastically reduced the computational effort and the complexity of the algorithms compared with

other conventional SVM and sinusoidal PWM modulation techniques [56]-[62]. A survey of recent SVM algorithms for power voltage source multilevel converters was presented in [63]. These techniques provide the nearest state vectors to the reference vector forming the switching sequence and calculating the corresponding duty cycles using extremely simple calculations without involving trigonometric functions, look-up tables or coordinate system transformations which increase the computational effort corresponding to the modulation of a multilevel converter. Therefore, these methods drastically reduce the computational load maintained permitting the on-line computation of the switching sequence and the on-state durations of the respective switching state vectors. In addition, the low computational cost of the proposed methods is always the same and it is independent of the number of levels of the converter.

The three dimensional SVM (3D-SVM) technique presented in [59] is a generalization of the well known 2D-SVM strategy [60] used when the power system is balanced (without triple harmonics) and therefore the state vectors are located in a plane (alpha-beta plane). However, it is necessary to generalize to a 3D space if the system is unbalanced or if there is zero sequence or triple harmonics because in this case state vectors are not on a plane. 3D-SVM technique for multilevel converters is successfully used for compensating zero sequence in active power filters with neutral with single-phase distorting loads which generate large neutral currents. In general, 3D-SVM is useful in systems with or without neutral, unbalanced load, triple harmonics and for generating whatever three-dimensional control vector. Moreover, this technique also permits to balance the DC-link capacitors voltage.

The strategy proposed in [59] is the first 3D-SVM technique for multilevel converters which permits the on-line calculation of the sequence of the nearest space vector for generating the reference voltage vector. The computational cost of the proposed method is very low and it is independent of the number of levels of the converter. This technique can be used as modulation algorithm in all applications which provide a 3D vector control.

Finally, four-leg multilevel converters are finding relevance in active power filters and fault-tolerant three-phase rectifiers with capability for load balancing and distortion mitigation thanks to their ability to meet the increasing demand of power ratings and power quality associated with reduced harmonic distortion and lower EMI [64][65]. A four-leg multilevel converter permits a precise control of neutral current due to an extended range for the zero sequence voltages and currents.

A generalized and optimized 3D-SVM algorithm for four-leg multilevel converters has been recently presented in [66]. The proposed technique directly allows the optimization of the switching sequence minimizing the number of switching in four-leg systems. As in [56]-[61], the computational complexity has been reduced up to minimum. This technique can be used as modulation algorithm in all applications needing a 3D control vector such as four-leg active, where the conventional 2D-SVM can not be used.

C. Other Multilevel Modulation Algorithms

Although SVM and Multicarrier PWM are widely accepted and have reached a certain maturity for multilevel applications, other algorithms have been developed to satisfy particular needs of different applications. Selective Harmonic Elimination (SHE), for example, has been extended to the multilevel case for high power applications due to the strong reduction in the switching losses [6][12][67]. However, SHE algorithms are very limited to open-loop or low-bandwidth applications, since the switching angles are computed offline and stored in tables, which are then interpolated according to the operating conditions. In addition, SHE based methods become very complex to design and implement for converters with high number of levels (above five), due to the increase of switching angles, hence equations, that need to be solved. In this case, other low switching frequency methods are more suitable. For example, multilevel Space Vector Control (SVC) takes advantage of the high number voltage vectors generated by a converter with high number of levels, by approximating the reference to the closest generable vector [68]. This

principle results in a natural fundamental switching frequency with reduced switching losses, like in SHE, that can be easily implemented in closed-loop and high-bandwidth systems. The time domain version of SVC, is the Nearest Level Control (NLC), which in essence is the same principle but considering the closest voltage level that can be generated by the inverter instead of the closest vector [69]. Both methods, are suitable for inverters with high number of levels, since the operating principle is based on an approximation and not a modulation with a time average of the reference, and also due to the low and variable switching frequency, they present higher total harmonic distortion for inverter with lower number of levels and also for low modulation indexes.

As mentioned before not all the modulation schemes mentioned before and illustrated in Fig. 7 are suitable for each topology, moreover some algorithms are not applicable to some converters. Fig. 8 summarizes the compatibility between the modulation methods and the multilevel topologies.

V. OPERATIONAL AND TECHNOLOGICAL ISSUES

Multilevel converters offer very attractive characteristics for high power applications, however the power circuit of the multilevel topologies have more complex structures than classic converters and sometimes their operation is not straightforward, and particular problems need to be addressed. In other occasions this extra complexity can also be embraced as an opportunity to introduce enhanced operating characteristics like efficiency, power quality and fault tolerant operation, which are not feasible in classic topologies.

One of the most analyzed and extensively addressed drawbacks of multilevel technology is the neutral point control or capacitor voltage balance necessary for NPC converters. The NPC experiments a capacitor unbalance for certain operating conditions, depending on the modulation index, dynamic behavior and load conditions among others, which produce a voltage difference between both capacitors, shifting the neutral point and causing undesirable distortion at the converter output. This drawback has been addressed in many works for different modulation methods, both in vector and time domain [70]-[74], and is widely accepted as a solved problem. The neutral point control of NPC converters and the power circuit structure becomes even more complex for non traditional configurations with more output levels (five and up), especially due to the amount of clamping diodes needed. Therefore mainly three-level NPC converters are found on the market.

FC converters, on the contrary have a natural voltage balancing operation [31] but the capacitor voltages have to be pre-charged at startup close to their nominal values, also know as initialization. This can be performed via an additional and simple control logic of the switches of the converter by connecting successively each capacitors to the source and disconnect them when the desired voltage is reached. Although the topology is modular in structure and can be increased in an arbitrary number of cells, the additional flying capacitors and the involved costs has kept traditional configurations up to about four levels. In addition, more cells do not necessarily signify an increase of the power rating of the converter, since the output voltage amplitude does not vary, only the number of levels, hence the power quality.

CHB converters, have also no voltage balancing problems due to the independent and isolated dc-sources provided by the multipulse secondary windings of the input transformer. Furthermore, it does not need special initialization, and its circuit structure enables series connection to reach power levels for very high power applications (maximum rates 13.8KV, 1400A and 31000KVA), where it has found industrial acceptance. However, the isolation transformer is non standard due to the amount of secondaries, and to the angle shifts between windings for input current harmonic mitigation. This is an important drawback that has kept this topology with a smaller market penetration. Nevertheless, transformer-less applications, like photovoltaic power conversion, active filters and battery powered electric vehicles, have been reported as suitable applications [32]-[39]. The

complicated transformer has also been avoided using a standard transformer to power only one cell (per phase) of the converter, and use the control strategy to control the circulating power to keep the other power cells dc-links charged at desired values [76].

For the case of CHB with unequal dc-sources, the same drawback of the equally fed case apply, with the difference that the input transformer has even power rate differences between windings, and in addition no input current harmonic compensation is achieved. Another drawback is the loss of modularity since the asymmetric power distribution between cells forces different ratings of the components (mainly the voltage rate of the capacitors and semiconductors). Nevertheless, these topologies offer very high power quality waveforms with less power semiconductors (reduction in size and cost, while increase in reliability), and lower switching losses, since the high power cells only commute at fundamental switching frequency. Moreover, the complicated transformer can be avoided by similar control strategies applied to the symmetric case, or in transformer-less applications (specially active filters). Another issue with the asymmetric CHB is that the low power cells regenerate power during some operating conditions (they vary depending on the asymmetry, the modulation index, and the load), even if the power converter is in motoring mode [77]. If this power is not handled appropriately by using an active front end rectifier or by resistive dissipation, the lower power cells dc-link voltages will drift and become unbalanced generating output voltage distortion. This problem can be minimized using appropriate voltage asymmetries between the cells [14].

Although common mode voltages and bearing currents are strongly reduced when using multilevel converters, due to the reduced dv/dt 's and more sinusoidal outputs, this is still a subject under research, and several contributions have been reported [78]-[81].

Since CHB and FC have a modular structure, they can be more directly adapted to operate under internal fault conditions. This is a very attractive capability for industry applications, specially considering those downtimes (and the associated costs) can be avoided, or greatly reduced while a more organized and scheduled reparation is prepared. Fault operation is only possible if the malfunction is properly and timely detected, making the fault diagnostic an important issue. Several contributions have been reported, from simply bypassing faulty cells to more complex reference pre-compensation methods for enhanced operation [82]-[85]. Different fault detection mechanisms have also been reported, for example, based on the spectral analysis of the carrier and sidebands harmonics of the output voltage [86],[87].

Although the three main topologies analyzed in the paper present unique features and drawbacks, making each one special for a particular application, they have been compared in terms of structure, cost, and efficiency in [88].

VI. CONCLUSIONS

Multilevel converters have matured from being an emerging technology to a well established and attractive solution for medium voltage high power drives. As it was presented along this paper, these converters have overcome the technical barriers which had been the curb for their deep use as an optimized solution in the power market. Modeling, control strategies design and modulation methods development have been introduced in last years to carry out this technical revolution. Nowadays multilevel converter topologies as NPC, FC and CHB own very interesting features in terms of power quality, power range, modularity and other characteristics achieving high quality output signals being specially designed for medium and high power applications. Therefore, it's the time for betting on this technology for actual and future power applications just now when the market is step to step going forward more powerful and distributed energy sources. The current trends and challenges faced by energy applications, such as renewable power conversion and distributed generation systems, together with the recent developments in multilevel converter technology are opening a new vast area of applications where this technology has a lot to offer. It is just a

question of time before multilevel converters will reach an important market share in these applications. You could say its time for multilevel converters...

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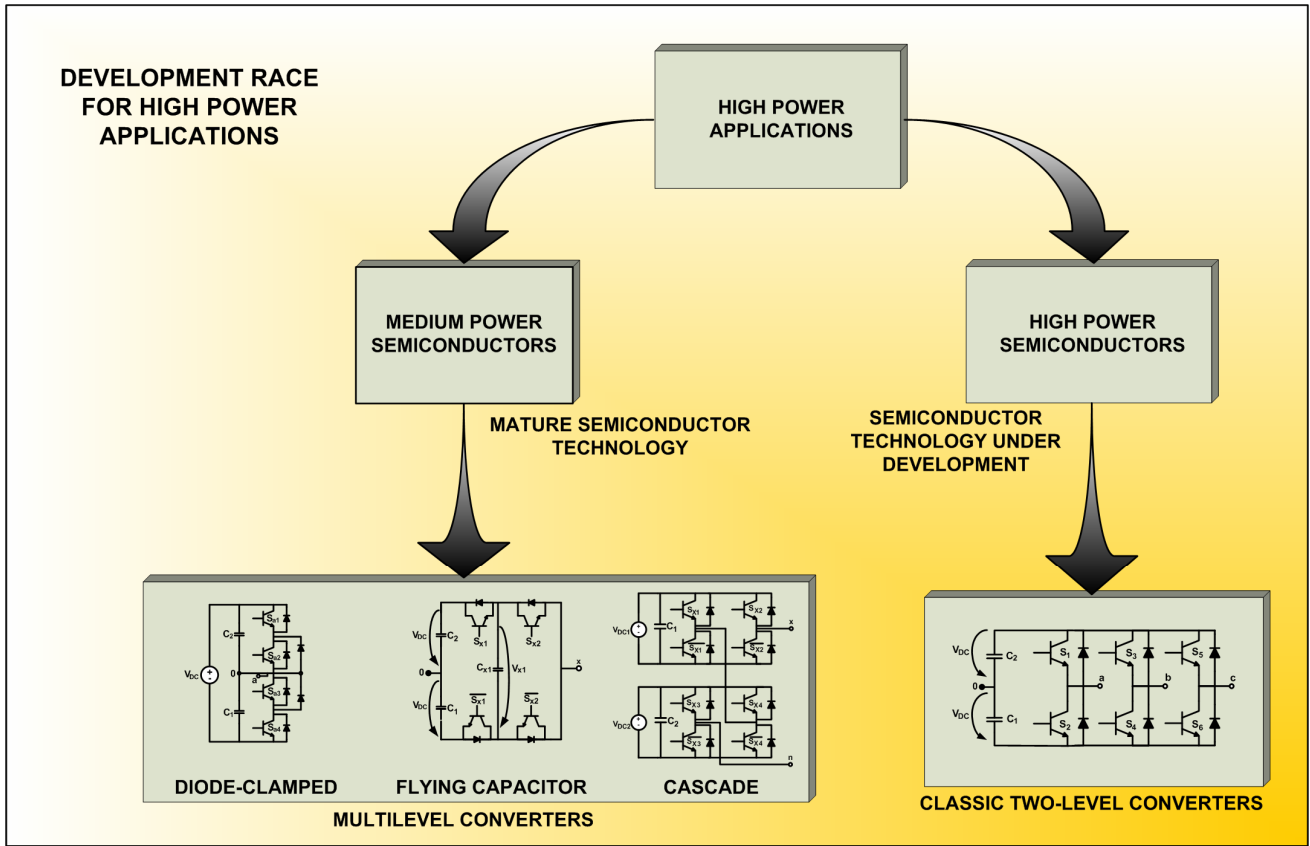


Fig. 1. Classic two-level power converters versus most common multilevel power converters. Development race between two different solutions in high power applications.

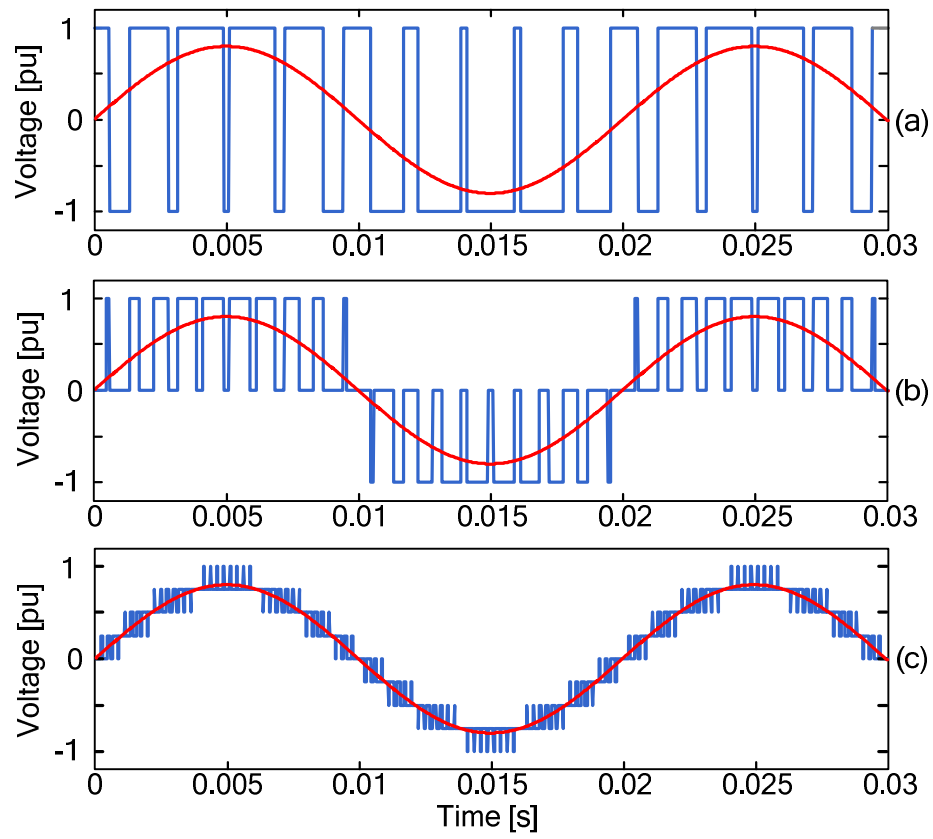


Fig. 2. Comparison of output phase voltage waveforms: a) two level inverter. b) three level inverter. c) nine level inverter.

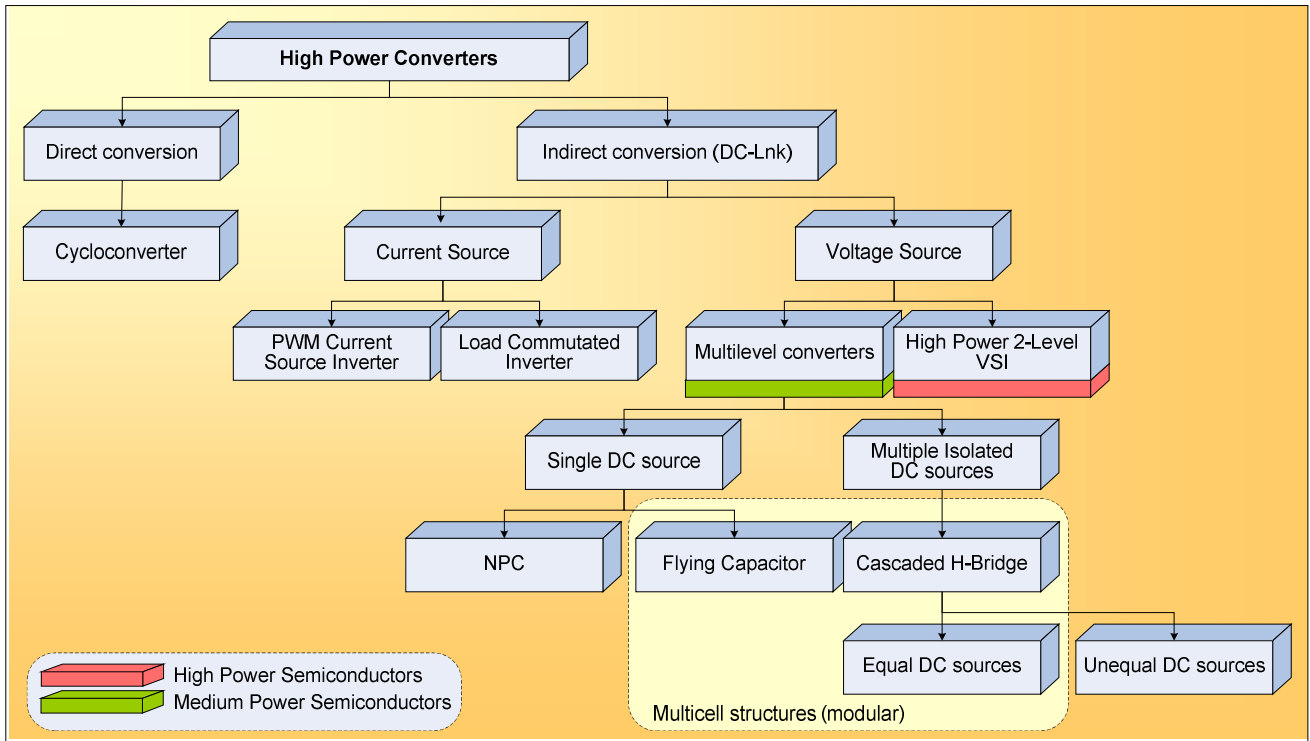


Fig. 3. High power converters classification.



Fig. 4. Multilevel cascaded H-bridge converter with six cells per phase, 13 levels, 15MW for regenerative drives

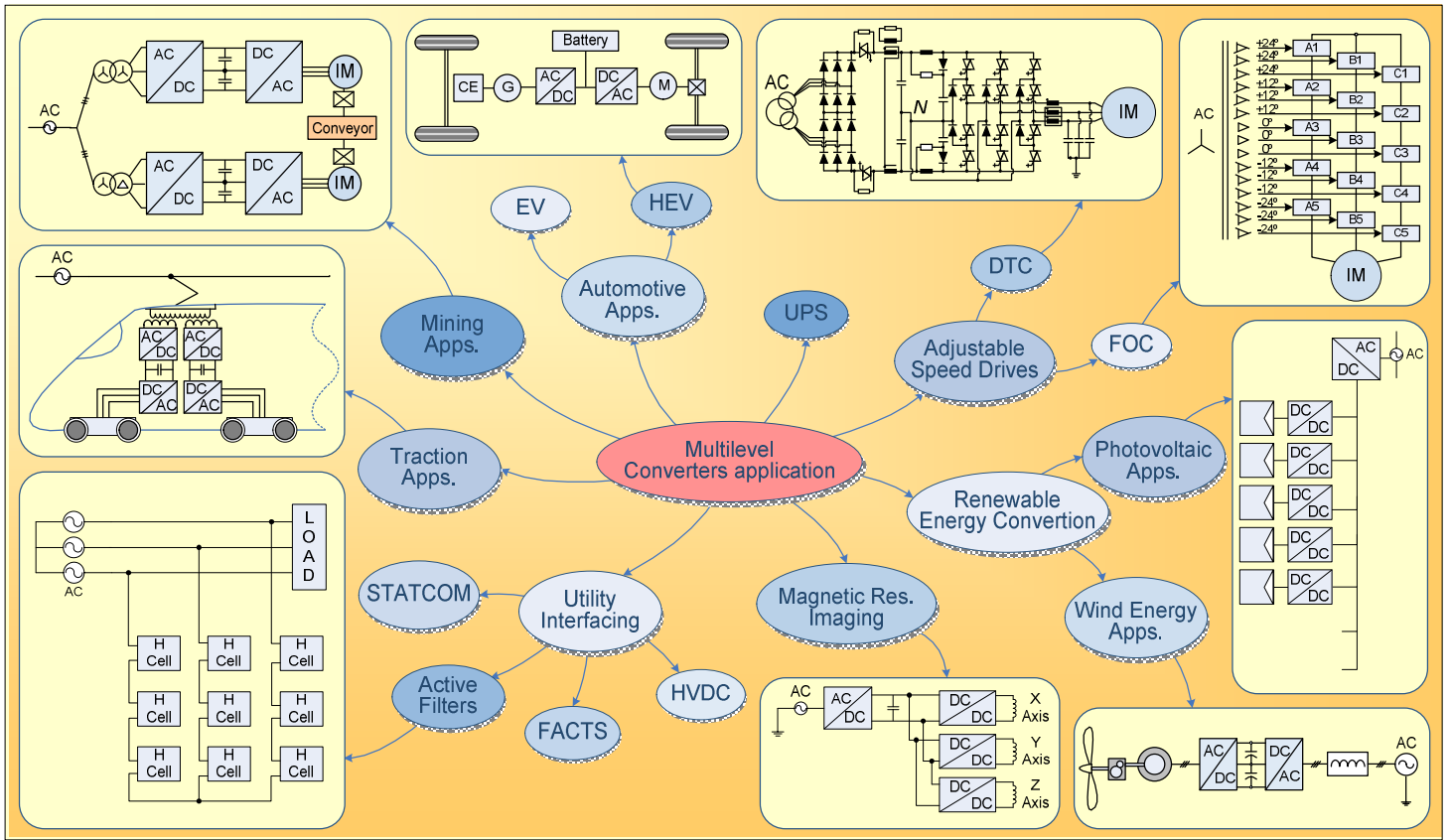


Fig. 5. Multilevel converter driven applications overview.

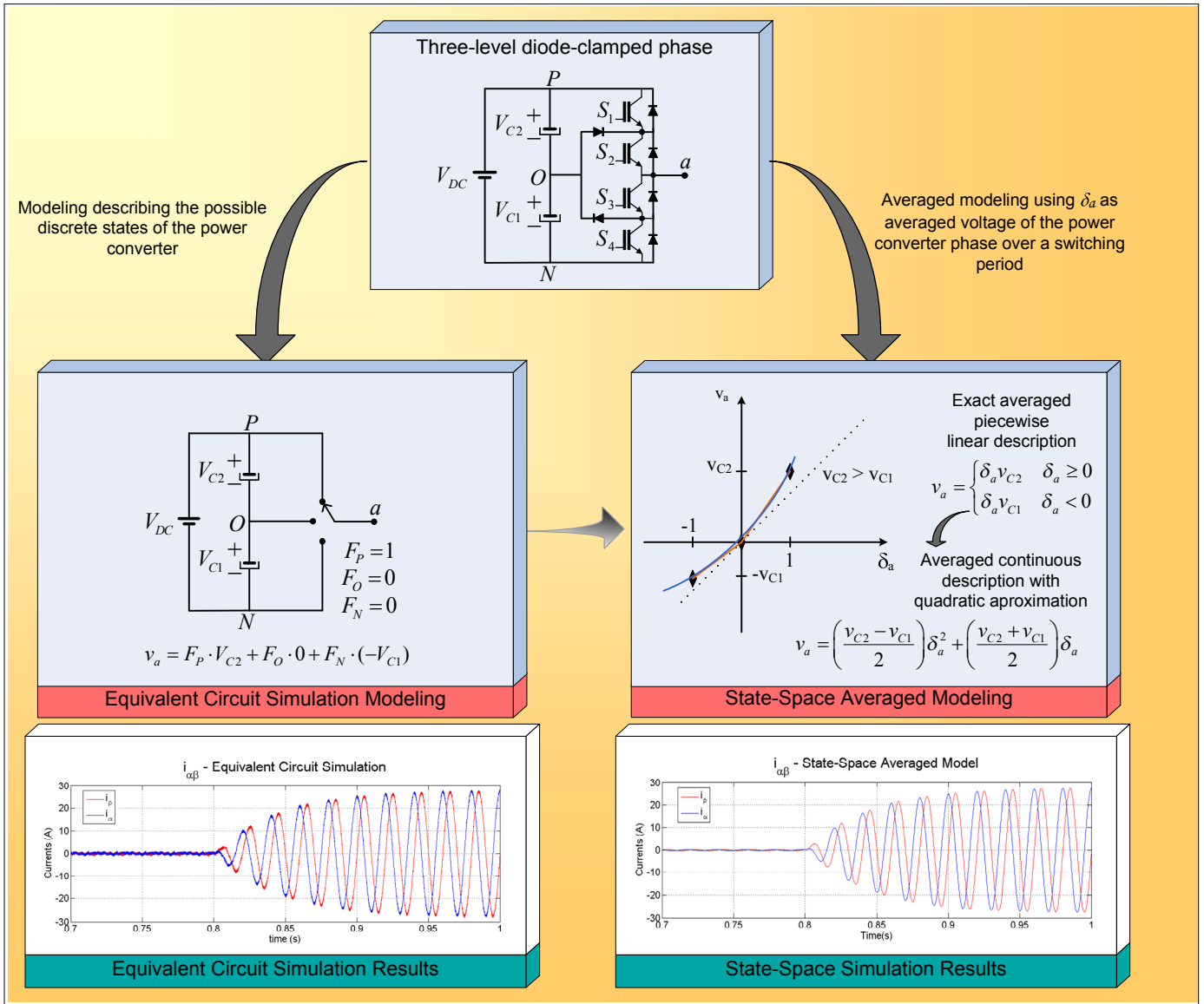


Fig. 6. Equivalent circuit and State-Space Modeling of multilevel converters

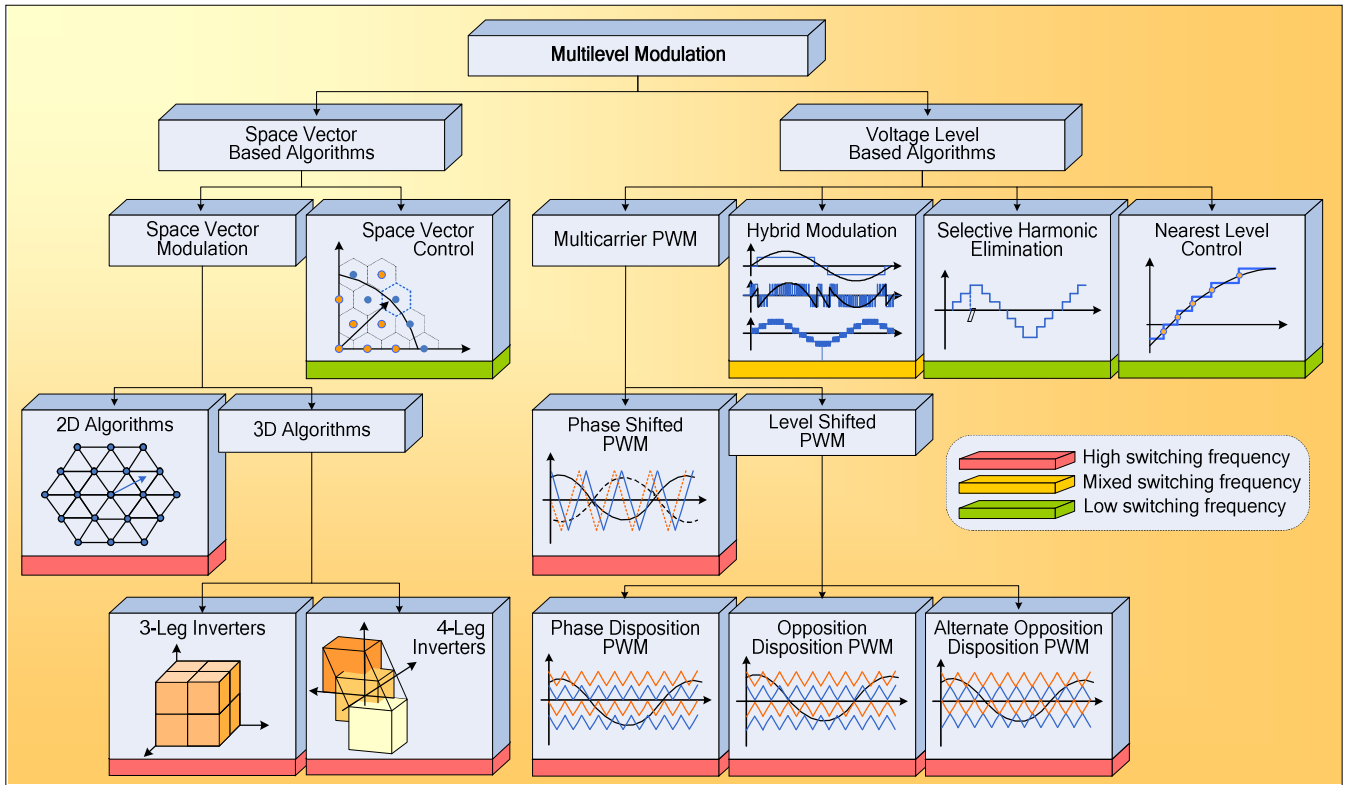


Fig. 7. Multilevel inverter modulation classification.

		Topologies		
		NPC	FC	CHB
Modulation Methods	SVM	✓	✓	✓
	LS-PWM	✓	✓	—
	PS-PWM	✗	✓	✓
	Hybrid modulation	✗	✗	✓
	SHE	✓	✓	✓
	SVC	—	✓	✓
	NLC	—	✓	✓

✓ Applicable/Recommended ✗ Not Applicable — Applicable/Not Recommended

Fig. 8. Applicability of modulation methods to multilevel topologies.