

Article

# PVT-Robust CMOS Programmable Chaotic Oscillator: Synchronization of Two 7-Scroll Attractors

Victor Hugo Carbajal-Gomez <sup>1,2,†</sup>, Esteban Tlelo-Cuautle <sup>3,†,\*</sup>, Carlos Sanchez-Lopez <sup>1,†</sup> and Francisco Vidal Fernandez-Fernandez <sup>4,†</sup>

<sup>1</sup> Department of Electronics, Universidad Autónoma de Tlaxcala, Apizaco Tlaxcala 90300, Mexico; vict hug26@gmail.com (V.H.C.-G.); carlsanmx@yahoo.com.mx (C.S.-L.)

<sup>2</sup> Faculty of Electronic Sciences, Benemérita Universidad Autónoma de Puebla, Puebla 72570, Mexico

<sup>3</sup> Department of Electronics, INAOE, Puebla 72840, Mexico

<sup>4</sup> Instituto de Microelectrónica de Sevilla, CSIC and Universidad de Sevilla, 41092 Sevilla, Spain; pacov@imse-cnm.csic.es

\* Correspondence: etlelo@inaoe.mx; Tel.: +52-222-2663100

† These authors contributed equally to this work.

Received: 28 September 2018; Accepted: 12 October 2018; Published: 16 October 2018



**Abstract:** Designing chaotic oscillators using complementary metal-oxide-semiconductor (CMOS) integrated circuit technology for generating multi-scroll attractors has been a challenge. That way, we introduce a current-mode piecewise-linear (PWL) function based on CMOS cells that allow programmable generation of 2–7-scroll chaotic attractors. The mathematical model of the chaotic oscillator designed herein has four coefficients and a PWL function, which can be varied to provide a high value of the maximum Lyapunov exponent. The coefficients are implemented electronically by designing operational transconductance amplifiers that allow programmability of their transconductances. Design simulations of the chaotic oscillator are provided for the 0.35  $\mu\text{m}$  CMOS technology. Post-layout and process–voltage–temperature (PVT) variation simulations demonstrate robustness of the multi-scroll chaotic attractors. Finally, we highlight the synchronization of two seven-scroll attractors in a master–slave topology by generalized Hamiltonian forms and observer approach. Simulation results show that the synchronized CMOS chaotic oscillators are robust to PVT variations and are suitable for chaotic secure communication applications.

**Keywords:** chaos; current-mirror; current-mode; MOS transistor; PWL function; operational transconductance amplifier; programmability; master–slave synchronization; PVT variations

## 1. Introduction

Chaotic systems have been studied for a long time and nowadays many examples of electronic implementations using discrete devices can be found in the literature. However, the big challenge remains the generation of multi-scroll attractors and their design using CMOS integrated circuit (IC) technology to develop real life applications. For instance, the control and synchronization of chaotic systems were first proposed no more than three decades ago [1–7], from which some practical developments have impacted areas such as high-performance circuit design (e.g., delta-sigma modulators and power converters), liquid mixing, chemical reactions, biological systems (e.g., sensing signals produced in the human brain, heart or other organs), power electronics, secure communication systems, etc. [8–13]. That way, this new and challenging line for research and development is becoming highly inter-disciplinary, involving systems and control engineers, theoretical and experimental physicist, applied mathematicians, physiologists and, above all, IC design specialists.

Relevant electronic implementations of chaotic oscillators are summarized in [14], where one can see the usefulness of piecewise-linear (PWL) functions to generate attractors as for the well-known double-scroll Chua's circuit [15–18]. If the PWL function modeling the Chua's diode is augmented to have more break-points, by combining slopes, one can generate multi-scroll chaotic attractors [19,20]. In addition, adding more PWL functions allows generating multi-scroll attractors not only in one direction (1D) [21,22], but also in two (2D) [23], three (3D) [24], and four directions (4D) [25].

From the electronic design point of view, the majority of chaotic oscillators are based on the traditional voltage operational amplifier [26]. However, there are many drawbacks related to this approach, such as requiring a high number of amplifiers and passive elements for its design, they have low frequency response, and require high voltage biases up to  $\pm 18$  V. On the other hand, as already shown in [15,16], the good option to design CMOS chaotic oscillators is by using operational transconductance amplifiers (OTAs), which are biased using low voltages of around  $\pm 1.65$  V or lower, and they provide higher frequency response than voltage amplifiers. However, the challenge in IC design is the generation of multi-scroll attractors, for which up to now the highest number of scrolls that have been generated is five [27,28]. In this manner, we introduce a CMOS design of a seven-scroll attractor that is based on a new current-mode PWL function that can be programmed to generate 2–7-scroll attractors. We performed post-layout simulations using 0.35  $\mu\text{m}$  CMOS technology from AMS to guarantee robustness to process–voltage–temperature (PVT) variations. We also show the synchronization of two seven-scroll attractors to highlight that the proposed CMOS design can be suitable to develop applications in security and Internet of Things (IoT).

The rest of this article shows the CMOS design of a chaotic oscillator using OTAs and a new programmable current-mode PWL function to generate up to seven scrolls. The chaotic oscillator has four coefficients that have been optimized in [29–32] to provide a high maximum Lyapunov exponent (MLE). Section 2 lists feasible solutions providing different values of MLE. It is worth mentioning that the seminal work in [33] introduced the first algorithm to compute Lyapunov exponents from experimental chaotic time series. Afterwards, other authors introduced different approaches to compute MLE [34–38]. Section 3 details the design of the OTA that allows programmability of the transconductance, and introduces our proposed current-mode PWL function. The whole CMOS chaotic oscillator is introduced in Section 4, where we detail the programmability of the current-mode PWL function. Section 5 shows the master–slave synchronization of two CMOS chaotic oscillators. The layout of the chaotic oscillator has been performed using 0.35  $\mu\text{m}$  CMOS technology, as shown in Section 6, where we highlight post-layout simulations including PVT variations for the synchronization of two seven-scroll chaotic attractors using generalized Hamiltonian forms and observer approach. Finally, the conclusions are listed in Section 7.

## 2. OTA-Based Chaotic Oscillator Using a CMOS Programmable Current-Mode PWL Function

Chaotic oscillators have a complex dynamical behavior that is associated to their high sensitivity to small variations in the initial conditions. They also have bounded trajectories in the phase space. They possess at least one MLE and have a continuous power spectrum [39–46]. Chaotic oscillators can be described by the state-space approach given by

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{f}(\mathbf{x}, \mathbf{u}, t) \\ \mathbf{y} &= \mathbf{h}(\mathbf{x}, \mathbf{u}, t)\end{aligned}\quad (1)$$

where the dot denotes differentiation with respect to time and the functions  $\mathbf{f}(\cdot)$  and  $\mathbf{h}(\cdot)$  are in general nonlinear. In Equation (1), the variety of possible nonlinear functions is infinite, but, in some cases, they can be approached by PWL functions leading to the state-space representation given by

$$\begin{aligned}\dot{\mathbf{x}} &= \mathbf{Ax} + \mathbf{Bu} \\ \mathbf{y} &= \mathbf{Cx} + \mathbf{Du}\end{aligned}\quad (2)$$

where **A**, **B**, **C** and **D** are matrices (possibly time-dependent) of appropriate dimensions. If the input vector **u** is fixed or equals zero, the model describes an autonomous dynamical system.

Lets us consider the multi-scroll chaotic oscillator modeled by [26]:

$$\begin{aligned} \dot{x}_1 &= x_2 \\ \dot{x}_2 &= x_3 \\ \dot{x}_3 &= -ax_1 - bx_2 - cx_3 + d_1f(x_1) \end{aligned} \quad (3)$$

where  $a, b, c$ , and  $d_1$  are real and positive constants, and  $f(x_1)$  models a saturated nonlinear function (SNLF) series that can be approached by a PWL function, as already shown in [23,26,47,48]. In Equation (3), the coefficients  $a, b, c$ , and  $d_1$  must have appropriate values to estimate the quality of chaotic behavior [49,50]. For example, one can evaluate Lyapunov exponents, Kaplan–York dimension and entropy. In this work. we focus on evaluating Lyapunov exponents, which are asymptotic measures characterizing the average rate of growth (or shrinkage) of small perturbations to the solutions of a dynamical system [38], and provide quantitative measures of sensitivity of the system response to small changes in initial conditions [35].

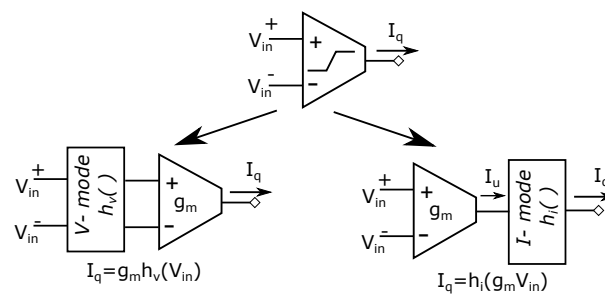
The Lyapunov exponents  $\lambda_i$  can be computed by applying numerical methods [35,36,41]. Furthermore, the optimization of Equation (3) requires varying the coefficients to obtain high values of MLE, as already demonstrated in [31]. For instance, in [51], three meta-heuristics (genetic algorithms (GA), differential evolution (DE), and particle swarm optimization (PSO)) have been applied to optimize MLE. When the coefficient values are fixed to 0.7, as already done in [26,52], the MLE value is 0.105422 to generate two-scroll, 0.138087 to generate three scrolls, 0.142087 to four scrolls, 0.134534 to five scrolls, 0.147785 to six scrolls, and 0.148159 to generate seven scrolls. However, after applying GA, DE and PSO, the optimized MLE values increase according to Table 1, where we list the mean value, standard deviation and coefficient values to generate two to seven scrolls.

The goal of this article is the introduction of a current-mode PWL function to design the chaotic oscillator in Equation (3), using CMOS technology to program the generation of 2–7-scroll attractors. That way, Table 1 is the reference to design the CMOS OTAs to accomplish the values of the coefficients  $a, b, c$ , and  $d_1$ . According to Trejo-Guerra *et al.* [14], there are very few integrated designs presented in the literature with this purpose, and they only generate up to five-scroll attractors. In this article, we highlight the design of a CMOS programmable current-mode PWL function to generate up to seven-scroll. The main idea is sketched in Figure 1, where the PWL function is generated from an input voltage ( $V_{in}^+ - V_{in}^-$ ) to provides an output current  $I_q$ . This PWL function can be generated in either voltage-mode  $h_v()$  or current-mode  $h_i()$ . This article details the CMOS design of the current-mode PWL function labeled as saturated nonlinear function (SNLF) in Figure 2, which shows the OTA-capacitor ( $g_m - C$ ) implementation of Equation (3), where the state variables are  $x_1, x_2$  and  $x_3$ . By applying Kirchhoff's current law to Figure 2, one gets Equation (4), where SNLF is described by  $f(x_1)$ , and the equations resemble the original ones defined by Equation (3). The operating frequency is evaluated by  $f = g_{m(x|y|z)}/2\pi C$ .

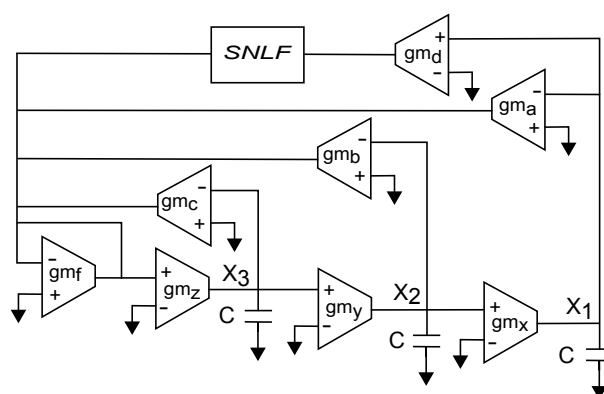
$$\begin{aligned} \dot{x}_1 &= \frac{g_{mx}x_2}{C} \\ \dot{x}_2 &= \frac{g_{my}x_3}{C} \\ \dot{x}_3 &= \frac{g_{mz}}{C} \left( -\frac{g_{ma}x_1}{g_{mf}} - \frac{g_{mb}x_2}{g_{mf}} - \frac{g_{mc}x_3}{g_{mf}} + \frac{g_{md_1}f(x_1)}{g_{mf}} \right) \end{aligned} \quad (4)$$

**Table 1.** Optimized MLE values to generate 2–7-scroll attractors applying GA, DE and PSO [51].

Scrolls	MLE	Mean	St.dev.	Optimized Values for $a, b, c, d_1$
2 GA	0.221986	0.216023	0.005391	[0.9816, 0.8410, 0.4988, 0.6540]
2 DE	0.222767	0.218224	0.001765	[1.0000, 0.8284, 0.5321, 1.0000]
2 PSO	0.223114	0.219041	0.002024	[0.9970, 0.8469, 0.5098, 0.9221]
3 GA	0.298260	0.283042	0.011624	[0.9895, 0.7774, 0.3560, 1.0000]
3 DE	0.297813	0.290483	0.002884	[1.0000, 0.7782, 0.3416, 1.0000]
3 PSO	0.301033	0.294377	0.003385	[1.0000, 0.7724, 0.3618, 0.9927]
4 GA	0.303209	0.289411	0.014313	[0.9367, 0.6894, 0.3204, 0.9896]
4 DE	0.310734	0.300321	0.006029	[0.9399, 0.7037, 0.2854, 0.9660]
4 PSO	0.315349	0.306306	0.004998	[0.9607, 0.7028, 0.2728, 0.9880]
5 GA	0.296158	0.281553	0.012683	[0.9810, 0.8134, 0.2931, 1.0000]
5 DE	0.321793	0.302033	0.009817	[0.9770, 0.6622, 0.2180, 1.0000]
5 PSO	0.322885	0.309523	0.007469	[0.9497, 0.6494, 0.2749, 0.9966]
6 GA	0.313739	0.298833	0.008199	[0.9520, 0.5422, 0.2819, 1.0000]
6 DE	0.323515	0.307036	0.006663	[0.9167, 0.5410, 0.2467, 0.9521]
6 PSO	0.324055	0.310436	0.009127	[0.9502, 0.5745, 0.2395, 0.9916]
7 GA	0.322424	0.304251	0.016513	[0.9815, 0.7355, 0.1961, 1.0000]
7 DE	0.323100	0.307249	0.009793	[0.9692, 0.5269, 0.2312, 1.0000]
7 PSO	0.332127	0.320217	0.009676	[0.9391, 0.5217, 0.2172, 0.9699]



**Figure 1.** Voltage-to-current implementations of the PWL function in: voltage-mode  $h_v()$ ; and current-mode  $h_i()$ .



**Figure 2.** OTA-based implementation of Equation (3), where SNLF represents the PWL function in current mode  $h_i()$ .

### 3. CMOS Design of the OTA Enabling the Proposed Current-Mode PWL Function

Figure 3 shows the CMOS topology of the OTA that is designed herein and allows programmability of its transconductance  $g_m$ . Its CMOS design combines a differential pair with source degeneration to linearize  $g_m$ , which is tuned by the feedback resistors R that are designed as active loads using MOSFETs controlled by voltage  $V_c$ , as shown in Figure 4.

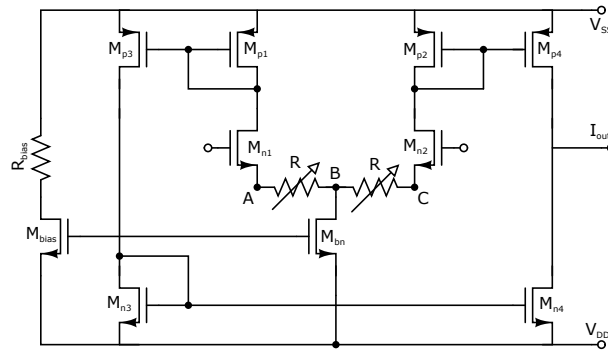


Figure 3. CMOS OTA that allows programmability of  $g_m$ .

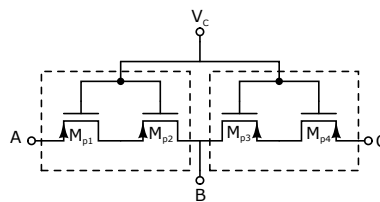


Figure 4. CMOS design of resistors R in Figure 3, allowing programmability of  $g_m$  through  $V_c$ .

Looking at Table 1, the values of the optimized coefficients  $a, b$  and  $d_1$  are in the range  $[0.5, 1]$ , and coefficient  $c$  in the range  $[0.19, 0.5]$ . Therefore, to implement all those combinations of coefficients, the OTA for the former case is designed herein with a central transconductance of  $g_m = 200 \mu\text{A}/\text{V}$ , and with a tunable range of  $\pm 50 \mu\text{A}/\text{V}$ . Considering the ranges of coefficient  $c$ , the OTA is designed with a central transconductance of  $g_m = 50 \mu\text{A}/\text{V}$ , and with a tunable range of  $\pm 50 \mu\text{A}/\text{V}$ . Another OTA is designed to accomplish the slope  $k \geq 10$  required by the PWL function, with a central transconductance of  $g_m = 2 \text{ mA}/\text{V}$ , and with a tunable range of  $\pm 500 \mu\text{A}/\text{V}$ . According to Equation (4), to implement the coefficients to generate seven scrolls (see Table 1, where  $[a, b, c, d_1] = [0.93, 0.52, 0.21, 0.96]$ ), we select  $g_{m_x} = g_{m_y} = g_{m_z} = 200 \mu\text{A}/\text{V}$ ,  $g_{m_a} = 186 \mu\text{A}/\text{V}$ ,  $g_{m_b} = 104 \mu\text{A}/\text{V}$ ,  $g_{m_c} = 41 \mu\text{A}/\text{V}$  and  $g_{m_d} = 1.92 \text{ mA}/\text{V}$ .

The sizes of the OTA having a central value of  $g_m = 200 \mu\text{A}/\text{V}$  are listed in Table 2. Table 3 lists its electrical characteristics. The  $g_m$  is tuned by the feedback resistors R controlled by  $V_c$  in the range  $[-5 \text{ V}, -3 \text{ V}]$ . The sizes of the MOSFETs for the active loads R are:  $M_{p1}-M_{p4}$ ,  $L = 2.1 \mu\text{m}$ ,  $W = 3.8 \mu\text{m}$ , and the multiplication factor  $M = 4$ .

The sizes for the OTA designed with a central transconductance of  $g_m = 50 \mu\text{A}/\text{V}$ , are also listed in Table 2, and Table 3 lists its performance characteristics. These OTAs with centered transconductances at  $g_m = 200 \mu\text{A}/\text{V}$  and  $g_m = 50 \mu\text{A}/\text{V}$  are used to tune the coefficient values  $a, b, c$ , and  $d_1$  listed in Table 1. The integrators and PWL function also require OTAs with transconductance centered at  $g_m = 2 \text{ mA}/\text{V}$ . In this case, the transistor sizes are listed in Table 2, and Table 3 lists its performance characteristics.

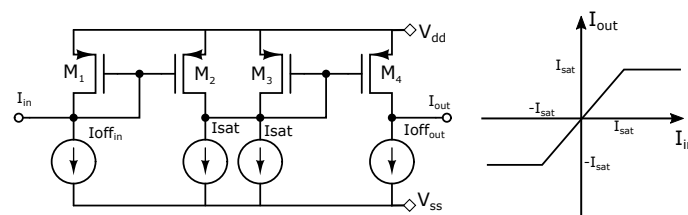
Table 2. Sizes of the OTA with different multiplicity (M) for the  $g_m$  centered at  $200 \mu\text{A}/\text{V}$ ,  $50 \mu\text{A}/\text{V}$  and  $2 \text{ mA}/\text{V}$ .

MOSFET	L ( $\mu\text{m}$ )	W ( $\mu\text{m}$ )	M for $g_m = 200 \mu\text{A}/\text{V}$	M for $g_m = 50 \mu\text{A}/\text{V}$	M for $g_m = 2 \text{ mA}/\text{V}$
$M_{bias}$	1.05	6.15	8	8	8
$M_{bn}$	1.05	6.40	16	16	16
$M_{n1}, M_{n2}$	1.05	29.65	8	8	8
$M_{p1}, M_{p2}$	1.05	15.7	8	8	8
$M_{p3}$	1.05	14.8	8	8	8
$M_{p4}$	1.05	16.8	8	2	80
$M_{n3}$	1.05	6.1	8	8	8
$M_{n4}$	1.05	6.6	8	2	80

**Table 3.** Performance ranges of the programmable OTAs with  $g_m$  centered at 200  $\mu\text{A}/\text{V}$ , 50  $\mu\text{A}/\text{V}$  and 2  $\text{mA}/\text{V}$ .

Parameter	$g_m = 200 \mu\text{A}/\text{V}$	$g_m = 50 \mu\text{A}/\text{V}$	$g_m = 2 \text{mA}/\text{V}$	Units
DC Gain	27.9–31.99	27.89–31.98	37.8–63.98	dB
Transconductance range	151.23–255.94	1.51–2.55	37.8–63.98	$\mu\text{A}/\text{V}$
Input dynamic range	$\pm 1.50$ –0.993	$\pm 1.41$ –0.88	$\pm 1.61$ –2.55	V
Gain-BandWidth	18.04–29.52	5.55–9.37	32.59–45.36	MHz
Output offset	817.65–250.17	817.65–250.17	817.65–45.36	$\mu\text{A}$
Output capacitance	10	10	10	pF
Power consumption @ $I_{bias} = 100 \mu\text{A}$	1.6–1.68	1.4	7.47–7.92	mW

PWL techniques have been used extensively in circuits and systems theory to model nonlinear characteristics of electronic devices [53,54], and to study a large class of nonlinear resistive networks [55,56]. A SNLF series can be generated using the CMOS topology shown in Figure 5 to generate the PWL function that allows programmability of the break-points by tuning the currents  $I_{off\_in}$ ,  $I_{off\_out}$  and  $I_{sat}$  to implement the required plateaus and slopes. This approach has the following advantages: (1) the current mode circuits are in open loop configuration, being unconditionally stable; (2) the current mode blocks have high frequency performance; (3) the simplicity and modularity of the current-mode blocks make them very appropriate to approach a PWL function; (4) a small number of transistors is required for each block; and (5) the current mode blocks allow programmability of the breakpoints for each segment of the PWL function. It should be noted that, to generate a slope  $k = 10$ , it is necessary to inject an input signal  $I'_{in} = 10 \times I_{in}$ . All transistors have sizes  $L = 0.7 \mu\text{m}$  and  $W = 3.5 \mu\text{m}$ , but the multiplicity is 4 for  $M_1, M_3 - M_4$  and 12 for  $M_2$ .



**Figure 5.** CMOS design of the PWL function by cascading simple current mirrors.

#### 4. Integrated Multi-Scroll Chaotic Oscillator Using the Proposed Current Mode PWL Function

The majority of CMOS chaotic oscillators are based on OTAs. For example, the authors in [57] highlighted the benefits of low-voltage implementation, integrability and electronic tunability. Following this direction, in this work, we highlight the programmability of the PWL function enabled through current mode cells and the transconductances of the OTAs to tune the fractional values of the coefficients  $a, b, c$ , and  $d_1$  listed in Table 1. By using the current mode cell shown in Figure 5, we propose the CMOS design sketched in Figure 6 to generate 2–7 scrolls by programming the parallel connection of all the saturated blocks. The current mode blocks are modified by the shift currents  $I_{off\_in}$  and  $I_{off\_out}$ . The saturated regions are limited by the bias current  $I_{sat}$ . That way, to connect  $n - 1$  current mode blocks to generate  $n$ -scroll, a 3–8-bit decoder is designed. As one sees, the input currents to each current mode block are copies of the input current  $I_{in}$ , generated from the class AB current mirror shown in Figure 7. To generate seven scrolls, six copies of the input current are required. The transistor sizes of the multi-output current mirror using 0.35  $\mu\text{m}$  CMOS process from AMS are listed in Table 4. The electrical characteristics are: current gain of 1.005, dynamic range of  $\pm 2 \text{mA}$ ,  $R_{in} = 1.168 \text{K}\Omega$ ,  $R_{out} = 748.4 \text{K}\Omega$ , and  $I_{offset} = 1.28 \mu\text{A}$ .

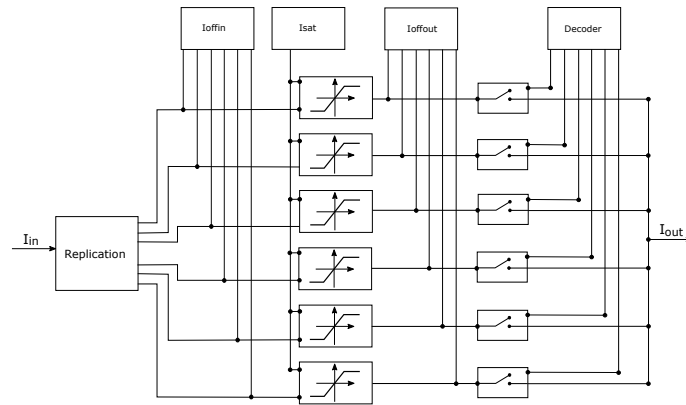


Figure 6. Proposed programmable CMOS current mode PWL function to generate from two to seven scrolls.

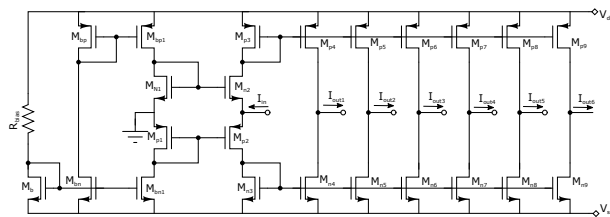
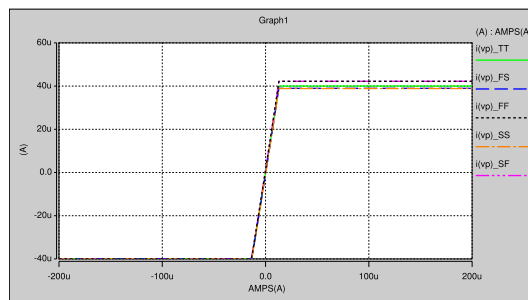


Figure 7. Replication of the input current  $I_{in}$ .

Table 4. Sizes of the current mirror shown in Figure 7.

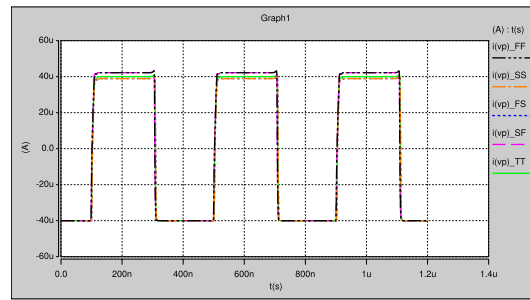
Transistor	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Multiplicity (M)
$M_b, M_{bn}, M_{bn1}$	1.05	12.15	8
$M_{bp}, M_{bp1}$	1.05	30.65	8
$M_{N1}$	0.7	27.8	7
$M_{N2}$	0.7	28.5	4
$M_{P1}$	0.7	59.2	7
$M_{P2}$	0.7	59.5	4
$M_{P3} - M_{P9}$	2	49	4
$M_{N3} - M_{N9}$	2	19.35	4

PVT variation simulations are performed to verify the robustness of our proposed current mode block using the BSIM3v3 model. The tested corners are: (NMOS–PMOS) typical–typical, fast–fast, fast–slow, slow–fast, and slow–slow (TT, FF, FS, SF, and SS, respectively) of the 0.35 $\mu\text{m}$  CMOS technology. The temperature is swept from  $-20\text{ }^\circ\text{C}$  to  $100\text{ }^\circ\text{C}$  in steps of  $40\text{ }^\circ\text{C}$ . Figures 8 and 9 show the PVT simulation results.



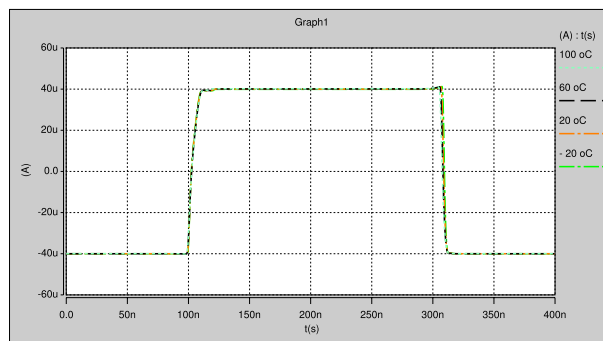
(a)

Figure 8. Cont.

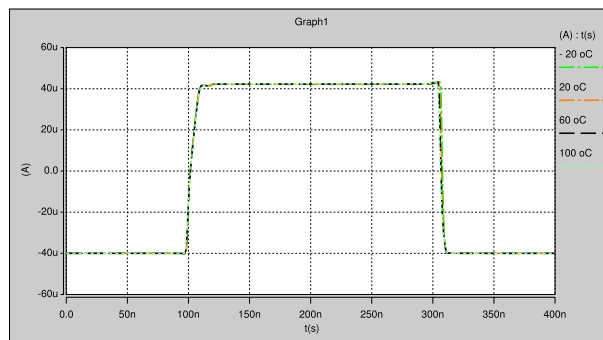


(b)

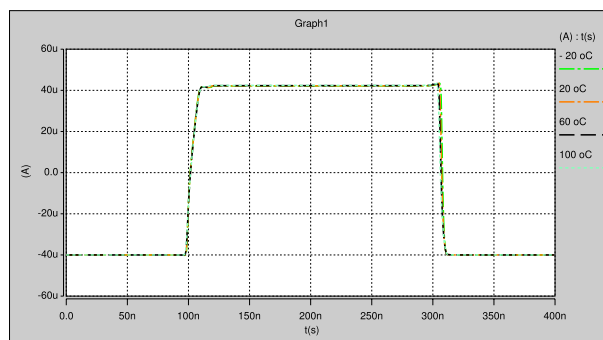
Figure 8. PVT variations for Figure 6 at 5 MHz: (a) DC; and (b) time domain.



(a)



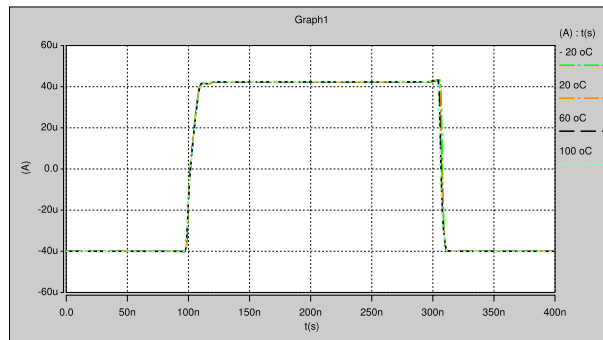
(b)



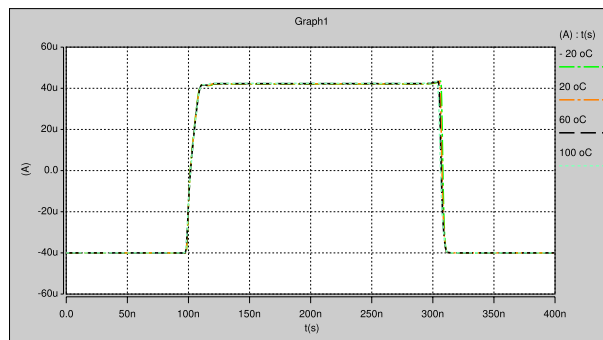
(c)

Figure 9. Cont.





(d)



(e)

Figure 9. Temperature variations of Figure 6 for the cases: (a) TT; (b) SF; (c) FS; (d) SS; and (e) FF.

Figure 10 shows the proposed circuit used to tune  $I_{offin}$  shown in Figure 6. Its sizes are listed in Table 5. Figure 11 shows the proposed circuit to tune  $I_{sat}$  and  $I_{offout}$ , and the transistor sizes are listed in Table 6. Table 7 shows the digital control word and the activation outputs of the 3-to-7-bit digital decoder, which is designed to select the number of current mode building blocks in Figure 6 for the generation of 2–7 scrolls. The output functions are shown in Figure 12, where  $O_0 = A + B + C$ ,  $O_1 = A + B$ ,  $O_2 = A + BC$ ,  $O_3 = A$ ,  $O_4 = AC + AB$ ,  $O_5 = AB$  and  $O_6 = ABC$ .

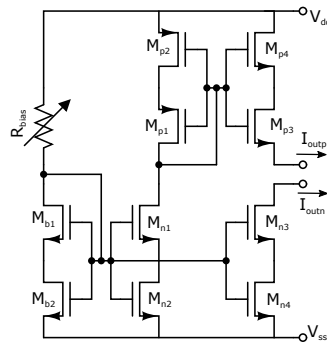


Figure 10. Proposed circuit to tune  $I_{offin}$  in Figure 6.

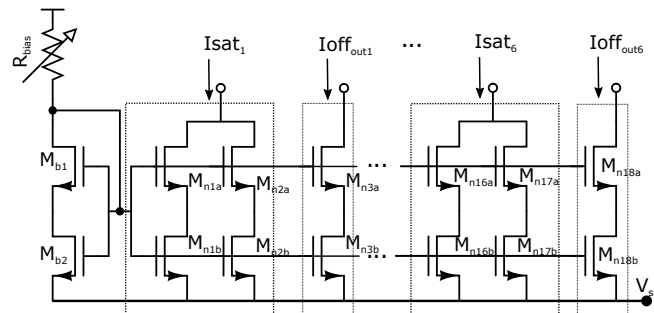


Figure 11. Proposed circuit to tune  $I_{sat}$  and  $I_{off_{out}}$  in Figure 6.

Table 5. Sizes of the circuit in Figure 10.

Transistor	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Multiplicity (M)
$M_{b1}, M_{n1}$	0.7	30	6
$M_{b2}, M_{n2}$	0.7	30	2
$M_{n3}$	0.7	30.2	6
$M_{n4}$	0.7	30.2	2
$M_{p1}$	0.7	90	2
$M_{p2}$	0.7	90	6
$M_{p3}$	0.7	92.4	2
$M_{p4}$	0.7	92.4	6

Table 6. Sizes of the circuit in Figure 11.

Transistor	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Multiplicity (M)
$M_{b1}, M_{n1}$	0.7	3.35	6
$M_{b2}, M_{n2}$	2.5	3.35	2
$M_{n1a}, M_{n2a}$	2.5	3.4	6
$M_{n1b}, M_{n2b}$	2.5	3.4	2
$M_{n3a}, M_{n2a}$	2.5	3.5	6
$M_{n3b}, M_{n2b}$	2.5	3.4	2

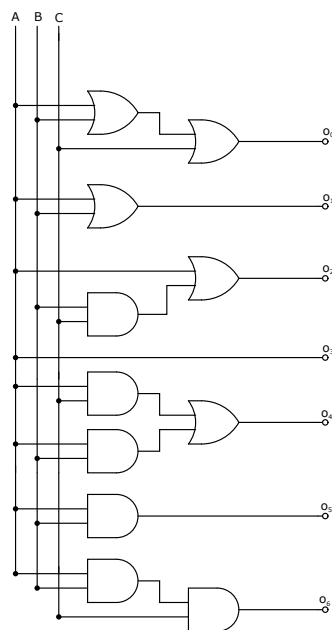
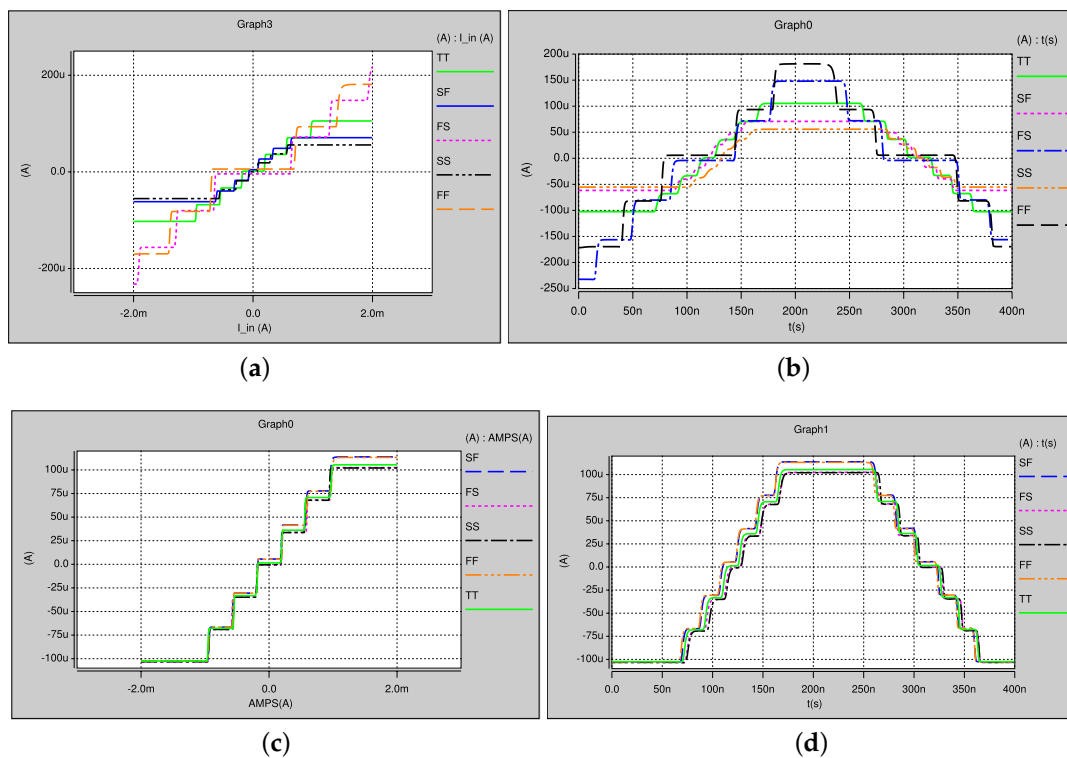


Figure 12. Logic gates to implement the decoder.

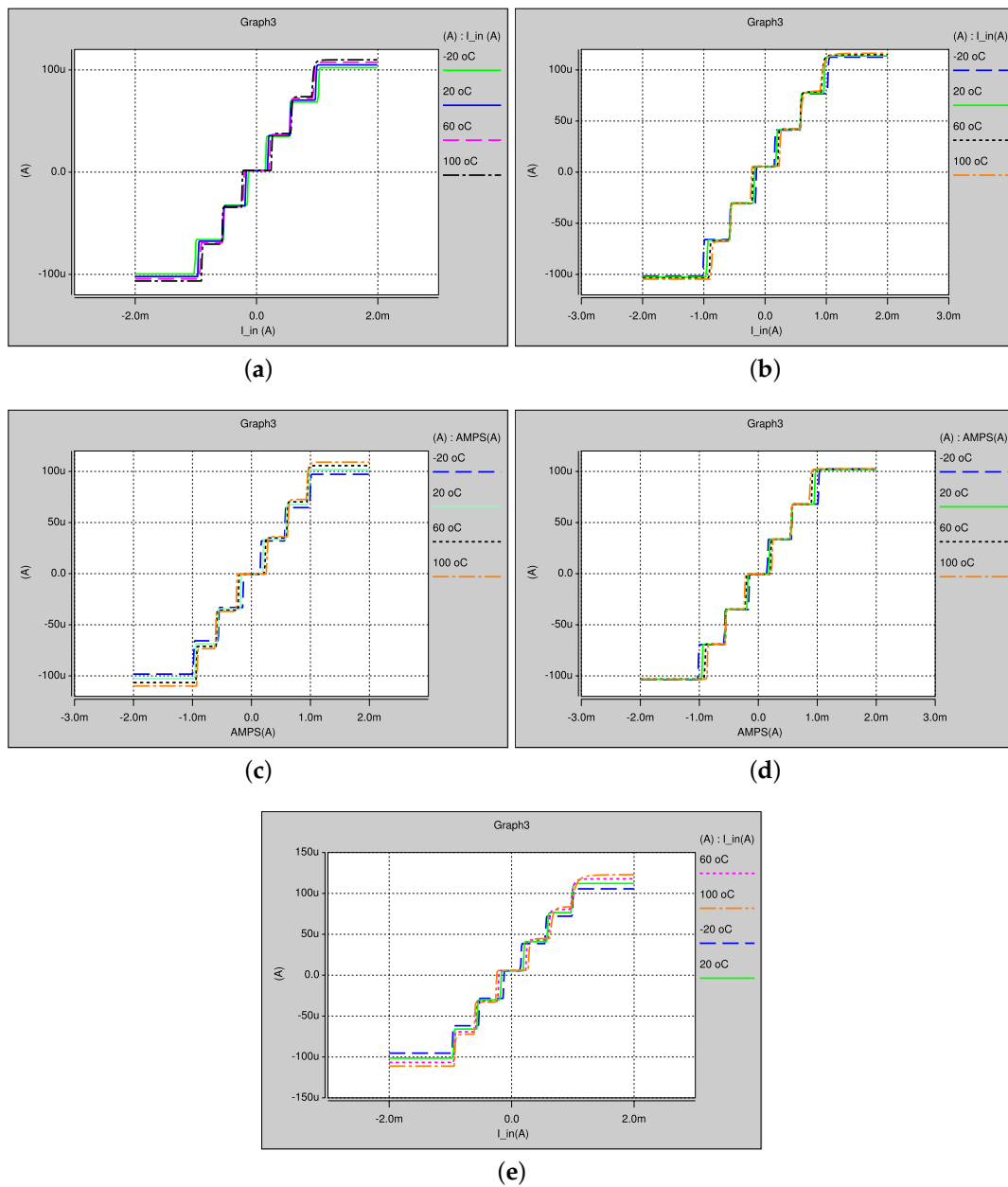
**Table 7.** Decoder 3-to-7-bit control.

A	B	C	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	Scrolls
0	0	0	0	0	0	0	0	0	0	NA
0	0	1	0	0	0	0	0	0	1	2
0	1	0	0	0	0	0	0	1	1	3
0	1	1	0	0	0	0	1	1	1	4
1	0	0	0	0	0	1	1	1	1	5
1	0	1	0	0	1	1	1	1	1	6
1	1	0	0	1	1	1	1	1	1	7
1	1	1	1	1	1	1	1	1	1	NA

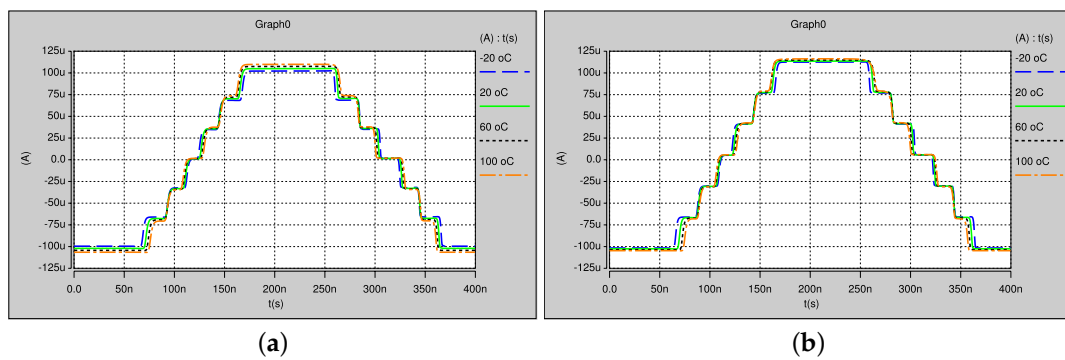
A PWL function to generate two scrolls is implemented by setting the decoder inputs to logic  $A, B, C = [0, 0, 1]$ , i.e.,  $1 = 1.65v$  and  $0 = -1.65v$ . The shift currents are set to  $I_{sat} = I_{offout} = 50 \mu A$ , and  $I_{offin} = 0 \mu A$ . A PWL function to generate three scrolls is implemented by setting  $A, B, C = [0, 1, 0]$ ,  $I_{sat} = I_{offout} = 40 \mu A$ , and  $I_{offin1,2} = \pm 440 \mu A$ . A PWL function to generate four scrolls is implemented by setting  $A, B, C = [011]$ ,  $I_{sat} = I_{offout} = 30 \mu A$ ,  $I_{offin1,2} = 0 \mu A$ , and  $I_{offin3,4} = \pm 660 \mu A$ . A PWL function to generate five scrolls is implemented by setting  $A, B, C = [100]$ ,  $I_{sat} = I_{offout} = 24 \mu A$ ,  $I_{offin1,2} = 264 \mu A$ , and  $I_{offin3,4} = \pm 792 \mu A$ . A PWL function to generate six scrolls is implemented by setting  $A, B, C = [101]$ ,  $I_{sat} = I_{offout} = 20 \mu A$ ,  $I_{offin1,2} = 0 \mu A$ ,  $I_{offin3,4} = \pm 440 \mu A$ , and  $I_{offin5,6} = \pm 880 \mu A$ . Finally, a PWL to generate seven scrolls is implemented by setting  $A, B, C = [110]$ ,  $I_{sat} = I_{offout} = 17.14 \mu A$ ,  $I_{offin1,2} = 188.54 \mu A$ ,  $I_{offin3,4} = \pm 565.73 \mu A$ , and  $I_{offin5,6} = \pm 942.81 \mu A$ . For this last case, we show the simulation results in Figures 13–15, respectively, to conclude that, with adjustment of the current shifts, our proposed current mode PWL function is robust to PVT variations and allows for programmability to choose any value between two- and seven-scroll attractors.



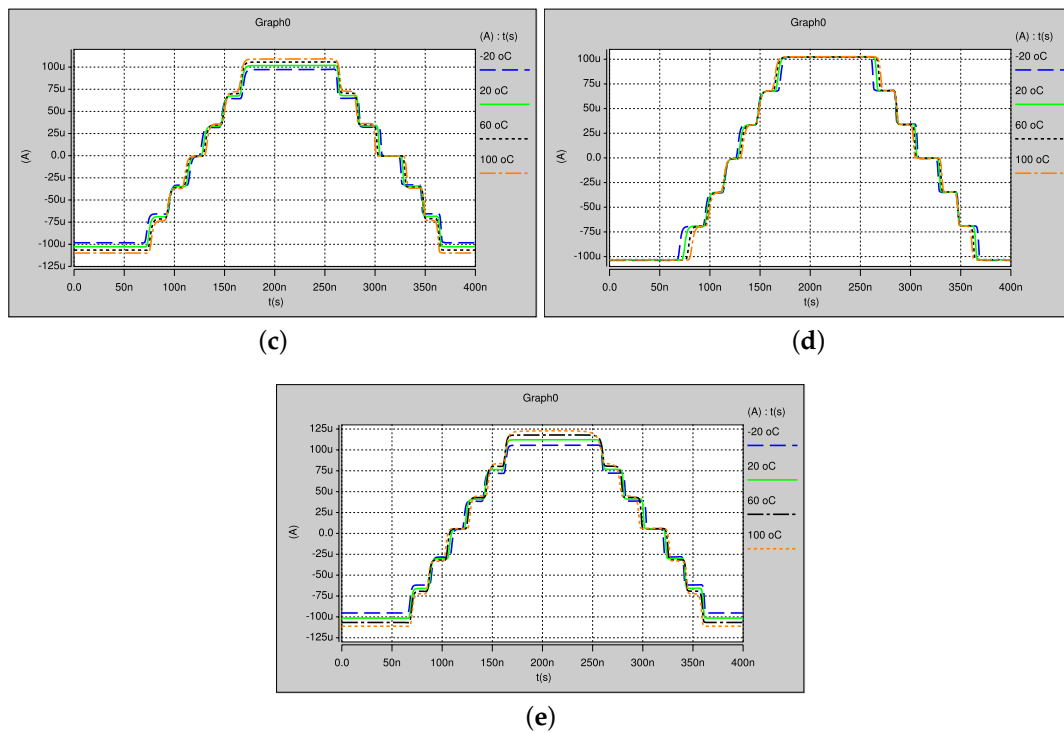
**Figure 13.** PVT simulation of the proposed PWL function to generate seven-scroll: (a,b) without adjustment of the current offsets; and (c,d) with adjustment of the current offsets.



**Figure 14.** Temperature variations of the proposed PWL function in DC to generate seven-scroll: (a) TT; (b) SF; (c) FS; (d) SS; and (e) FF corner.



**Figure 15.** Cont.



**Figure 15.** Temperature variations of the proposed PWL function in time simulation to generate seven-scroll: (a) TT; (b) SF; (c) FS; (d) SS; and (e) FF corner.

### 5. Master–Slave Synchronization of Two Chaotic Oscillators

Chaos synchronization is an important problem in nonlinear science. During the last three decades, synchronization has received a great interest among various scientists [1–7]. The synchronization can be seen as the property shared by some objects to express a uniform rate of coexistence. For example, two harmonic oscillators can be synchronized if their periods are equal. However, for the case of chaotic oscillators, the concepts of frequency and phase are not well defined and, therefore, two chaotic oscillators can be synchronized if eventually, after a transitional time (a long or short time span), the oscillations coincide exactly at all times despite both oscillators started at different initial conditions.

The idea of synchronizing two identical chaotic systems from different initial conditions was introduced in the seminal work in [1]. After that, several synchronization schemes were introduced in [50,58–66]. Besides, the practical applications of chaotic synchronization has some limitations to accomplish identical synchronization. For example, parameter mismatch will probably destroy the manifold of a synchronization. To deal with this issue, generalized synchronization approaches were introduced [3,67]. In this manner, we perform the synchronization of two chaotic oscillators following the approach given in [3]. Therefore, the chaos generator model from Equation (3) in Generalized Hamiltonian form, is given by

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2b} & \frac{1}{2} \\ -\frac{1}{2b} & 0 & 1 \\ -\frac{1}{2} & -1 & 0 \end{bmatrix} \frac{\partial H}{\partial x} + \begin{bmatrix} 0 & \frac{1}{2b} & -\frac{1}{2} \\ \frac{1}{2b} & 0 & 0 \\ -\frac{1}{2} & 0 & -c \end{bmatrix} \frac{\partial H}{\partial x} + \begin{bmatrix} 0 \\ 0 \\ d_1 f(x_1) \end{bmatrix} \quad (5)$$

The Hamiltonian energy function can be described by

$$H(x) = \frac{1}{2}[ax_1^2 + bx_2^2 + x_3^2] \quad (6)$$

and the gradient vector can be described by

$$\frac{\partial H}{\partial x} = \begin{bmatrix} a & 0 & 0 \\ 0 & b & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} ax_1 \\ bx_2 \\ x_3 \end{bmatrix}$$

The destabilizing vector field calls for  $x_1$  and  $x_2$  signals to be used as the outputs of the master model (Equation (5)). The matrices  $C$ ,  $S$ , and  $I$  are given by

$$C = \begin{bmatrix} \frac{1}{a} & 0 & 0 \end{bmatrix}$$

$$S = \begin{bmatrix} 0 & \frac{1}{2b} & -\frac{1}{2} \\ \frac{1}{2b} & 0 & 0 \\ -\frac{1}{2} & 0 & -c \end{bmatrix}$$

$$I = \begin{bmatrix} 0 & \frac{1}{2b} & \frac{1}{2} \\ -\frac{1}{2b} & 0 & 1 \\ -\frac{1}{2} & -1 & 0 \end{bmatrix}$$

The pair  $(C, S)$  is observable. Therefore, the nonlinear state observer for Equation (5) to be used as the slave model is designed as

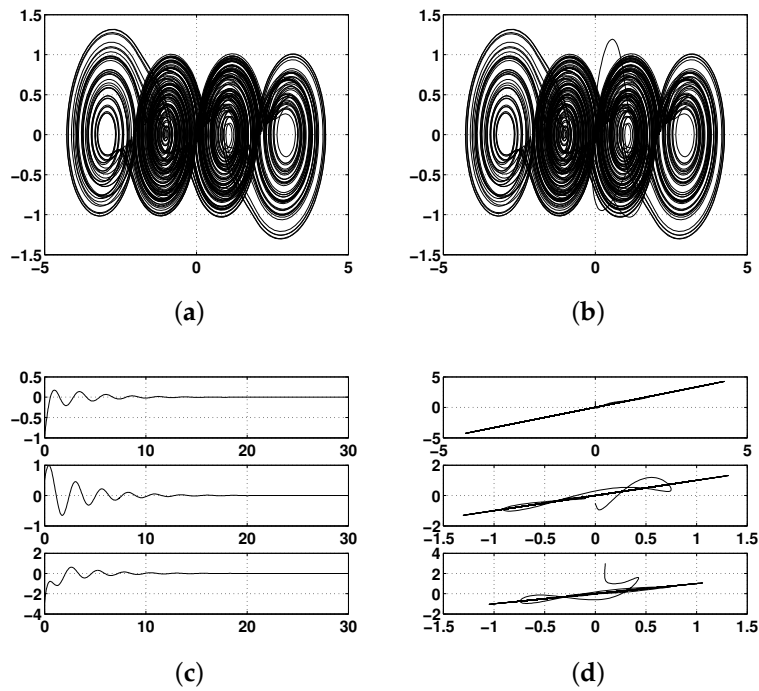
$$\begin{bmatrix} \dot{\xi}_1 \\ \dot{\xi}_2 \\ \dot{\xi}_3 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2b} & \frac{1}{2} \\ -\frac{1}{2b} & 0 & 1 \\ -\frac{1}{2} & -1 & 0 \end{bmatrix} \frac{\partial H}{\partial \xi} + \begin{bmatrix} 0 & \frac{1}{2b} & -\frac{1}{2} \\ \frac{1}{2b} & 0 & 0 \\ -\frac{1}{2} & 0 & -c \end{bmatrix} \frac{\partial H}{\partial \xi} + \dots + \begin{bmatrix} 0 \\ 0 \\ d_1 f(\xi) \end{bmatrix} + \begin{bmatrix} k_1 \\ k_2 \\ k_3 \end{bmatrix} e_y \tag{7}$$

The gains  $k_i, i = 1, 2, 3$  must be selected to guarantee asymptotic exponential stability to zero of the state reconstruction error trajectories (i.e., synchronization error  $e(t)$ ). From Equations (5) and (7), the synchronization error dynamics is governed [21] by

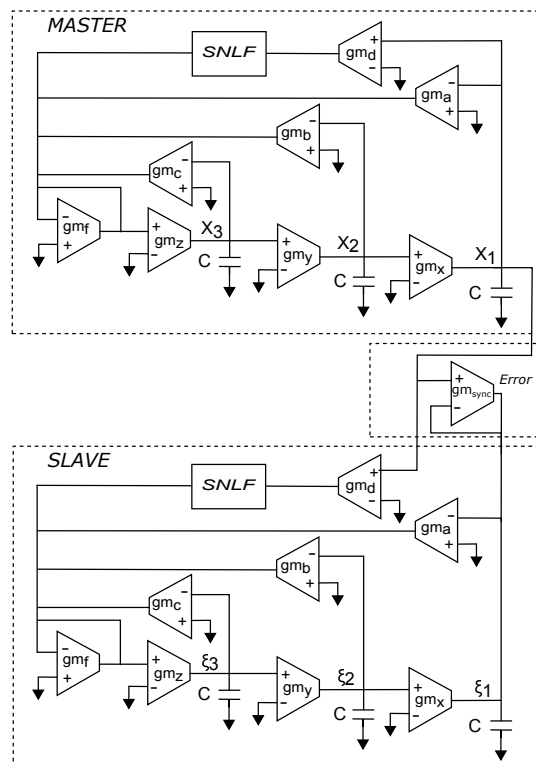
$$\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \\ \dot{e}_3 \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2b} & \frac{1}{2} \\ -\frac{1}{2b} & 0 & 1 \\ -\frac{1}{2} & -1 & 0 \end{bmatrix} \frac{\partial H}{\partial e} + \begin{bmatrix} 0 & \frac{1}{2b} & -\frac{1}{2} \\ \frac{1}{2b} & 0 & 0 \\ -\frac{1}{2} & 0 & -c \end{bmatrix} \frac{\partial H}{\partial e} + \begin{bmatrix} k_1 \\ k_2 \\ k_3 \end{bmatrix} e_y \tag{8}$$

By setting  $K = (k_1, k_2, k_3)^T$  with  $k_1 = 2, k_2 = 5, k_3 = 7$ , and considering the initial condition  $X(0) = [0, 0, 0.1], \xi(0) = [1, -0.5, 3]$ , we performed numerical simulations by using *ode45* in MATLAB, with a time integration of  $T = 2000$  to generate four scrolls. Figure 16 shows the state trajectories of the master and slave models described by Equations (5) and (7), respectively, and their synchronization. The coincidence of the states is represented by a straight line with a unity-slope in the phase plane of each state. The synchronization error is also shown in their transient evolution.

The proposed scheme for the synchronization of multi-scroll chaotic oscillators of the form shown in Equation (3) using OTAs is shown in Figure 17. The vector  $K$  in Equation (7) is the observer gain and it is adjusted by selecting the value of the OTA  $gm_{sync}$  according to the sufficient conditions for synchronization given in [3]. In all our simulations, the values of the transconductances were evaluated as:  $gm_f = gm_x = gm_y = gm_z = 200 \mu A/V$ , and we used the values for  $a, b, c, d_1$  from the cases listed in Table 1 for the PSO algorithm. Those values are tuned from the OTAs with these equations:  $g_{ma} = ag_{mf}, g_{mb} = bg_{mf}, g_{mc} = cg_{mf},$  and  $g_{md} = d_1g_{mf}$ .



**Figure 16.** Master–slave synchronization of two four-scroll chaotic attractors with  $a = b = c = d_1 = 0.7$ : (a) master oscillator; (b) slave oscillator; (c) error synchronization; and (d) error phase diagram for the states of the master  $x$  and the slave  $\xi$ .



**Figure 17.** Synchronization of two multi-scroll chaotic attractors implemented with OTAs and with our proposed current mode PNLF function described by the block SNLNF.

## 6. Layout and Post-Layout Simulations of the Synchronization of Two Multi-Scroll Chaotic Oscillators

The layout of our proposed CMOS programmable current-mode PWL function in Figure 6 is shown in Figure 18. It is used in the complete layout of the OTA-based CMOS multi-scroll chaotic oscillator shown in Figure 19. The dimension of the silicon area is  $900\ \mu\text{m} \times 350\ \mu\text{m}$ . A total of 2005 elements and 175 nodes were required, and a total of 21 inputs/outputs were considered to design the pad frame that contains a protection diode, Vdd, Vss and open contacts to connect the manufactured designs.

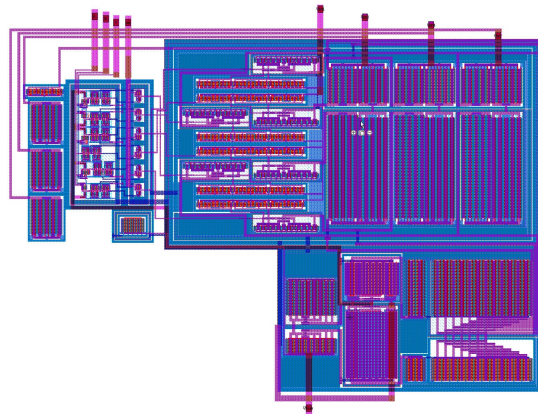


Figure 18. Proposed SNLF Blocks Layout.

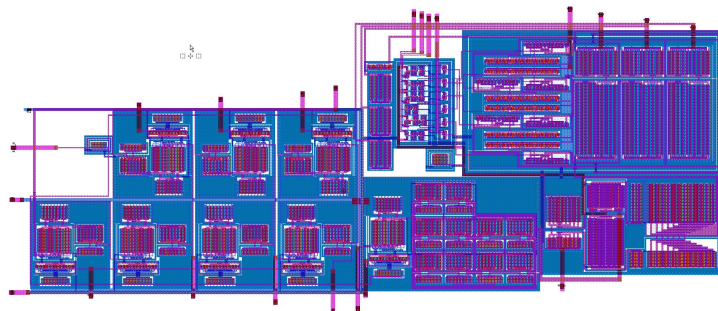
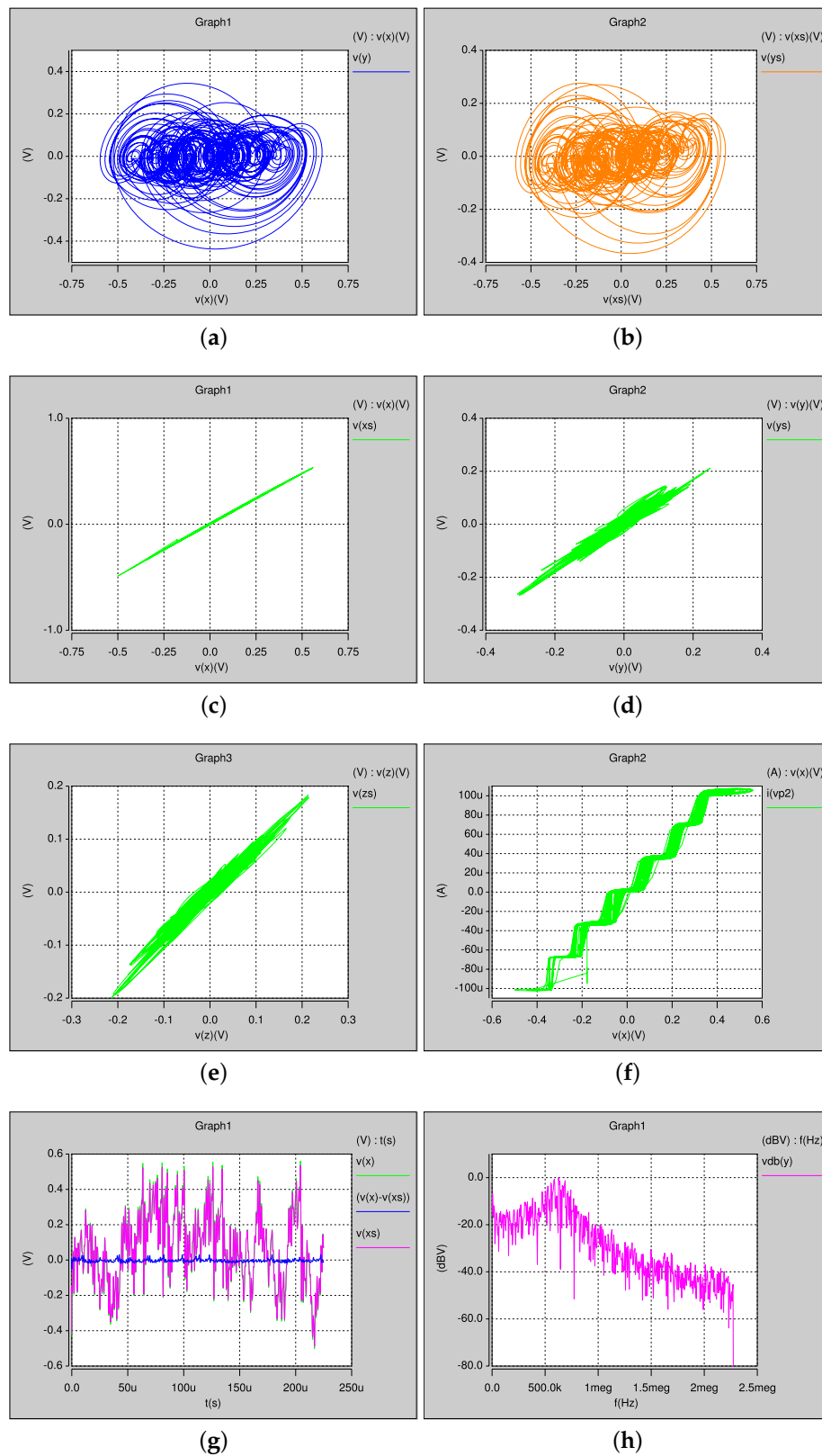


Figure 19. Multi-scroll chaotic oscillator layout

The layout of the CMOS multi-scroll chaotic oscillator was designed by using *Tanner suite* version 16.2, and the post-layout simulations demonstrate that effectively we can program the proposed CMOS current-mode PWL function to generate 2–7 scrolls, as shown in Figure 20. External integration capacitances are used to control the spectra scaling of the system. A 0.5 pF parasitic capacitance and an inductor  $L = 2\text{ nH}$  have been introduced in the simulation at the outputs of the state variables, which resemble the internal IC parasitic elements of the circuit and the pad frame.

A 20 pF parasitic capacitance associated to an oscilloscope was included at the outputs of the state variables, and an external integrator capacitance of  $C = 30\text{ pF}$  was used, calculated to correspond to a 636.62 kHz dominant frequency. Higher frequencies of chaotic oscillation can be reached using bipolar technology [68] to compete with digital implementations [69]. In Figure 20, it can be seen the good synchronization for all the cases when plotting the state variables of the master oscillator  $x$  vs. the slave oscillator  $\zeta$ . This leads us to conclude that these multi-scroll chaotic attractors are robust to PVT variations, they allow programmability to generate 2–7 scrolls, and therefore are quite suitable for the development of applications like chaotic secure communication systems.





**Figure 20.** Post-layout simulation for the synchronization of two seven-scroll chaotic oscillators with optimized MLE: (a) master oscillator showing  $x_1$  vs.  $x_2$ ; (b) slave oscillator showing  $\xi_1$  vs.  $\xi_2$ ; (c) synchronization of  $x_1$  vs.  $\xi_1$ ; (d) synchronization of  $x_2$  vs.  $\xi_2$ ; (e) synchronization of  $x_3$  vs.  $\xi_3$ ; (f) SNLNF  $f(x_1)$  to generate seven-scroll; (g) synchronization error  $x_1 - \xi_1$ ; and (h) FFT analysis of  $x_2$  showing  $f = 626.67$  KHz.

## 7. Conclusions

We have introduced a new CMOS current-mode programmable PWL function using 0.35  $\mu\text{m}$  CMOS technology of AMS. It is used to design a CMOS chaotic oscillator that can be programmed to generate 2–7-scroll attractors. The coefficients  $a, b, c, d_1$  of this chaotic oscillator were tuned by designing programmable OTAs. Using two chaotic oscillators, we showed the implementation of a synchronized master–slave topology, performed by generalized Hamiltonian forms and observer approach.

It was highlighted that the required PWL function, considered as a saturated nonlinear function (SNLF) series, can be implemented in current-mode, and one can take control of the break-points and slopes of the linear segments. The simulation results showed that our CMOS multi-scroll chaotic oscillator is robust to PVT variations. Finally, the simulations performed after the layout parasitic extraction, and the five PVT corner analysis and four temperatures ( $-20\text{ }^\circ\text{C}$ ,  $20\text{ }^\circ\text{C}$ ,  $60\text{ }^\circ\text{C}$  and  $100\text{ }^\circ\text{C}$ ), demonstrate the suitability of our proposed CMOS chaotic oscillator to be used in engineering applications, such as chaotic secure communication systems, healthcare informatics, security, Internet of Things, and so on. These practical applications require low-power consuming circuits, such as our proposed CMOS chaotic oscillator that is also quite suitable to enhance wireless systems.

**Author Contributions:** Investigation, V.H.C.-G., E.T.-C., C.S.-L. and F.V.F.-F.; and Writing—review and editing, V.H.C.-G., E.T.-C. and C.S.-L.

**Funding:** This work was supported in part by the National Council for Science and Technology (CONACyT/Mexico), under Grants 237991 and 222843; in part by Universidad Autónoma de Tlaxcala (UATx), Tlaxcala de Xicohtencatl, TL, Mexico, under Grant CACyPI-UATx-2017; and by the Program to Strengthen Quality in Educational Institutions, under Grant C/PFCE-2016-29MSU0013Y-07-23.

**Conflicts of Interest:** The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

## References

1. Pecora, L.M.; Carroll, T.L. Synchronization in chaotic systems. *Phys. Rev. Lett.* **1990**, *64*, 821. [[CrossRef](#)] [[PubMed](#)]
2. Cuomo, K.M.; Oppenheim, A.V. Circuit implementation of synchronized chaos with applications to communications. *Phys. Rev. Lett.* **1993**, *71*, 65. [[CrossRef](#)] [[PubMed](#)]
3. Sira-Ramirez, H.; Cruz-Hernández, C. Synchronization of chaotic systems: A generalized Hamiltonian systems approach. *Int. J. Bifurc. Chaos* **2001**, *11*, 1381–1395. [[CrossRef](#)]
4. Dachsel, F.; Schwarz, W. Chaos and cryptography. *IEEE Trans. Circuits Syst. I Fund. Theory Appl.* **2001**, *12*, 1498–1509. [[CrossRef](#)]
5. Yu, S.; Ma, Z.; Qiu, S.; Peng, S.; Lin, Q. Generation and synchronization of n-scroll chaotic and hyperchaotic attractors in fourth order systems. *Chin. Phys.* **2004**, pp. 317–328.
6. Stavroulakis, P. *Chaos Applications in Telecommunications*; CRC Press: Boca Raton, FL, USA, 2005.
7. Kapitaniak, T. *Chaos for Engineers: Theory, Applications, and Control*; Springer Science & Business Media: Berlin, Germany, 2012.
8. Goldberger, A.L. Nonlinear dynamics, fractals and chaos: Applications to cardiac electrophysiology. *Ann. Biomed. Eng.* **1990**, *18*, 195–198. [[CrossRef](#)] [[PubMed](#)]
9. Tsonis, A.A. *Chaos: From Theory to Applications*; Springer Science & Business Media: Berlin, Germany, 2012.
10. Degn, H.; Holden, A.V.; Olsen, L.F. *Chaos in Biological Systems*; Springer Science & Business Media: Berlin, Germany, Volume 138, 2013.
11. Weller, R. *Resistance, Chaos and Control in China: Taiping Rebels, Taiwanese Ghosts and Tiananmen*; Springer: Berlin, Germany, 2013.
12. Strogatz, S.H. *Nonlinear Dynamics and Chaos: With Applications to Physics, Biology, Chemistry, and Engineering*; Westview Press: Boulder, CO, USA, 2014.
13. Ditto, W.L.; Sinha, S. Exploiting chaos for applications. *Chaos Interdisciplin. J. Nonlinear Sci.* **2015**, *25*, 097615. [[CrossRef](#)] [[PubMed](#)]

14. Trejo-Guerra, R.; Tlelo-Cuautle, E.; Carbajal-Gómez, V.H.; Rodriguez-Gomez, G. A survey on the integrated design of chaotic oscillators. *Appl. Math. Comput.* **2013**, *219*, 5113–5122. [[CrossRef](#)]
15. Delgado-Restituto, M.; Rodríguez-Vázquez, A. Design considerations for integrated continuous-time chaotic oscillators. *IEEE Trans. Circuits Syst. I Fund. Theory Appl.* **1998**, *45*, 481–495. [[CrossRef](#)]
16. Rodríguez-Vázquez, A.; Delgado-Restituto, M. CMOS design of chaotic oscillators using state variables: A monolithic Chua's circuit. *IEEE Trans. Circuits Syst. II Analog Dig. Signal Process.* **1993**, *40*, 596–613. [[CrossRef](#)]
17. Tlelo-Cuautle, E.; Gaona-Hernández, A.; García-Delgado, J. Implementation of a chaotic oscillator by designing Chua's diode with CMOS CFOAs. *Analog Integr. Circuits Signal Process.* **2006**, *48*, 159–162. [[CrossRef](#)]
18. Sánchez-López, C.; Castro-Hernández, A.; Pérez-Trejo, A. Experimental verification of the Chua's circuit designed with UGCs. *IEICE Electron. Express* **2008**, *5*, 657–661. [[CrossRef](#)]
19. Trejo-Guerra, R.; Tlelo-Cuautle, E.; Sánchez-López, C.; Munoz-Pacheco, J.; Cruz-Hernández, C. Realization of multiscroll chaotic attractors by using current-feedback operational amplifiers. *Rev. Mex. Fis.* **2010**, *56*, 268–274.
20. Sanchez-Lopez, C.; Tlelo-Cuautle, E.; Carrasco-Aguilar, M.; Morales-López, F.; Cante-Michcol, B. Multi-scroll chaotic oscillator employing UGCs. In Proceedings of the International Conference on Electrical, Communications, and Computers, Cholula, Mexico, 26–29 February 2009; pp. 189–191.
21. Muñoz-Pacheco, J.M.; Zambrano-Serrano, E.; Félix-Beltrán, O.; Gómez-Pavón, L.C.; Luis-Ramos, A. Synchronization of PWL function-based 2D and 3D multi-scroll chaotic systems. *Nonlinear Dyn.* **2012**, *70*, 1633–1643. [[CrossRef](#)]
22. Munoz-Pacheco, J.; Tlelo-Cuautle, E. *Electronic Design Automation of Multi-Scroll Chaos Generators*; Bentham Sciences Publishers: Dubai, UAE, 2010.
23. Muñoz-Pacheco, J.; Tlelo-Cuautle, E. Automatic synthesis of 2D-n-scroll chaotic systems by behavioral modeling. *J. Appl. Res. Technol.* **2009**, *7*, 5–14.
24. Zhou, T.; Chen, G. Classification of chaos in 3-D autonomous quadratic systems-I: Basic framework and methods. *Int. J. Bifurc. Chaos* **2006**, *16*, 2459–2479. [[CrossRef](#)]
25. Varrientos, J.E.; Sánchez-Sinencio, E. A 4-D chaotic oscillator based on a differential hysteresis comparator. *IEEE Trans. Circuits Syst. I Fund. Theory Appl.* **1998**, *45*, 3–10. [[CrossRef](#)]
26. Lü, J.; Chen, G. Generating multiscroll chaotic attractors: theories, methods and applications. *Int. J. Bifurc. Chaos* **2006**, *16*, 775–858. [[CrossRef](#)]
27. Trejo-Guerra, R.; Tlelo-Cuautle, E.; Jiménez-Fuentes, M.; Muñoz-Pacheco, J.; Sánchez-López, C. Multiscroll floating gate-based integrated chaotic oscillator. *Int. J. Circuit Theory Appl.* **2013**, *41*, 831–843. [[CrossRef](#)]
28. Trejo-Guerra, R.; Tlelo-Cuautle, E.; Jiménez-Fuentes, J.; Sánchez-López, C.; Muñoz-Pacheco, J.; Espinosa-Flores-Verdad, G.; Rocha-Pérez, J. Integrated circuit generating 3-and 5-scroll attractors. *Commun. Nonlinear Sci. Numer. Simul.* **2012**, *17*, 4328–4335. [[CrossRef](#)]
29. de la Fraga, L.G.; Tlelo-Cuautle, E.; Carbajal-Gómez, V.; Munoz-Pacheco, J. On maximizing positive Lyapunov exponents in a chaotic oscillator with heuristics. *Rev. Mex. Fis* **2012**, *58*, 274–281.
30. Carbajal-Gómez, V.H.; Tlelo-Cuautle, E.; Fernández, F.V. Optimizing the positive Lyapunov exponent in multi-scroll chaotic oscillators with differential evolution algorithm. *Appl. Math. Comput.* **2013**, *219*, 8163–8168. [[CrossRef](#)]
31. de la Fraga, L.G.; Tlelo-Cuautle, E. Optimizing the maximum Lyapunov exponent and phase space portraits in multi-scroll chaotic oscillators. *Nonlinear Dyn.* **2014**, *76*, 1503–1515. [[CrossRef](#)]
32. Carbajal-Gómez, V.; Tlelo-Cuautle, E.; Fernández, F.; de la Fraga, L.; Sánchez-López, C. Maximizing Lyapunov Exponents in a Chaotic Oscillator by Applying Differential Evolution. *Int. J. Nonlinear Sci. Numer. Sim.* **2014**, *15*, 11–17. [[CrossRef](#)]
33. Wolf, A.; Swift, J.B.; Swinney, H.L.; Vastano, J.A. Determining Lyapunov exponents from a time series. *Phys. D Nonlinear Phenom.* **1985**, *16*, 285–317. [[CrossRef](#)]
34. Barna, G.; Tsuda, I. A new method for computing Lyapunov exponents. *Phys. Lett. A* **1993**, *175*, 421–427. [[CrossRef](#)]
35. Dieci, L. Jacobian free computation of Lyapunov exponents. *J. Dyn. Differ. Equ.* **2002**, *14*, 697–717. [[CrossRef](#)]

36. Rugonyi, S.; Bathe, K.J. An evaluation of the Lyapunov characteristic exponent of chaotic continuous systems. *Int. J. Numer. Methods Eng.* **2003**, *56*, 145–163. [[CrossRef](#)]
37. Chen, Z.M.; Djidjeli, K.; Price, W. Computing Lyapunov exponents based on the solution expression of the variational system. *Appl. Math. Comput.* **2006**, *174*, 982–996. [[CrossRef](#)]
38. Yang, C.; Zhu, W.; Ren, G. Approximate and efficient calculation of dominant Lyapunov exponents of high-dimensional nonlinear dynamic systems. *Commun. Nonlinear Sci. Numer. Simul.* **2013**, *18*, 3271–3277. [[CrossRef](#)]
39. Banks, J.; Brooks, J.; Cairns, G.; Davis, G.; Stacey, P. On Devaney's definition of chaos. *Am. Math. Mon.* **1992**, *99*, 332–334. [[CrossRef](#)]
40. Cook, P. *Nonlinear Dynamical Systems*; Prentice Hall: Upper Saddle River, NJ, USA, 1994.
41. Parker, T.S.; Chua, L.O. *Practical Numerical Algorithms for Chaotic Systems*; Springer: New York, NY, USA, 1989.
42. Hoppensteadt, F.C. *Analysis and Simulation of Chaotic Systems*; Springer: Berlin, Germany, 2000.
43. Birta, L.G.; Arbez, G. *Modelling and Simulation: Exploring Dynamic System Behaviour*; Springer: Berlin, Germany, 2007.
44. Zelinka, G.; Chen, S. Chaos synthesis by means of evolutionary algorithms. *Int. J. Bifurc. Chaos* **2008**, *18*, 911–942. [[CrossRef](#)]
45. Gálvez, A. Numerical-Symbolic MATLAB Program for the analysis of three-dimensional chaotic systems. In *International Conference on Computational Science*; Springer: Berlin/Heidelberg, Germany, 2007; pp. 211–218.
46. Li, S.; Mou, X.; Cai, Y.; Ji, Z.; Zhang, J. On the security of a chaotic encryption scheme: Problems with computerized chaos in finite computing precision. *Comput. Phys. Commun.* **2003**, *153*, 52–58. [[CrossRef](#)]
47. Lü, J.; Chen, G. Design and Analysis of Multiscroll Chaotic Attractors From Saturated Function Series. *IEEE Trans. Circuits Syst.* **2004**, *51*, 2476–2490. [[CrossRef](#)]
48. Lü, J.; Yu, S.; Leung, H.; Chen, G. Experimental verification for 3-D hysteresis multiscroll chaotic attractors. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'05), Kobe, Japan, 23–26 May 2005.
49. Schuster, H.G.; Just, W. *Deterministic Chaos: An Introduction*; John Wiley & Sons: Hoboken, NJ, USA, 2006.
50. Grigoras, V.; Grigoras, C. Digital Data Encryption Based on Discrete Additive Systems. In *Topics on Chaotic Systems, Selected Papers from CHAOS 2008 International Conference*; World Scientific Publishing Co. World Scientific: Singapore, 2009; pp. 149–157.
51. Carbajal-Gómez, V.H.; Tlelo-Cuautle, E.; Fernández, F.V. Application of Computational Intelligence Techniques to Maximize Unpredictability in Multiscroll Chaotic Oscillators. In *Computational Intelligence in Analog and Mixed-Signal (AMS) and Radio-Frequency (RF) Circuit Design*; Springer: Berlin, Germany, 2015; pp. 59–81.
52. Trejo-Guerra, R.; Tlelo-Cuautle, E.; Munoz-Pacheco, J.; Sánchez-López, C.; Cruz-Hernández, C. On the Relation between the Number of Scrolls and the Lyapunov Exponents in PWL-functions-based  $\eta$ -Scroll Chaotic Oscillators. *Int. J. Nonlinear Sci. Numer. Simul.* **2010**, *11*, 903–910. [[CrossRef](#)]
53. Chua, L.O. *Introduction to Nonlinear Network Theory*; McGraw-Hill: New York, NY, USA, 1969.
54. Chua, L. *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques*; Prentice Hall: Upper Saddle River, NJ, USA, 1975.
55. Chien, M.J.; Kuh, E.S. Solving nonlinear resistive networks using piecewise-linear analysis and simplicial subdivision. *IEEE Trans. Circuits Syst.* **1977**, *24*, 305–317. [[CrossRef](#)]
56. Bazaraa, M.S.; Sherali, H.D.; Shetty, C.M. *Nonlinear Programming: Theory and Algorithms*; John Wiley & Sons: Hoboken, NJ, USA, 2013.
57. Dar, M.R.; Kant, N.A.; Khanday, F.A. Realization of Integrable Incommensurate-Fractional-Order-Rössler-System Design Using Operational Transconductance Amplifiers (OTAs) and Its Experimental Verification. *Int. J. Bifurc. Chaos* **2017**, *27*, 1750077. [[CrossRef](#)]
58. Carroll, T.L.; Pecora, L.M. Synchronizing chaotic circuits. *IEEE Trans. Circuits Syst.* **1991**, *38*, 453–456. [[CrossRef](#)]
59. Zeng, Y.; Singh, S.N. Adaptive control of chaos in Lorenz system. *Dyn. Control* **1997**, *7*, 143–154. [[CrossRef](#)]
60. Agiza, H.; Yassen, M. Synchronization of Rossler and Chen chaotic dynamical systems using active control. *Phys. Lett. A* **2001**, *278*, 191–197. [[CrossRef](#)]
61. Kocarev, L. Chaos-based cryptography: A brief overview. *IEEE Circuits Syst. Mag.* **2001**, *1*, 6–21. [[CrossRef](#)]

62. Yassen, M. Adaptive control and synchronization of a modified Chua's circuit system. *Appl. Math. Comput.* **2003**, *135*, 113–128. [[CrossRef](#)]
63. Huang, L.; Feng, R.; Wang, M. Synchronization of chaotic systems via nonlinear control. *Phys. Lett. A* **2004**, *320*, 271–275. [[CrossRef](#)]
64. Yassen, M. Chaos synchronization between two different chaotic systems using active control. *Chaos Solitons Fractals* **2005**, *23*, 131–140. [[CrossRef](#)]
65. Guyeux, C.; Bahi, J. A new chaos-based watermarking algorithm. In Proceedings of the 2010 International Conference on Security and Cryptography (SECRYPT), Athens, Greece, 26–28 July 2010; pp. 455–458.
66. Volos, C.; Kyprianidis, I.; Stouboulos, I.; Pham, V.T. Radio Frequency Chaotic Circuit Design: From Theory to Practice. In *Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design*; IGI Global: Hershey, PA, USA, 2014; p. 364.
67. Rulkov, N.F.; Sushchik, M.M.; Tsimring, L.S.; Abarbanel, H.D. Generalized synchronization of chaos in directionally coupled chaotic systems. *Phys. Rev. E* **1995**, *51*, 980. [[CrossRef](#)]
68. Efremova, E.V.; Dmitriev, A.S. Ultrawideband Microwave 3-to-7 GHz Chaotic Oscillator Implemented as SiGe Integrated Circuit. In *Emergent Complexity from Nonlinearity, in Physics, Engineering and the Life Sciences*; Mantica, G., Stoop, R., Stramaglia, S., Eds.; Springer International Publishing: Cham, Switzerland, 2017; pp. 71–80.
69. Karimov, T.I.; Butusov, D.N.; Pesterev, D.O.; Predtechenskii, D.V.; Tedoradze, R.S. Quasi-chaotic mode detection and prevention in digital chaos generators. In Proceedings of the 2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus), Moscow, Russia, 29 January–1 February 2018; pp. 303–307.



© 2018 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).