Load-independent characterization of trade-off fronts for operational amplifiers

Abstract—**In emerging design methodologies for analog integrated circuits, the use of performance trade-off fronts, also known as Pareto fronts, is a keystone to overcome the limitations of the traditional top-down methodologies. However, most techniques reported so far to generate the front neglect the effect of the surrounding circuitry (such as the output load impedance) on the Pareto-front, thereby making it only valid for the context where the front was generated. This strongly limits its use in hierarchical analog synthesis because of the heavy dependence of key performances on the surrounding circuitry, but, more importantly, because this circuitry remains unknown until the synthesis process. We will address this problem by proposing a new technique to generate the trade-off fronts that is independent of the load that the circuit has to drive. This idea is exploited for a commonly used circuit, the operational amplifier, and experimental results show that this is a promising approach to solve the issue.**

Keywords - Analog synthesis; Multi-objective optimization; Pareto-optimal fronts; Hierarchical synthesis.

I. INTRODUCTION

Analog integrated circuits still lag behind in comparison to their digital counterpart in terms of Electronic Design Automation. Beyond any single reason, the inherent complexity of designing the simplest of the analog systems (the many non-ideal effects, the larger sensitivity to noise, etc.) has hindered the same pace of evolution in systematic design methodologies.

A hot topic in this sense is the systematization of hierarchical design of analog circuits. This process begins with the system requirements and ends at the device level, with the specification of transistor sizes, values of all passive devices, and so on. The facts that most building blocks in any analog hierarchy feature a multi-dimensional space of performance characteristics and that the mapping between design objectives (or performances) and design variables (like the W and L of a transistor) is an involved problem, make analog hierarchical synthesis a very complex problem.

Traditionally, this problem has been addressed by using a top-down design approach [1], where the system is hierarchically decomposed in different sub-system building blocks, down to the device level. At each hierarchical level, an appropriate architecture is selected for each block and its specifications are transmitted into a sub-set of specifications for each of the sub-blocks. The top-down specification transmission process ends up when the device level is reached, i.e., specification transmission at that level implies obtaining device sizes.

However, this approach has two important flaws: first, it does not guarantee the feasibility of the building blocks (as their requirements are being derived in the specification transmission process) since it is unknown if these requirements are realizable or not at lower hierarchical levels; second, there are not accurate estimates of power consumption and area occupation at the beginning of the specification transmission process (at any intermediate hierarchical level) since these two figures depend also on low-level details, not known at this early stage of the design.

In the recently proposed multi-objective bottom-up (MOBU) approach [2], the hierarchy is handled in a bottom-up-first way by means of the concept of Pareto-optimal front (POF), a promising resource to palliate the drawbacks of traditional top-down design methodologies [3][4][5]. A POF is the set of different instances or designs (e.g., different sizing) of a circuit block that best characterizes the trade-offs between competing performances, like power vs. speed. Generating the POF is a multi-objective optimization problem, typically solved by a population-based optimization algorithm, coupled to a performance evaluator (such as an electrical simulator). POF generation typically involves many thousands of simulations and, hence, quite long computation times. The ultimate potential of the POF concept is that, once generated, it could be used wherever and whenever necessary, that is, in any synthesis problem involving such building blocks. Notice that the front establishes fully defined, bi-univocal relations between performances and device sizes. In this way, it is in principle possible to hierarchically compose all the building blocks's trade-off fronts to obtain the complete trade-off front of an analog system. Then, mapping the systems requirements becomes a rapid, straightforward process, where, both feasibility and accurate estimates are guaranteed.

However, there still lies a fundamental issue: that the ultimate value of many commonly used performance characteristics of analog circuits do not only depend on the block itself, but on its surrounding circuitry. That is, the

generated Pareto-front depends on the context where the analog building block is being used. Consider, for instance, the load impedance that a typical analog block such as the operational amplifier has to drive. For instance, if the operational amplifier is required to have a dc gain of 50dB when a 5kΩ-load is at its output and the Pareto front was obtained with a 100kΩ-load, then the selected designs may turn useless, possibly because their output impedances are much larger than 5kΩ. This same situation arises in hierarchical synthesis, because, as said above, the surrounding circuitry of the building block is unknown (and so is the load impedance). It is essential to stress the importance of this fact, because the use of POFs to solve the issues of top-down design and improve the systematic design of analog circuits is heavily compromised by this limitation.

In the application of the MOBU methodology to a real-life design problem, a ΔΣ A/D converter [6], the problems with the surrounding circuitry have been circumvented by selecting only those designs from the Pareto fronts of the different building blocks that meet certain constraints: for instance, that the output impedance of the DAC block is higher than the output resistance of the corresponding integrator, or that the first non-dominant pole of the output impedance of the DAC is significantly higher than the integrator gain-bandwidth product. The problem is that this is an *ad-hoc* solution, that overly constrains the design problem and limits the effectiveness of POF-based synthesis as only a small fraction of designs of the POF are eventually used (imposing the above described constraints leads to an important reduction in the number of valid solutions for the converter, for which there initially were over a hundred valid designs for each building block).

Our proposed approach is to generate Pareto fronts of analog circuits that circumvent the dependence with the surrounding circuitry. In this paper, we develop this approach for operational amplifiers, for which a methodology to transform the POF of small-signal characteristics among arbitrary load conditions is introduced

Section II describes Pareto-optimal fronts and the computational techniques for obtaining them. Section III introduces the generation of POFs independently of the surrounding circuitry. Section IV is devoted to discuss different strategies for the application of these POFs, mainly to hierarchical synthesis problems. Finally, conclusions are presented in Section V.

II. Generation of Pareto-optimal Fronts

Generation of the POF for the selected performances of a circuit block can be posed as a multi-objective optimization problem. This problem is formulated by maximizing or minimizing, simultaneously, a set of b design objectives, $\boldsymbol{y} = \boldsymbol{f}(\boldsymbol{x}) = \{f_1(\boldsymbol{x}), f_2(\boldsymbol{x}), \cdots, f_b(\boldsymbol{x})\}$, where $\boldsymbol{x}$ is a vector of design variables (e.g. device sizes, performance characteristics of sub-blocks at intermediate hierarchical levels), and each $f_i(\mathbf{x})$ is a performance characteristic of the block (such as dc gain), subject to some constraints (e.g., slew rate larger than a certain value). The problem can be mathematically posed by following the next formulation:

$$\min_{\boldsymbol{x}} \boldsymbol{f}(\boldsymbol{x}) \quad \text{subject to} \begin{cases} \boldsymbol{g}(\boldsymbol{x}) \geq 0 \\ \boldsymbol{X}_L < \boldsymbol{x} < \boldsymbol{X}_H \end{cases} \tag{1}$$

where $\boldsymbol{X}_L$ and $\boldsymbol{X}_H$ are the lower and upper bounds to the $\boldsymbol{x}$ vector, respectively. Vector $\boldsymbol{g}(\boldsymbol{x}) \geq 0$ corresponds to the user-defined constraints, delimiting the feasible region. A design point, $\boldsymbol{a} \in \boldsymbol{X}$, is said to *dominate* another design point, $\boldsymbol{b} \in \boldsymbol{X}$, (noted as $\boldsymbol{a} \prec \boldsymbol{b}$) if $\boldsymbol{F}(\boldsymbol{a}) \leq \boldsymbol{F}(\boldsymbol{b})$ and $f_i(\boldsymbol{a}) < f_i(\boldsymbol{b})$ for at least one function i[1]. The design point $\boldsymbol{a}$ is said to be *non-dominated* if there is no other design that dominates it. The non-dominated set of the entire feasible search space is known as the Pareto-optimal front. All these concepts are illustrated in Figure 1 for a two performance front.

The computation of the Pareto front is typically efficiently and accurately done by using multi-objective evolutionary algorithms [7], coupled to an electrical simulator (e.g., HSPICE). These algorithms start with a random population of individuals that, after being evaluated by the electrical simulator, is modified in such a way that after n iterations (called generations) a population of non-dominated individuals is obtained, the Pareto-optimal front. Being of stochastic nature, the computational cost due to the high number of required fitness evaluations (circuit simulations) is the main drawback of these algorithms [8]. Efficiency, convergence to the true POF, and diversity of solutions are areas of intense and current research. An example is the definition of new quality evaluation metrics suitable to analog design problems proposed in [9].

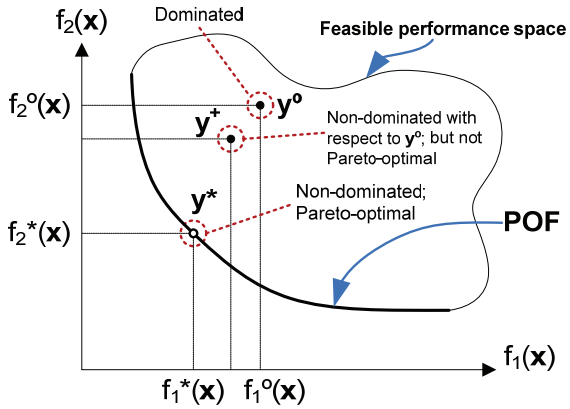

Figure 1. Illustrating the Pareto-optimal front concept for a two-dimensional front.

[1] This formulation is valid for minimization problems. A simple change of sign applies for maximization.

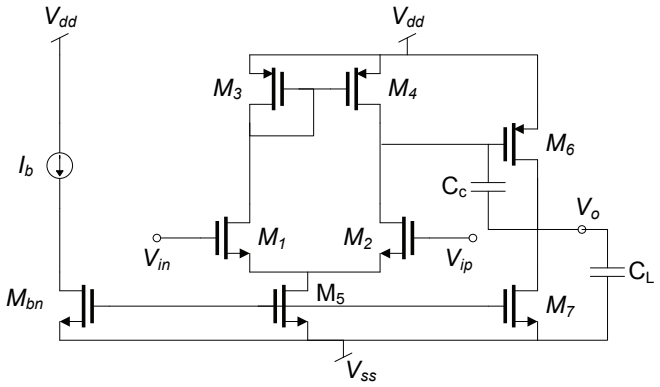

Figure 2. Miller operational amplifier used in this work.

In order to illustrate the potentiality of POFs, let us consider the Miller operational amplifier depicted in Figure 2, for which the performances of interest are: dc gain, A_0 , unity-gain frequency, f_u , phase margin, *PM,* and output impedance, Z_o . The optimization process aims at maximizing the first three performances (A_0 , f_u and *PM*) and minimizing Z_o . Some of these performances depend on the load conditions, so when the POF for this block is generated, a load will be included in the evaluation of the individuals of the POF. The design variables in this case are the width and length of the transistors, plus the bias current and the compensation capacitor. Different constraints are imposed to the problem in order to obtain correct and useful sized circuits; for example, dc gain is set to be larger than 20dB, and phase margin $90^o > PM > 10^o$. The POF with a capacitive load of 1pF was generated by coupling the electrical simulator HSPICE to the multi-objective evolutionary optimization algorithm NSGAII [10]. The population size and number of generations were 1500 and 150, respectively. Generation of this POF took about 1 hour 36 minutes of CPU time on a 2.2 GHz processor. The result is obviously 1500 sample points of the 4-dimensional POF. For illustration purposes, Figure 3 shows the projections of the 1500 points of this 4-dimensional hypersurface on the dc gain vs. unity-gain frequency plane, on the phase margin vs. unity-gain-frequency plane, and on the dc gain vs. output impedance plane. Each of these points represents a sized circuit showing the best trade-offs among the four performances considered.

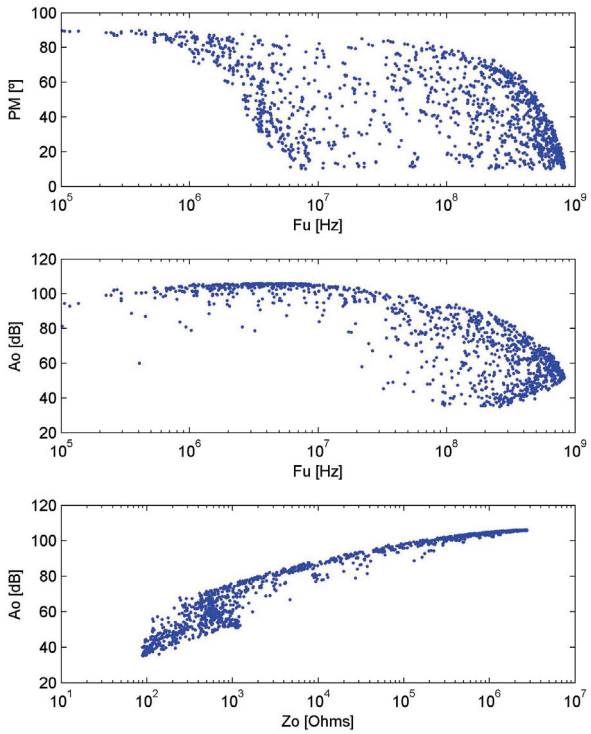

Figure 3. Projections of the POF generated by the multiobjective optimization algorithm for a capacitive load of 1pF.

III. LOAD-INDEPENDENT PARETO-OPTIMAL FRONTS

A. *POF Generation Methodogy*

Let us consider the same amplifier and the same performances used in Section II. As already mentioned, some of these performances depend on the load conditions. However, the load conditions are not known until the synthesis process is being performed, that is, until any other circuitry around the amplifier is known. Since the POF generation process is a computationally expensive process, the objective of our research is to generate trade-off information a priori and easily and efficiently transform this information into the POFs of performances (A_0 , f_u , *PM,* and Z_o) when the load conditions are known.

The operational amplifier can be considered a two-port, like that shown in Figure 4. Voltage v_1 and current i_1 represent the differential input voltage and current respectively. Voltage v_2 and current i_2 represent the output voltage and current respectively (in case of single output) and the differential output voltage and current (in case of fully differential amplifier). As we need a load-independent characterization of the amplifier, we may consider, a priori, any matrix characterization of two-ports [11]. However, the two-port matrix parameters must be selected intelligently, according to the performances of interest of the block. Let us consider the hybrid-2 parameters [11] to characterize the two-port:

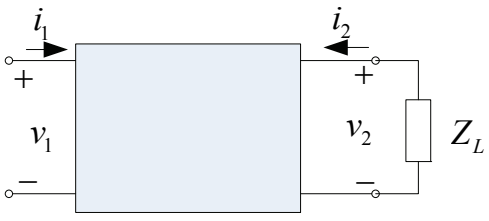

Figure 4. Two-port with arbitrary load.

$$i_1 = h'_{11} \cdot v_1 + h'_{12} \cdot i_2$$
$$v_2 = h'_{21} \cdot v_1 + h'_{22} \cdot i_2 \quad (2)$$

In this equation, parameter h'_{11} represents the input impedance, h'_{12} is the inverse current gain, h'_{21} represents the voltage gain of the amplifier without any load and h'_{22} is the output impedance. The voltage gain and output impedance when a certain load Z_L is added can be obtained from (2) and the constitutive equation:

$$v_2 = -Z_L \cdot i_2 \quad (3)$$

yielding:

$$A_v(s) = \frac{h'_{21}(s)}{1 + \frac{h'_{22}(s)}{Z_L(s)}}$$
$$Z_o(s) = h'_{22}(s) \quad (4)$$

Equation (4) allows to obtain the hybrid-2 parameters h'_{21} and h'_{22} from the voltage gain, $A_v(s)$, and output impedance, $Z_o(s)$, for some known load conditions, and vice versa, obtain the voltage gain $A_v(s)$ and output impedance $Z_o(s)$ for some load from the hybrid-2 parameters h'_{21} and h'_{22} . Moreover, a particular case is that in which $Z_L \to \infty$. In this case, h'_{21} and h'_{22} are identical to $A_v(s)$ and $Z_o(s)$, respectively. This is the key to developing the POF generation and transformation methodology that is proposed in this paper to transform a POF for some known loading conditions to arbitrary new loading conditions.

Let us assume that we wish to generate the POF for the output impedance, dc voltage gain, unity-gain frequency, and phase margin for some arbitrary loading conditions. The generation methodology proceeds as follows:

1) Generate the POF of the performances of interest for some known loading conditions by using a multi-objective optimization algorithm with a nested electrical simulator as performance evaluator.

2) For each sample or individual of this POF, store pole and zero locations of the output impedance $Z_o(s)$ and the voltage gain $A_v(s)$, both being frequency dependent functions. This information can be retrieved from common electrical simulators. If this information is not available, a reduced two-pole model can be easily extracted from the dc gain, unity-gain frequency, and phase margin values.

3) Use equation (4) to extract the hybrid parameters $h'_{21}(s)$ and $h'_{22}(s)$ for each sample. Notice that, from basic circuit theory, the poles of $h'_{21}(s)$ and $h'_{22}(s)$ are identical.

4) Apply equation (4) to obtain the voltage gain for the new arbitrary loading conditions (new $Z_L(s)$) from the previously calculated hybrid parameters.

5) Obtain the performance parameters dc gain, unity-gain frequency, phase margin, and output impedance by simple processing of the network functions.

Notice that this procedure can be applied to any initial known loading conditions. This includes the case in which the POFs are generated for the circuit without any load. In this case, steps 2 and 3 are unified in a single step.

The first step of this methodology has the heaviest computational effort by far, but notice that the results of step 3 are independent of the application, i.e., independent of the final loading conditions. Therefore, the first three steps can be performed beforehand, and the results stored and used whenever and wherever necessary.

B. Results

In this section, the proposed methodology will be applied to the generation of the POF of the Miller operational amplifier, when a resistive-capacitive load is applied. Following step 1, a POF with a capacitive load of 1pF was first generated for the four objectives (see Section II): dc voltage gain, unity-gain frequency, phase margin, and output impedance.

From the electrical simulation of the 1500 points of the POF, the network functions $A_v(s)$ and $Z_o(s)$ of each design point can be easily obtained. And by applying equation (4) to each of these points, the hybrid-2 parameters h'_{21} and h'_{22} of the 1500 points are calculated. These two steps are performed in less than 5 minutes. Notice that all the steps performed so far are independent of the final load conditions. Therefore, although computationally costly, they are performed long before the load is known and the other steps have to be performed.

Assume that we need now to generate the POF for a load of 2pF and 50kΩ. Using the points previously stored, the new POF is generated by applying steps 4 and 5 in Section III. Figure 5 shows the three projections of the 4-dimensional front. The application of these two steps takes only 20 seconds.

To assess the procedure, the POF was also generated by coupling the optimizer with the electrical simulator for this new 2pF-50kΩ load (that is, not following the transformation procedure proposed here). A set of samples of the POF with similar quality characteristics is obtained (see Figure 6). However, as in the generation of the initial POF, 1 hour and 36 minutes of CPU are employed instead of the 20 seconds that were required by the transformation procedure described here. This is an acceptable time in order to incorporate this technique into a hierarchical synthesis flow where iterative evaluations of circuit performances are necessary. Notice that the POFs in Figures 5 and 6 are similar but the samples are different due to the finite population size and the stochastic nature of the multi-objective evolutionary algorithm. When comparing Figure 3 and Figure 5, it can be observed that the transformation procedure implies an important movement of points in the design objective space. Density of points in Figure 5 might

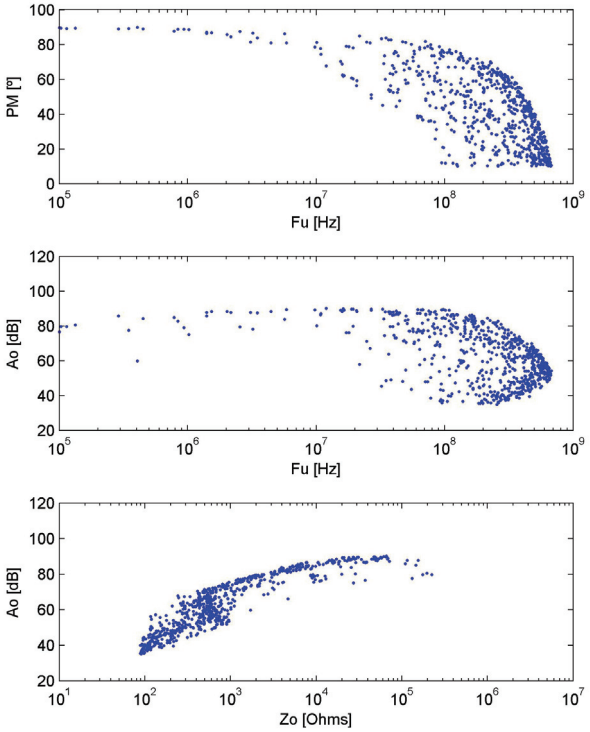

Figure 5. Projections of the POF obtained by the transformation procedure for a load of 2pF-50kΩ.

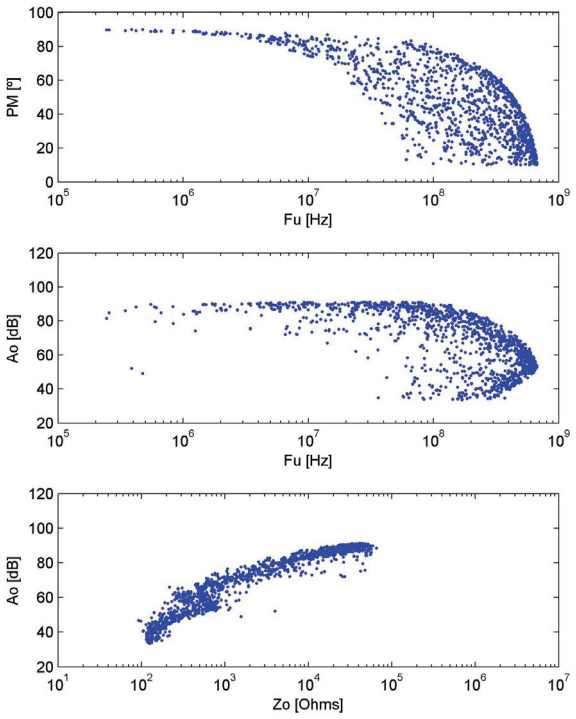

Figure 6. Projections of the POF generated by the multiobjective optimization algorithm for a load of 2pF-50KΩ.

become smaller because in the transformation some points may move to regions that are not of interest (for example, very low phase margin or dc gain), or because the transformation procedure can move a point to a position in the objective/performance space where it becomes dominated by other points. Although some points may become dominated after the transformation, the procedure guarantees that a point of the transformed POF may not originate from a dominated point of the initial performance space.

IV. CONCLUSIONS

This paper introduces a POF transformation procedure for operational amplifiers based on a hybrid-2 parameter characterization. This approach enables the efficient and rapid generation of POFs to arbitrary interconnection conditions, which can be used in hierarchical synthesis based on POFs. Future work will address the generation of denser transformed POFs by simultaneously considering the POFs generated for different load conditions.

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