Analysis and Modeling of the Non-Linear Sampling Process in Switched-Current Circuits - Application to Bandpass Sigma-Delta Modulators

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Abstract – **This paper presents a precise model for the transient behaviour of Fully Differential (FD) *SwItched-current* (SI) memory cells placed at the front-end of high-speed A/D interfaces. This model allows us to analyze the main errors associated to the S/H process, namely: excess transfer-function delay and harmonic distortion. For the latter, the analysis is extended to BandPass ΣΔ Modulators (BP-ΣΔMs) and a closed-form expression is derived for the third-order intermodulation distortion. Time-domain simulations and experimental measurements taken from a 0.8μm CMOS 4th-order BP-ΣΔM silicon prototype validate our approach.**

1. Introduction

Nowadays the market of digital communication devices is rapidly expanding with the development of new services and applications. This trend, together with the continuous scaling of digital CMOS technologies, has motivated exploring analog design techniques compatible with standard, VLSI processes. This is the case of *SwItched-current* (SI) circuits, which taking advantage of current processing, are suitable for fast operation with low-power consumption and low-voltage supplies [1].

Up to now, the potential of the SI technique has been barely demonstrated through actual, practical circuits. Thus, in the case of ΣΔ Modulators (ΣΔMs), performances featured by reported SI silicon prototypes are well below those of Switched-Capacitor (SC) counterparts, even if the latter are realized in standard technologies without good passive capacitors. Such poorer performances are partly due to the larger influence of SI non-idealities, as well as to the incomplete modeling of their influence. Particularly, for BandPass ΣΔMs (BP-ΣΔMs), and due to the necessity to cope with the frequency specifications required for modern digital wireless systems [2], Harmonic Distortion (HD) caused by non-linear dynamics becomes one of the dominant limiting factors.

Most attempts to model HD due to the non-linear transient assumed that the input signal is constant during the sampling phase[3][4]. However, this assumption does not apply to a memory cell placed at the front-end of BP-ΣΔMs. In this case, the input signal frequency is typically a quarter of the sampling frequency. Hence, large variations of the drain-source current will occur during the sampling phase, thus causing an additional HD which cannot be explained by an step-response.

The analysis of the HD of a SI memory cell with a continuous-time sinewave signal was analysed in [5]. In this paper, that analysis is extended to the case of BP-ΣΔMs. For this purpose, a precise model is described for a front-end Fully Differential (FD) memory cell. On the one hand, this model allows us to study the dominant non-idealities associated to the sampling process, namely: excess transfer-function delay and harmonic distortion. On the other hand, it enables hierarchical systematic analysis of SI circuits composed of memory cells, such as BP-ΣΔMs. As a result, a closed-form expression is derived for the third-order intermodulation distortion. It is demonstrated that large HD levels are obtained even for a low settling error, as confirmed by experimental measurements taken from a 0.8μm CMOS 4th-order BP-ΣΔM [6].

2. Modeling of front-end FD SI memory cells

Fig. 1(a) shows a FD second-generation memory cell. In what follows, it will be assumed that the error associated to the transient response is the dominant limitation. Therefore, the effect of the charge injection error, and the finite output conductance, analysed elsewhere [1][7], will not be considered. Besides, in most practical cases the time constant formed by the drain-source capacitance and the switch-on resistance is much smaller than that due to the gate-source capacitance, C_{gs}, and the small-signal transconductance, g_{mQ}. In such a case, the behaviour of the cell during the sampling phase, ϕ_1, can be modelled by the equivalent circuit in Fig.1(b). In this circuit, the large-signal behaviour is modelled by g_{m+} and g_{m-}, which represent the transconductances of $M_{+,-}$, given by $g_{m+,-} = g_{mQ}\sqrt{1+m_{i+,-}}$, where $m_{i+,-} = i_{i+,-}/I_{bias}$, $i_{i+,-} = \pm i_i/2$, and i_i is the input current [3].

Let us consider that i_i is a continuous-time sinewave of amplitude I_i and frequency $f_i \cong f_s/4$ ‡, with f_s being the sampling frequency. In this case, i_i will change during the sampling phase up to $I_i/\sqrt{2}$ ††, thus causing an additional error to that due to the incomplete settling error, which cannot be explained by analysing the step-response of the cell. For a better understanding of this phenomenon, we will consider first the linear analysis of Fig.1(b), with $g_{m+} = g_{m-} = g_{mQ}$ and $i_i(t) = I_i \sin(2\pi f_i t)$. Thus, solving v_g for the initial condition, $v_g(t_o)$, yields:

$$v_g(t) = \left[v_g(t_o) - \frac{i_i(t_o)}{g_{mQ}} F_{t_o}(f_i) \right] e^{\frac{-(t-t_o)}{\tau}} + \frac{i_i(t) F_t(f_i)}{g_{mQ}} \quad (1)$$

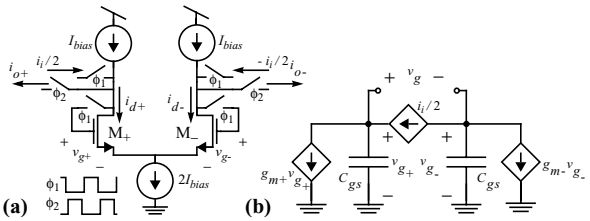

Figure 1. Fully differential memory cell. a) Schematic. b) Equivalent circuit during the sampling phase.

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‡.This is the typical case of a front-end memory cell in a BP-ΣΔM.

††.The maximum signal variation during the sampling phase is given by: $I_i\left|\sin[2\pi f_i(t+T_s/2)] - \sin[2\pi f_i t]\right|\Big|_{f_i = f_s/4} \le I_i/\sqrt{2}$.

where $F_t(f_i) = \dfrac{1-2\pi f_i\tau\cot(2\pi f_i t)}{1+(2\pi f_i\tau)^2}$, $\tau = C_{gs}/g_{mQ}$.
Assuming that the memory switch becomes OFF at $t_o = (n-1)T_s$ (T_s is the sampling period), it can be shown from (1) that the differential drain-source current at the end of the sampling phase, $i_{d,n-1/2} = g_{mQ}v_{g,n-1/2}$ ‡‡, is given by:

$$i_{d,n-1/2} = i_{i,n-1/2}F_{n-1/2}(f_i) + \\ +[i_{d,n-1} - i_{i,n-1}F_{n-1}(f_i)]\varepsilon_s \quad (2)$$

where $\varepsilon_s = \exp[-T_s/(2\tau)]$ is the incomplete settling error and $F_n(f_i) = F_{t=nT_s}(f_i)$.

During the hold phase, i_d keeps constant at the value reached at the end of the sampling phase and the cell delivers the output current, i_o. Thus, at the end of the hold phase nT_s, the output current is:

$$i_{o,n} = i_{o,n-1}\varepsilon_s - \\ -[i_{i,n-1/2}F_{n-1/2}(f_i) - i_{i,n-1}F_{n-1}(f_i)\varepsilon_s] \quad (3)$$

The above expression can be simplified for two particular cases. On the one hand, consider us the case of stationary ($f_iT_s \ll 1$) input signals, i.e, $i_{i,n-1/2} \cong i_{i,n-1}$. In this case, $f_i\tau \ll 1$ and $F_n(f_i) \to 1$. Making these approximations in (3), results in the well-known finite difference equation of a memory cell degraded by ε_s [1].

On the other hand, considering a negligible settling error, i.e, $\tau \ll T_s$, and taking into account that $i_{i,n} = I_i\sin(2\pi f_i nT_s)$, it can be shown from (3) that:

$$i_{o,n} \cong \frac{-I_i\sin[2\pi f_i(n-1/2)T_s - \operatorname{atan}(2\pi f_i\tau)]}{\sqrt{1+(2\pi f_i\tau)^2}} \quad (4)$$

meaning that the overall transfer function of the cell is:

$$\frac{i_o(f)}{i_i(f)} = \frac{-\exp[-j\pi f_iT_s - j\operatorname{atan}(2\pi f_i\tau)]}{\sqrt{1+(2\pi f_i\tau)^2}} \quad (5)$$

which can be seen as the cascade of two transfer functions: one of the Continuous-Time (CT) type, given by $H_{CT}(f) = 1/(1+j2\pi f\tau)$, and other one of the discrete-time type corresponding to the ideal transfer function of a memory cell, $-z^{-1/2}$. The former causes a transmission error which we will define as $\varepsilon_{CT} \equiv 2\pi f_i\tau$. This error can severely degrade the performance of the memory cell even for $\varepsilon_s \ll 1$ as will be shown in the next section.

In a more general case, i.e, for $\varepsilon_{CT} \neq 0$ and $\varepsilon_s \neq 0$, i_d will evolve in time during the sampling phase from the previous memorized value to the new stationary state input current, degraded by $H_{CT}(f)$. However, as a consequence of ε_s, that stationary state will not be reached at the end of the sampling phase, such that there will be an accumulation of two errors: ε_{CT} and ε_s. The latter has been analysed elsewhere [1][3][4]. Here, we will focus on studying the main effects of ε_{CT}.

2.1 Excess transfer-function phase delay

One of the main effects of ε_{CT} is to increase the phase delay between i_i and i_o. This is illustrated in Fig.2(a) by showing an electrical simulation (HSPICE) of the cell in Fig. 1(a) with $I_{bias} = 200\mu A$ and $\tau \cong 7.7ns$ assuming a CT input signal of $f_i \cong f_s/4$. This figure plots v_g as a function of i_i for three values of f_s. Comparing the resulting ellipses it can be concluded that the phase delay increases with f_s as a consequence of the increment of $f_i\tau$, i.e, ε_{CT}. This effect is predicted by the proposed model as Fig.2(b) illustrates. Besides, note that the ellipses become wider as ε_{CT} increases. This effect appears because f_i is not an exact submultiple of f_s – which is common in practice. Hence, since the number of sampling periods contained in an input period is not an integer, the sampled currents will vary from one input period to the next one.

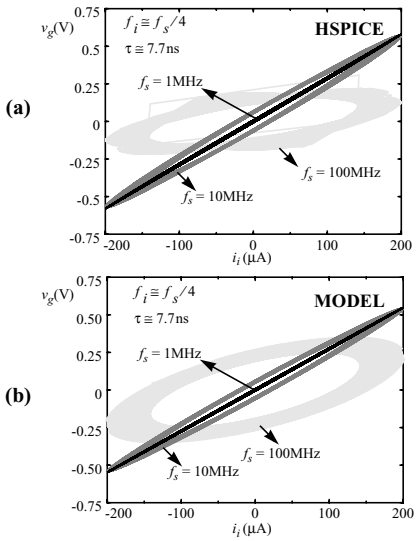

Figure 2. Excess transfer-function phase delay caused by ε_{CT} for a non-stationary input signal of $f_i \cong f_s/4$. a) HSPICE. b) Theoretical model.

Fig.3 illustrates the effect of changing f_i/f_s in memory cells with non-stationary input signals for $\tau = 7.7ns$ and $f_s = 10MHz$, ($\varepsilon_s \cong 0.15\%$). Observe that the phase delay becomes larger as a consequence of increasing $f_i\tau$, i.e, ε_{CT}, not due to ε_s (which is kept constant).

In the case of sampled-and-held input signals, the above-mentioned phenomenon appears but when ε_s is greatly increased. This is illustrated in Fig.4 for a FD memory cell with $I_{bias} = 200\mu A$, $f_i \cong f_s/4$ and $\tau = 3.7ns$. Note that the cell starts to behave as if it had a non-stationary input signal when the settling error becomes large ($f_s > 50MHz$), i.e, for $T_s \to \tau$, and the discrete-time approaches the continuous-time.

2.2 Harmonic distortion due to non-linear S/H

Another consequence of non-stationary input signals is the increase of the HD as compared to the case of stationary signals. This is illustrated in Fig.5 by comparing the

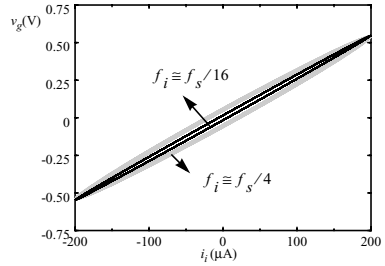

Figure 3. Effect of varying f_i on the transfer-function delay for $\tau = 7.7ns$ and $f_s = 10MHz$ ($\varepsilon_s \cong 0.15\%$).

‡‡.The notation $v_{g,n}$ is used to represent $v_g(nT_s)$.

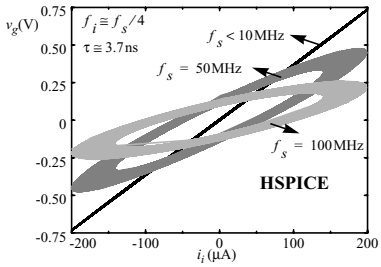

Figure 4. Excess transfer-function phase delay caused by ε_s for a sampled-and-held input signal of $f_i \cong f_s/4$.

simulated (HSPICE) output spectra of the cell in Fig.1(a) (with $I_{bias} = 100\mu A$, $I_i = I_{bias}/2$, $f_i = f_s/16$, $g_{mQ} = 268\mu A/V$, $C_{gs} = 1pF$ and $f_s = 1MHz$), corresponding to both a sampled-and-held and a continuous-time input tone. It is clear that the latter presents much more HD ($HD_3 = -89dB$) than the former ($HD_3 = -127dB$). However, in both cases the settling error is negligible ($\tau = 3.7ns$ and $T_s = 1\mu s$), meaning that the extra HD is caused by the non-linear sampling process. This phenomenon can be analysed by solving the non-linear circuit shown in Fig.1(b) for an sinewave input. A rigorous study will require using the Volterra series method as we demonstrated in [7]. However this method involves a tedious mathematical analysis and is difficult to extend to other SI circuits of higher hierarchy such as ΣΔMs. Instead, we can find a similar solution – but involving a more simple analysis – by replacing g_{mQ} in (3) with $g_{m+,-}$. Making this respectively in each branch of the FD cell, the output current can be approximated by:

$$i_{o,n} \cong -i_{i,n-1/2}\varphi_{n-1/2}(m_{i,n-1/2}) + \\ + [i_{i,n-1}\varphi_{n-1}(m_{i,n-1/2}) + i_{o,n-1}]\Psi(m_{i,n-1/2}) \quad (6)$$

where $\varphi_n(m_i) =$

$$= \frac{\frac{1}{2} - \pi f_i \tau \frac{\cot(2\pi f_i n T_s)}{\sqrt{1+m_i}}}{1 + \frac{(2\pi f_i \tau)^2}{1+m_i}} + \frac{\frac{1}{2} - \pi f_i \tau \frac{\cot(2\pi f_i n T_s)}{\sqrt{1-m_i}}}{1 + \frac{(2\pi f_i \tau)^2}{1-m_i}} \quad (7)$$

and $\Psi(m_i) =$

$$= \frac{1}{2}\left(\exp\left[\frac{-T_s}{2\tau}\sqrt{1+m_i}\right] + \exp\left[\frac{-T_s}{2\tau}\sqrt{1-m_i}\right]\right) \quad (8)$$

To obtain a closed-form expression of HD_3, we have performed a Taylor series expansion of (7) and (8) for $m_i \ll 1$, giving:

$$\varphi_n(i_i) \cong \xi_1 + \xi_2 i_i^2 \qquad \Psi(i_i) \cong \varepsilon_s + \varepsilon_{s2} i_i^2 \quad (9)$$

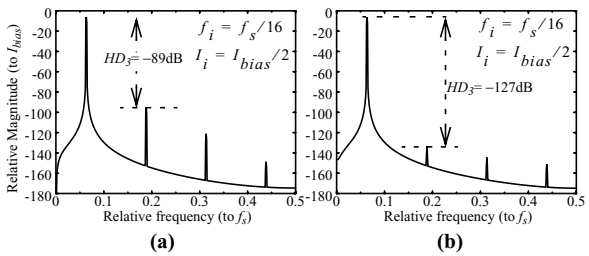

Figure 5. Output spectra of a FD memory cell with a (a) non-stationary and (b) stationary input tone of $f_i = f_s/16$.

where $\xi_1 = [1 - 2\pi f_i \tau \cot(2\pi f_i n T_s)]/(1 + (2\pi f_i \tau)^2)$

$$\xi_2 = -6\pi f_i \tau \cot(2\pi f_i n T_s)/(32 I_{bias}^2)$$

and $\varepsilon_{s2} = \varepsilon_s[T_s/(2\tau)][1 + T_s/(2\tau)]/(32 I_{bias}^2)$.
Substituting (9) into (6), it can be shown that the non-linear term appearing at the output of the cell is:

$$i_{NL,n} \cong i_{i,n-1/2}^2[(\xi_2\varepsilon_s + \xi_1\varepsilon_{s2})i_{i,n-1} + \varepsilon_{s2} i_{o,n-1}] - \\ -\xi_2 i_{i,n-1/2}^3 \quad (10)$$

Approximating i_o by its first-order harmonic and performing a Fourier series expansion of (10) it can be derived that the amplitude of the third-order harmonic is:

$$A_{3H} \cong \frac{(3 - 3\varepsilon_s - 32\varepsilon_{s2} I_{bias}^2)\pi f_i \tau}{64 I_{bias}^2} I_i^3 \cong \frac{3\pi f_i \tau I_i^3}{64 I_{bias}^2} \quad (11)$$

which agrees with HSPICE simulations as illustrated in Fig.6 by representing HD_3 ($\equiv A_{3H}/I_i$) vs. f_i/f_s for $I_{bias} = 100\mu A$, $g_{mQ} = 268\mu A/V$, $C_{gs} = 1pF$, $I_i = I_{bias}/2$, and different values of f_s.

It is important to mention that the model described here is valid not only for analysing the HD of a single memory cell as in [5], but also to perform precise time-domain behavioural simulations of any FD SI circuit based on memory cells [7][8]. We will take advantage of this fact to obtain the effect of non-linear ε_{CT} on the HD of BP-ΣΔMs.

3. Harmonic distortion of FD SI BP-ΣΔMs

Fig.7(a) shows the block diagram of the 4th-order BP-ΣΔM under study, with $A_{DAC2} = 2A_{DAC1}A_{RES}$, which has been obtained by applying a $z^{-1} \rightarrow -z^{-2}$ to a 2nd-order lowpass ΣΔM [2]. Because of this transformation, the original integrators become resonators with a transfer function $z^{-a}/(1 + z^{-2})$, where $0 < a \le 2$. This function can be realized by several filter structures [2]. The resonators of Fig.7(a) are based on LD Integrators (LDI's), which can be realized using FD SI memory cells as shown in Fig.7(b). This structure is advantageous as compared to the others because it remains stable under changes in the loop coefficients [7]. For the analysis of the HD caused by non-linear ε_{CT}, the following considerations have been taken into account:

- The HD referred to the modulator input is equal to the HD referred to the modulator output because the signal transfer function ($Y(z)/X(z)$) is unity in the signal band.
- The quantization error, modelled as an additive white noise source [2], does not contribute to HD.
- For $\varepsilon_s \ll 1$, the HD will be dominated by the non-linear ε_{CT} of the cell connected at the input node (see Fig.7(b)).

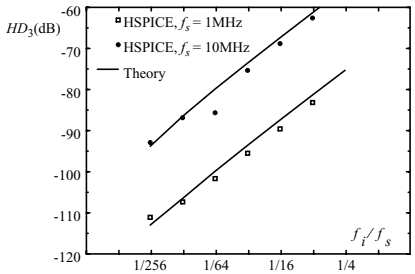

Figure 6. HD_3 vs. f_i/f_s due to non-linear ε_{CT}.

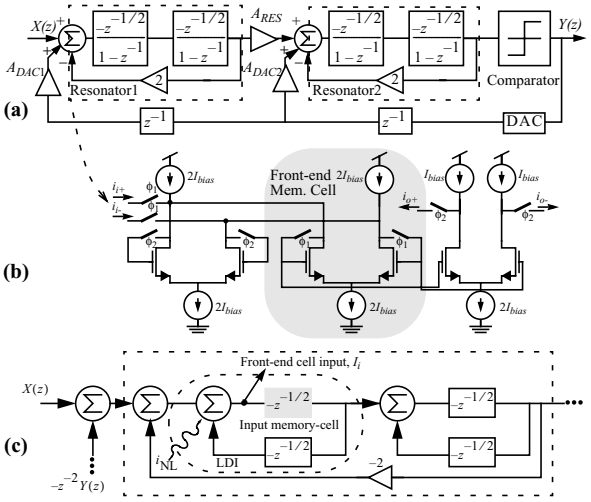

Figure 7. Fourth-order BP-ΣΔM. a) Block diagram. b) FD SI LDI-loop resonator. c) Block diagram for obtaining I_i.

Taking into account the above considerations, to calculate the third-order harmonic at the output of the modulator it is necessary to express I_i as a function of the modulator input amplitude, $|X| = A_x$. The analysis of Fig.7(c) gives:

$$I_i \cong A_x \left|(1-z^{-1})^2(1+z^{-1})\right|_{z=e^{j2\pi f_i T_s}} \cong 2\sqrt{2}A_x \qquad (12)$$

where $f_i \cong f_s/4$ has been assumed.

Substituting (12) into (11) and dividing by A_x it can be shown that the third-order intermodulation distortion, IM_3 †††, at the output of the BP-ΣΔM is:

$$IM_3 \cong \frac{9}{8\sqrt{2}n_b^2}\pi f_s \tau \left(\frac{A_x}{I_{DAC}}\right)^2 \qquad (13)$$

where $n_b = I_{bias}/I_{DAC}$, and I_{DAC} is the DAC output current.

This analysis has been validated by time-domain simulation using the behavioural simulator for SI circuits reported in [8]. Fig.8(a) compares (13) with simulations by plotting IM_3 vs. τ for different values of f_s, $n_b = 4$ and $A_x/I_{DAC} = 1/2$. The theoretical model accurately predicts the simulation results except for some cases where a maximum error of 4dB occurs. In these cases a more exact analysis using the Volterra series method should be used.

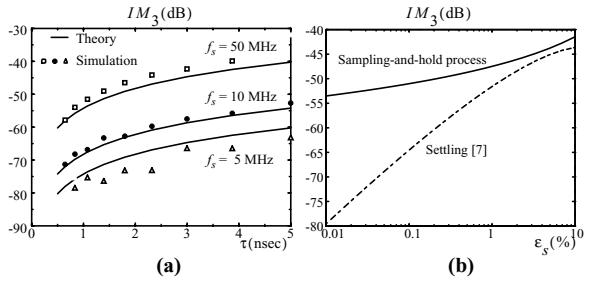

Figure 8. IM_3 due to the non-linear sampling. a) IM_3 vs. τ. b) Comparison with IM_3 due to non-linear ε_s [7].

†††. $IM_s \equiv 3HD_3$ is a more appropriate parameter for characterizing HD in BP-ΣΔMs.

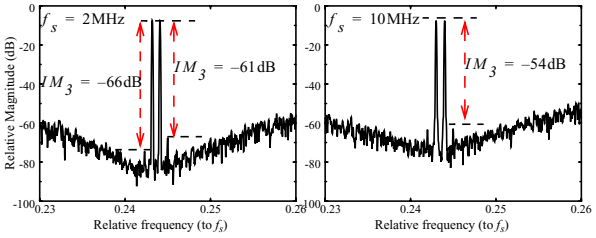

Figure 9. Experimental output spectra for different f_s.

To conclude this study, Fig.8(b) compares IM_3 caused by the non-linear ε_s [7] and ε_{CT} for $f_s = 10$MHz and $A_x/I_{DAC} = 1/2$. Note that, for $\varepsilon_s > 3\%$, both expressions approximately converge. However, for practical designs, i.e, for $\varepsilon_s < 0.1\%$, IM_3 due to ε_{CT} dominates, limiting the performance of SI BP-ΣΔMs unless a front-end S/H circuit will be used. This fact has been confirmed by experimental results from a 0.8μm CMOS 4th-order BP-ΣΔM [6]. Fig.9 shows two measured output spectra for $A_x/I_{DAC} = 0.42$ when clocked at $f_s = 2$MHz and $f_s = 10$MHz, obtaining $IM_3 = -61$dB and -54dB respectively. In this case, $g_{mQ} = 360\mu$A/V and $C_{gs} = 2.8$pF ($\varepsilon_s = 0.16\%$ at $f_s = 10$MHz), which according to (13) gives $IM_3 = -64$dB and $IM_3 = -55$dB respectively.

4. Conclusions

The effect of non-linear S/H process on SI circuits has been studied in detail. A model for FD memory cells placed at the front-end of A/D interfaces has been described. The analysis, validated by HSPICE, explains the main errors associated to the non-linear S/H, namely: excess phase delay and HD. For the latter, a closed-form expression has been derived for IM_3 at the output of BP-ΣΔMs, which as confirmed by experimental results, constitutes the main source of HD in practical designs.

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