Study of Non-Linear S/H Operation in Switched-Current Circuits using Volterra Series – Application to Bandpass ΣΔ Modulators

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Abstract

This paper analyses the transient behaviour of *SwItched-current* (SI) memory cells placed at the front-end of high-speed A/D interfaces. Based on the Volterra series method, the non-linear sampling process occurring in such cells is studied and closed-form expressions are obtained for the Total Harmonic Distortion (THD) and the intermodulation distortion. The analysis is extended to the case of BandPass ΣΔ Modulators (BP-ΣΔMs) using Fully-Differential (FD) SI memory cells. As a result, the third-order intermodulation distortion at the output of the modulator is derived. Time-domain simulations and experimental measurements taken from a 0.8μm CMOS 4th-order BP-ΣΔM silicon prototype validate the study.

1. Introduction

Nowadays the market of digital communication devices is rapidly expanding with the development of new services and applications. This trend, together with the continuous scaling of digital CMOS technologies, has motivated exploring analog design techniques compatible with standard, VLSI processes. This is the case of *SwItched-current* (SI) circuits, which taking advantage of current processing, are suitable for fast operation with low-power consumption and low-voltage supplies [1].

Up to now, the potential of the SI technique has been barely demonstrated through actual, practical circuits. Thus, in the case of ΣΔ Modulators (ΣΔMs), performances featured by reported SI silicon prototypes are well below those of Switched-Capacitor (SC) counterparts, even if the latter are realized in standard technologies without good passive capacitors. Such poorer performances are partly due to the larger influence of SI non-idealities, as well as to the incomplete modeling of their influence. Particularly, for BandPass ΣΔMs (BP-ΣΔMs), and due to the necessity to cope with the frequency specifications required for modern digital wireless systems [2], Harmonic Distortion (HD) caused by non-linear dynamics becomes one of the dominant limiting factors.

Most attempts to model HD due to the non-linear transient assumed that the input signal is constant during the sampling phase[3][4]. However, this assumption does not apply to a memory cell placed at the front-end of BP-ΣΔMs. In this case, the input signal frequency is typically a quarter of the sampling frequency. Hence, large variations of the drain-source current will occur during the sampling phase, thus causing additional HD which cannot be explained by evaluating the step-response. Based on some simplifications, the HD of a SI memory cell with a continuous-time sinewave was obtained in [5].

In this paper, the study of this phenomenon is extended to the case of Fully-Differential (FD) SI BP-ΣΔMs. For that purpose, a rigorous analysis –based on the Volterra series method [6]– is carried out at the memory cell level. On the one hand, this approach allows us to predict the HD of front-end memory cells considering all cases regarding the input signal frequency and the memory-cell bandwidth. On the other hand, it enables hierarchical systematic analysis of SI circuits composed of memory cells, such as BP-ΣΔMs. As a result, a closed-form expression is derived for the third-order intermodulation distortion (IM_3) at the output of the modulator. It is demonstrated that large IM_3 levels are obtained even for a low settling error, as confirmed by experimental measurements taken from a 0.8μm CMOS 4th-order BP-ΣΔM silicon prototype [7].

2. Extra HD due to non-linear S/H process

Fig.1 shows the single-ended (Fig.1(a)) and the FD (Fig.1(b)) versions of a second-generation simple memory cell. In what follows, it will be assumed that the error associated to the transient response is the dominant limitation. Therefore, the effect of the charge injection error and the finite output conductance, analysed elsewhere [1], will not be considered.

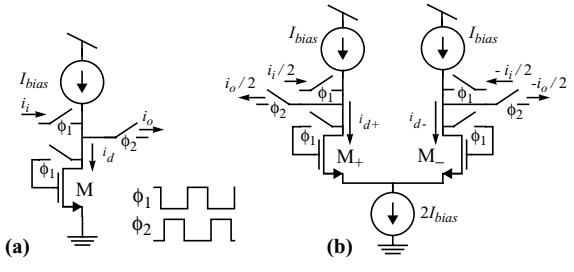

Fig. 1: Second-generation simple memory cell: (a) Single-ended version. (b) Fully-differential version.

Besides, in most practical cases the time constant formed by the drain-source capacitance and the switch-on resistance is much smaller than that due to the gate-source capacitance, C_{gs}, and the small-signal transconductance, g_m, of the memory transistor – M in Fig.1(a) and $M_{+,-}$ in Fig.1(b). In such a case, the small-signal transient response during the sampling phase, ϕ_1, will be governed by the time constant $\tau = C_{gs}/g_m$. Thus, if the input signal, i_i, remains stationary during ϕ_1, the transient response of the circuit in Fig.1 can be analysed as a step response. If the charge of C_{gs} is not completed at the end of the sampling phase, ϕ_1, an error occurs, called incomplete settling, $\varepsilon_s \equiv \exp[-T_s/(2\tau)]$, with T_s being the sampling period [1]. In addition to that linear error, ε_s, the signal-dependent step response leads to harmonic distortion as demonstrated in [3][4].

Let us consider that i_i is a continuous-time sinewave of amplitude I_i and frequency $f_i \cong f_s/4^{\dagger}$, where $f_s = 1/T_s$ is the sampling frequency. Fig.2 shows the transient evolution of the drain current, i_d ($i_d \equiv i_{d+} - i_{d-}$ for the FD cell). Observe that, in this case, i_i will change during the sampling phase up to $I_i/\sqrt{2}^{\dagger\dagger}$, thus causing an additional error to that due to the incomplete settling error. This additional error, dominantly non-linear, will cause extra HD which cannot be explained by analysing the step-response of the cell, i.e, considering stationary input signals during the sampling phase.

Fig.3 illustrates the increase of HD due to non-stationary input signals by comparing the simulated (HSPICE) output spectra of the FD cell in Fig.1(b) (with $I_{bias} = 100\mu A$, $I_i = I_{bias}/2$, $f_i = f_s/16$, $g_m = 268\mu A/V$, $C_{gs} = 1pF$ and $f_s = 1MHz$), corresponding to both a sampled-and-held (stationary) and a continuous-time (nonstationary) input tone. It is clear that the latter presents much more HD ($HD_3 = -89dB$) than the former $HD_3 =$ ($= -127dB$). However, in both cases the settling error

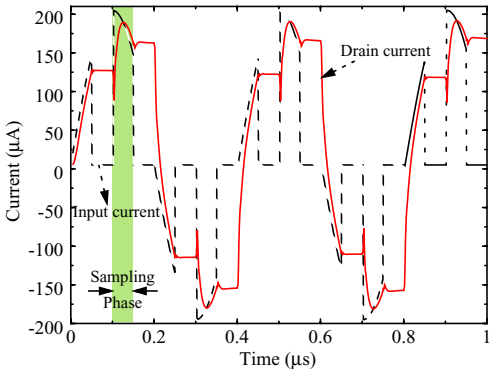

Fig. 2: Transient evolution of i_d for an input sinewave with $I_i = I_{bias}/2$, and $f_s = 10MHz$.

†. This is the typical case of a front-end cell in a BP-ΣΔM.

††. The maximum signal variation during sampling phase is given by: $I_i\left|\sin[2\pi f_i(t+T_s/2)] - \sin[2\pi f_i t]\right|_{f_i = f_s/4} \le I_i/\sqrt{2}$.

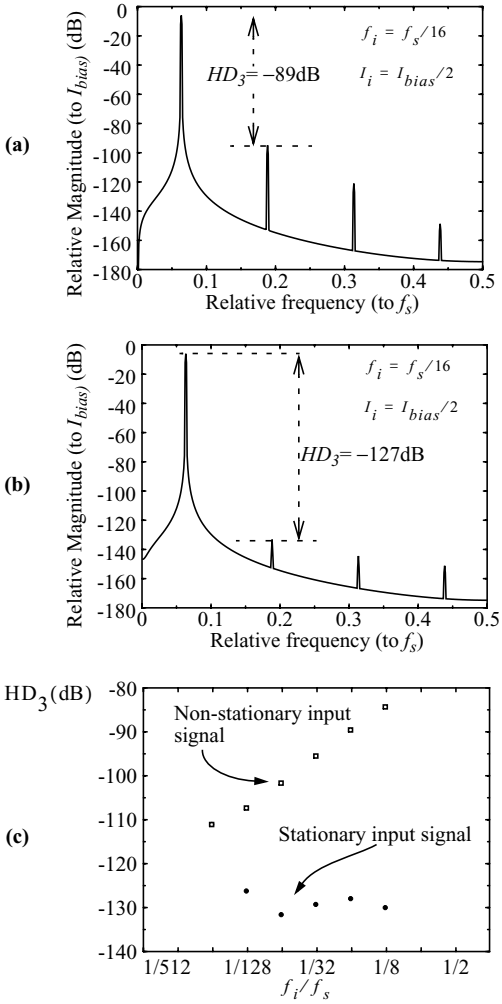

Fig. 3: Extra HD caused by the non-linear sampling. Output spectra (HSPICE) of a FD memory cell with a (a) non-stationary and (b) stationary input tone of $f_i = f_s/16$. (c) HD_3 vs. f_i/f_s.

is negligible ($\tau = 3.7ns$, and $T_s \equiv 1/f_s = 1\mu s$), meaning that the extra HD is caused by the non-linear sampling process. As illustrated in Fig.3(c), HD due to the non-linear sampling becomes lower as f_i/f_s is reduced, i.e, as the signal is more stationary during the sampling phase. This phenomenon can be analysed by using the Volterra series method [6] to solve the non-linear transient response of the cell of Fig.1 with an sinewave input signal.

3. Analysis of THD using Volterra series

A.Review of Volterra series

As well known, the output signal, $y(t)$, of a Linear Time-Invariant (LTI) system can be represented by:

$$y(t) = \int_{-\infty}^{\infty} h(t-\tau)x(\tau)d\tau \qquad (1)$$

where $h(t)$ is the impulsive response of the system and $x(t)$ is the input signal. Using fasorial analysis, the above expression can be expressed as:

$$Y(j\omega t) = H(j\omega)X(j\omega t) \tag{2}$$

where $H(j\omega)$ is the Fourier transform of $h(t)$ and $X(j\omega t) = \rho e^{j\omega t}$, is a *fasor* of amplitude ρ and angular frequency $\omega = 2\pi f$.

In the more general case, and under some general continuity conditions, a non-linear time-invariant system can be expanded into a series of the type [6],

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} h_1(t-\tau_1)x(\tau_1)d\tau_1 + \\ &+ \int_{-\infty}^{\infty}\int h_2(t-\tau_1, t-\tau_2)x(\tau_1)x(\tau_2)d\tau_1 d\tau_2 + \\ &+ \ldots + \\ &+ \int\int\ldots\int_{-\infty}^{\infty} h_n(t-\tau_1\ldots, t-\tau_n)x(\tau_1)\ldots x(\tau_n)d\tau_1\ldots d\tau_n \end{aligned} \tag{3}$$

which is called the *Volterra* series. In (3), the term $h_n(t)$, usually named nth-order Volterra kernel, plays an analogous role to that of $h(t)$ in LTI systems, but assuming that their currents and voltages are nth-order signals. It can be shown that it is possible to form a series of nth-order equivalent circuits, to solve each one by conventional linear analysis, and to combine their individual responses to form a total solution [6].

Expanding a non-linear system in Volterra series is useful for finding its frequency response and hence its sinusoidal response, which is directly related to harmonic distortion. For this purpose, it is more convenient to use the fasorial analysis in the same way as in linear systems. Thus, assuming that the input signal is a fasor, $x(t) = X(j\omega t)$, the output signal will be given by:

$$\begin{aligned} Y(j\omega_1, j\omega_2, \ldots, j\omega_n, t) &= H_1(j\omega_1)X(j\omega_1 t) + \\ &+ H_2(j\omega_1, j\omega_2)X(j\omega_1 t)X(j\omega_2 t) + \\ &+ \ldots + \\ &+ H_n(j\omega_1, \ldots, j\omega_n)X(j\omega_1 t)\ldots X(j\omega_n t) \end{aligned} \tag{4}$$

where

$$\begin{aligned} &H_n(j\omega_1, \ldots, j\omega_n) = \\ &= \int\int\ldots\int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n)e^{-j(\omega_1\tau_1 + \ldots + \omega_n\tau_n)}d\tau_1\ldots d\tau_n \end{aligned} \tag{5}$$

represents the nth-dimensional Fourier transform of the nth-order Volterra kernel. It can be shown that the nth-order harmonic distortion coefficients, HD_n, are related to the functions H_n as [8]:

$$\begin{aligned} HD_2(\omega) &= \frac{\rho}{2}\frac{H_2(j\omega, j\omega)}{H_1(j\omega)} \\ HD_3(\omega) &= \frac{\rho^2}{4}\frac{H_3(j\omega, j\omega, j\omega)}{H_1(j\omega)} \end{aligned} \tag{6}$$

Assuming two sinusoidal input signals of the same amplitude, ρ, and angular frequencies, ω_a and ω_b, the nth-order intermodulation distortion coefficients, IM_n, are given by:

$$\begin{aligned} IM_2(\omega_a \pm \omega_b) &= \rho\frac{H_2(j\omega_a, \pm j\omega_b)}{H_1(j\omega_a)} \\ IM_3(2\omega_a \pm \omega_b) &= \frac{3\rho^2}{4}\frac{H_3(j\omega_a, j\omega_a, \pm j\omega_b)}{H_1(j\omega_a)} \end{aligned} \tag{7}$$

Therefore, the obtainment of H_n is the key in calculating harmonic and intermodulation distortion coefficients of non-linear dynamic systems. In the next section this method will be applied to obtain the THD of an SI memory cell with a continuous-time sinewave.

B.Application to SI memory cells

Let us consider the simple SI memory cell shown in Fig.1(a). For the analysis that follows, these approximations will be considered:

- The transient response corresponds to a first-order dynamics, dominated by τ.
- The charge injection error and the finite output resistance will be neglected.
- Memory transistor, M, operates in the saturation region and can be modelled by:

$$i_d = \frac{\beta}{2}(v_{gs} - V_T)^2 \tag{8}$$

where $\beta = \mu_o C_{ox} W/L$.

Under the above-mentioned conditions, the equivalent circuit of the cell in Fig.1(a) is shown in Fig.4(a). Note that, this circuit can be viewed as the cascaded connection of two circuits as illustrated in Fig.4(b): one of them consists of the equivalent circuit of a simple current mirror and the other one is an ideal S/H circuit.

Except for the half clock period delay, the analysis of Fig. 4(b) during the sampling phase gives all information needed to analyse the non-linear transient behaviour of the cell and hence, to get a closed-form expression of the harmonic distortion. Therefore, in what follows, we will consider for our analysis the circuit in Fig. 4(b) during ϕ_1.

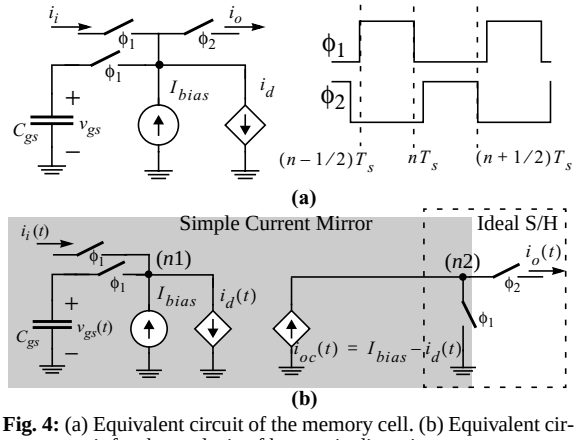

Fig. 4: (a) Equivalent circuit of the memory cell. (b) Equivalent circuit for the analysis of harmonic distortion.

By applying Kirchoff's current law to node *n*1 (see Fig.4(b)), we obtain:

$$i_i(t) + I_{bias} = i_d(t) + C_{gs}\frac{d}{dt}v_{gs}(t) \qquad (9)$$

By making the gate-source voltage, $v_{gs}(t)$, equal to a quiescent voltage, V_{gs}, plus an incremental voltage, $v(t)$, i.e, $v_{gs} = V_{gs} + v(t)$, (9) simplifies into:

$$i_i(t) = g_m v(t) + \frac{\beta}{2}v^2(t) + C_{gs}\frac{d}{dt}v(t) \qquad (10)$$

where $g_m = 2I_{bias}/(V_{gs} - V_T)$ and $I_{bias} = \beta(V_{gs} - V_T)^2/2$ has been considered.

The incremental voltage, $v(t)$, can be expressed in its Volterra series as:

$$v(t) = v_1(t) + v_2(t) + v_3(t) + \ldots + v_n(t) \qquad (11)$$

where $v_n(t)$ stands for the *n*th-order term of $v(t)$.

Substituting (11) into (10) and keeping only the most significant terms, it can be obtained that the differential equations corresponding to the first, second and third-order kernels are, respectively:

$$\begin{aligned} i_i(t) &= g_m v_1(t) + C_{gs}\frac{d}{dt}v_1(t) \\ 0 &= g_m v_2(t) + C_{gs}\frac{d}{dt}v_2(t) + \frac{\beta}{2}v_1^2(t) \\ 0 &= g_m v_3(t) + C_{gs}\frac{d}{dt}v_3(t) + \beta v_1(t)v_2(t) \end{aligned} \qquad (12)$$

Performing the same analysis for node *n*2 yields:

$$\begin{aligned} i_{oc1}(t) &= -g_m v_1(t) \\ i_{oc2}(t) &= -g_m v_2(t) - \frac{\beta}{2}v_1^2(t) \\ i_{oc3}(t) &= -g_m v_3(t) - \beta v_1(t)v_2(t) \end{aligned} \qquad (13)$$

where $i_{ocn}(t)$, represents the *n*th-order term of the Volterra series expansion of $i_{oc}(t)$.

Using fasorial analysis and solving for $I_{oc1}(j\omega_1 t)$, $I_{oc2}(j\omega_1, j\omega_2, t)$ and $I_{oc3}(j\omega_1, j\omega_2, j\omega_3, t)$ in the above expressions yields:

$$H_1(j\omega_1) \equiv \frac{I_{oc1}(j\omega_1 t)}{I_i(j\omega_1 t)} = \frac{-1}{1 + j\phi_1} \qquad (14)$$

$$\begin{aligned} H_2(j\omega_1, j\omega_2) &\equiv \frac{I_{oc2}(j\omega_1, j\omega_2, t)}{I_i^2(j\omega_1 t)} = \\ &= \frac{-j(\phi_1 + \phi_2)}{4I_{bias}(1 + j\phi_1)(1 + j\phi_2)[1 + j(\phi_1 + \phi_2)]} \end{aligned} \qquad (15)$$

$$\begin{aligned} H_3(j\omega_1, j\omega_2, j\omega_3) &\equiv \frac{I_{oc3}(j\omega_1, j\omega_2, j\omega_3, t)}{I_i^3(j\omega_1 t)} = \\ &= \frac{j(\phi_1 + \phi_2 + \phi_3)/\left(24I_{bias}^2\right)}{(1 + j\phi_1)(1 + j\phi_2)(1 + j\phi_3)[1 + j(\phi_1 + \phi_2 + \phi_3)]} \cdot \\ &\cdot \left[\frac{1}{1 + j(\phi_1 + \phi_2)} + \frac{1}{1 + j(\phi_1 + \phi_3)} + \frac{1}{1 + j(\phi_2 + \phi_3)}\right] \end{aligned} \qquad (16)$$

where $\phi_n \equiv \omega_n \tau$.

Substituting (14)-(16) into (6) and (7), closed-form expressions can be obtained for THD and the inter-modulation distortion, respectively. In this paper, we are mainly interested in the analysis of FD SI circuits. Thus, even-order harmonic coefficients can be neglected and hence, $\text{THD} \cong HD_3$ is given by:

$$HD_3(\omega) = \frac{-3j\omega\tau M_i^2}{32(1 + j\omega\tau)^2(1 + 2j\omega\tau)(1 + 3j\omega\tau)} \qquad (17)$$

where $M_i = I_i/(2I_{bias})$ for a FD SI memory cell, with I_i being the input signal amplitude.

Assuming $\omega_1 \cong \omega_2 \cong \omega_3 \cong \omega$ in (16), and $\omega\tau \ll 1$, expression (17) simplifies into:

$$HD_3(\omega) \cong \frac{-3}{32}j\omega\tau M_i^2 \qquad (18)$$

and the third-order intermodulation distortion can be obtained from (7) and (16), giving for $\omega\tau \ll 1$:

$$IM_3(\omega) \cong \frac{-9}{32}j\omega\tau M_i^2 = 3HD_3(\omega) \qquad (19)$$

The above results have been validated by electrical simulations using HSPICE with level-47 MOS models. Fig.5 represents HD_3 vs. f_i/f_s for a FD memory cell like that shown in Fig.1(b) with $I_{bias} = 100\mu\text{A}$, $g_m = 268\mu\text{A/V}$, $C_{gs} = 1\text{pF}$, $I_i = I_{bias}/2$, and different values of f_s. Observe that, for $f_s = 1\text{MHz}$, the settling error is negligible, $\varepsilon_s \cong 6 \cdot 10^{-59}$. However, there are high levels of harmonic distortion, $HD_3 \in (-95, -60)\text{dB}$.

The effect of τ on the harmonic distortion can be better appreciated in Fig.6 by displaying HD_3 as a function of g_m for $f_s = 10\text{MHz}$, $C_{gs} = 0.5\text{pF}$, $I_{bias} = 200\mu\text{A}$, $I_i = I_{bias}/2$ and different values of the input signal frequency. In this case, simulations were carried out by using the precise time-domain SI behavioural simulator described in [9]. Note from Fig.6 that HD_3 is reduced as g_m is increased and/or f_i is reduced, i.e, as $f_i\tau$ is decreased.

It is important to mention that the model described here is valid not only for analysing the HD of a single memory cell as in [5], but also to perform precise time-domain behavioural simulations of any FD SI cir-

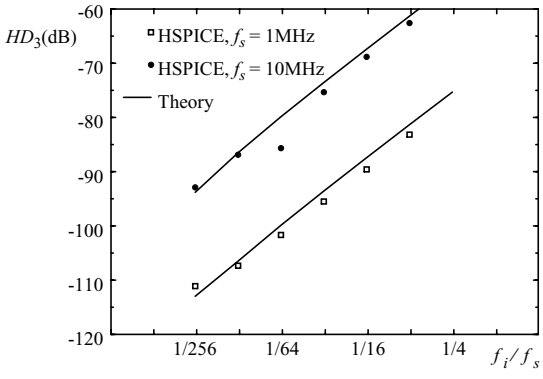

Fig. 5: HD_3 vs. f_i/f_s due to non-linear sampling.

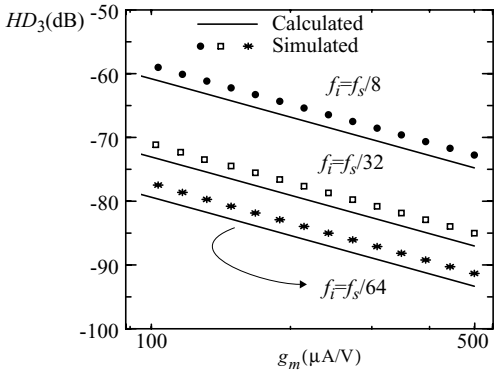

Fig. 6: HD_3 vs. g_m due to non-linear sampling.

cuit based on memory cells [9][10]. We will take advantage of this fact to obtain the effect of non-linear S/H on the intermodulation distortion of BP-ΣΔMs.

4. Harmonic distortion of FD SI BP-ΣΔMs

Fig.7(a) shows the block diagram of the 4th-order BP-ΣΔM under study, with $A_{DAC2} = 2A_{DAC1}A_{RES}$, which has been obtained by applying a $z^{-1} \rightarrow -z^{-2}$ to a 2nd-order lowpass ΣΔM [2]. Because of this transformation, the original integrators become resonators with a transfer function $z^{-a}/(1+z^{-2})$, where $0 < a \leq 2$. This function can be realized by several filter structures [2]. The resonators of Fig.7(a) are based on LD Integrators (LDIs), which can be realized using FD SI memory cells as shown in Fig.7(b). This structure is advantageous as compared to the others because

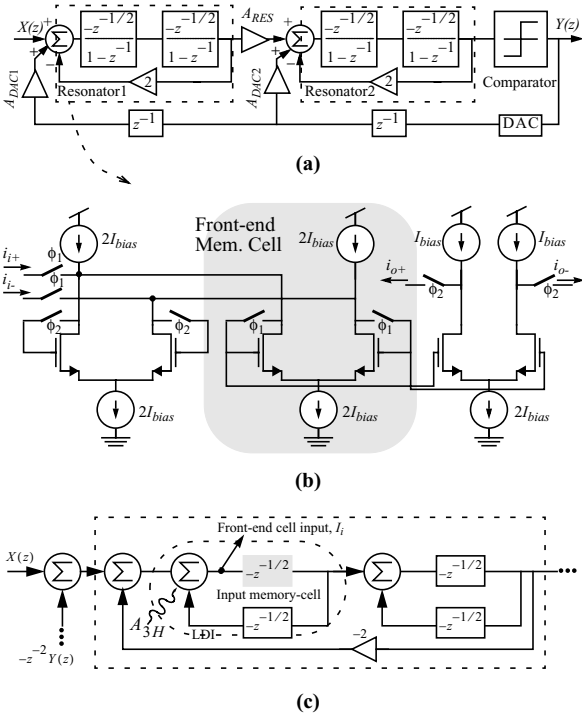

Fig. 7: Fourth-order BP-ΣΔM. a) Block diagram. b) FD SI LDI-loop resonator. c) Block diagram for obtaining I_i.

it remains stable under changes in the loop coefficients [10]. For the analysis of HD caused by the non-linear sampling, the following considerations have been taken into account:

- HD referred to the modulator input is equal to HD referred to the modulator output because the signal transfer function ($Y(z)/X(z)$) is unity in the signal band.
- The quantization error, modelled as an additive white noise source [2], does not contribute to HD.
- For $\varepsilon_s \ll 1$, HD will be dominated by the non-linear sampling of the cell connected at the input node (see Fig.7(b)). According to (17), this cell can be modelled as an ideal cell with an input signal having a third-order harmonic of amplitude:

$$A_{3H} \cong \frac{3\pi f_i \tau I_i^3}{64 I_{bias}^2} \tag{20}$$

Taking into account the above considerations, to calculate the third-order harmonic at the output of the modulator it is necessary to express I_i as a function of the modulator input amplitude, $|X| = A_x$. The analysis of Fig.7(c) gives:

$$I_i \cong A_x \left|(1-z^{-1})^2(1+z^{-1})\right|_{z=e^{j2\pi f_i T_s}} \cong 2\sqrt{2}A_x \tag{21}$$

where $f_i \cong f_s/4$ has been assumed.

From (19)-(21) it can be shown that the third-order intermodulation distortion at the output of the BP-ΣΔM is:

$$|IM_3| \cong \frac{9}{8\sqrt{2}n_b^2}\pi f_s \tau \left(\frac{A_x}{I_{DAC}}\right)^2 \tag{22}$$

where $n_b = I_{bias}/I_{DAC}$, and I_{DAC} is the DAC output current.

This analysis has been validated by time-domain simulation using the SI behavioural simulator reported in [9]. Fig.8(a) compares (22) with simulations by plotting $|IM_3|$ vs. τ for different values of f_s, $n_b = 4$ and $A_x/I_{DAC} = 1/2$. The theoretical model accurately predicts the simulation results except for some cases where a maximum error of 4dB occurs. In these cases, the exact expression in (16) should be considered for the analysis of the distortion in the modulator. However, the resulting expressions are, mathematically speaking, too complex, being better to resort to simulation results from the point of view of the circuit designer.

To conclude this study, Fig.8(b) compares IM_3 caused by the non-linear ε_s [10] and sampling error for $f_s = 10$MHz and $A_x/I_{DAC} = 1/2$. Note that, for $\varepsilon_s > 3\%$, both expressions approximately converge. However, for practical designs, i.e, for $\varepsilon_s < 0.1\%$, IM_3 due to non-linear sampling dominates, limiting the performance of SI BP-ΣΔMs unless a front-end S/H circuit will be used.

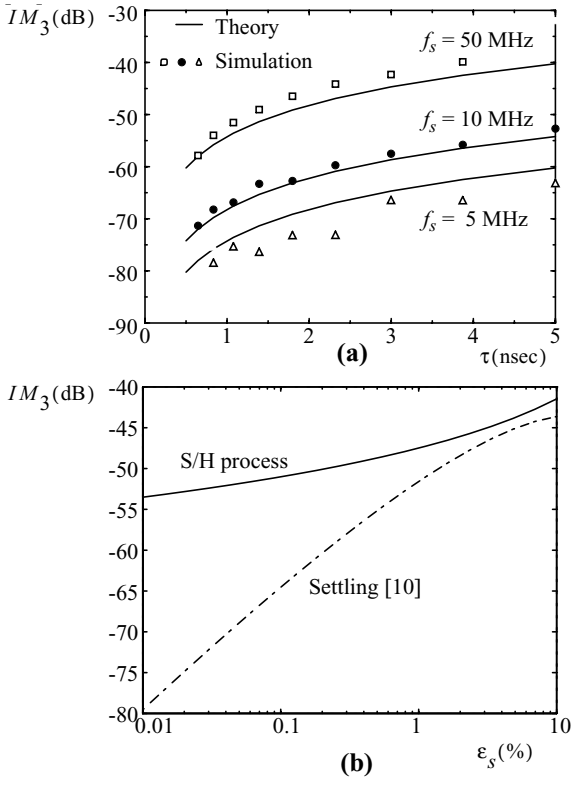

Fig. 8: IM_3 due to the non-linear sampling. a) IM_3 vs. τ. b) Comparison with IM_3 due to non-linear ε_s [10].

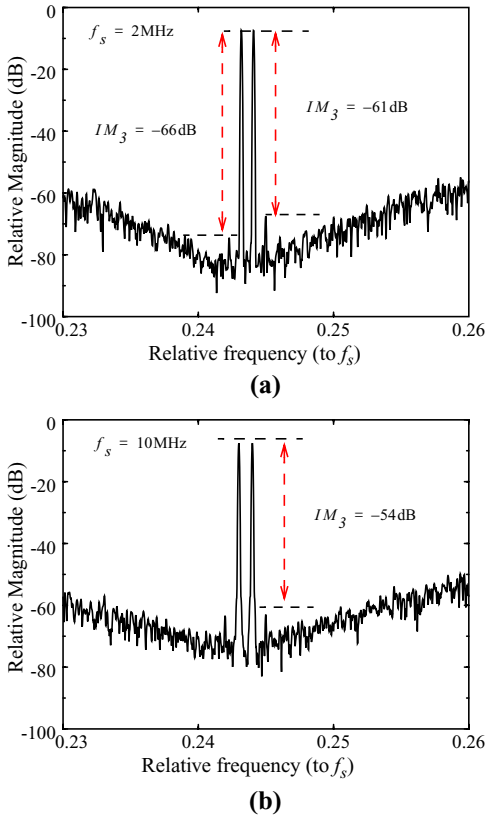

Fig. 9: Experimental output spectra for values of different f_s. a) f_s = 2MHz. b) f_s = 10MHz.

5. Experimental Results

The study presented here has been confirmed by experimental results from a 0.8µm CMOS 4th-order BP-ΣΔM, which digitizes AM signals with 10.5-bit resolution and 60mW power consumption from a 5V supply voltage [7]. Fig.9 shows two measured output spectra for A_x/I_{DAC} = 0.42 when clocked at f_s = 2MHz and f_s = 10MHz, obtaining IM_3 = −61dB and −54dB respectively. In this case, I_{bias} = 212.6µA, I_{DAC} = 50µA (n_b = 4.25), g_m = 360µA/V and C_{gs} = 2.8pF (ε_s = 0.16% at f_s = 10MHz), which according to (22) gives IM_3 = −64dB and IM_3 = −55dB respectively.

6. Conclusions

The effect of non-linear S/H process on the THD of SI circuits has been studied in detail. The analysis developed here, based on Volterra series, allows us to precisely predict the harmonic content of FD memory cells placed at the front-end of high-speed A/D interfaces. As an application, a closed-form expression has been derived for the third-order intermodulation distortion at the output of BP-ΣΔMs. This study, validated by HSPICE at the memory cell level and by experimental measurements at the modulator level, demonstrates that large HD can be obtained even for low values of the incomplete settling error, thus constituting one of the most performance limiting factors in practical designs.

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