# Selection of test techniques for high-resolution ΣΔ modulators

Oscar Guerra*, Sara Escalera*, Jose M. de la Rosa*, Eric Compaigne+, Christophe Galliard+ and Angel Rodríguez-Vázquez*
E-mails: *(guerra, escalera, jrosa, angel)@imse.cnm.es; +(eco, cga)@dolphin,fr
*Instituto de Microelectrónica de Sevilla (IMSE-CNM-CSIC) Av. Reina Mercedes, 41012-Sevilla, SPAIN.
+Dolphin Integration B.P. 65 ZIRST F38242 Meylan, France

**Abstract—This paper introduces a new tool which allows the evaluation of different test techniques in a complete impartial manner. This tool has been applied to the selection of the best test technique for their application to high-resolution ΣΔ modulators. Besides, three of these techniques have been presented.**

***Index Terms*—ΣΔ modulators, Test Techniques.**

## I. INTRODUCTION

The objective of this paper is to select the best test techniques for their application to high-resolution ΣΔ modulators. As the selection process is quite complex, a decision matrix has been created in order to evaluate the efficiency of the different techniques in term of their cost. We will first introduce this matrix, explaining the way it has to be used. Then, we will present a reference test plan that summarizes the way these kind of components are currently tested and we will evaluate the cost of the test thanks to the decision matrix on a high-resolution sensor interface. This cost could then be used as a reference to determine the efficiency of the different test techniques compared to the standard test methodologies.

## II. DECISION MATRIX

The decision matrix presented in the chart below is a tool that has been created for the TAMES-2 project in order to evaluate the efficiency of the different test techniques in term of cost.

| | Criteria | Parameters | Default value | Formula for cost computation Comments |
|---|---|---|---|---|
| 1 | Test time in second | Test time of the mixed signal function(s) | - | test time x cost of the tester used |
| | | Cost per second of the tester used (cts/s) | - | |
| 2 | Silicon area overhead in sq.mm | Area overhead (sq.mm) | - | area overhead x silicon cost |
| | | Silicon cost (cts/sq.mm) | 10 | |
| 3 | Cost of design and risk of degradation of performance due to DfT | DfT design time (man.week) | - | (DfT design time x man.week cost) / (number of chips for amortization x 10) |
| 4 | Package over cost | Cost of the package with DfT (cts) | - | (cost of the package with DfT - cost of the package without DfT) |
| | | Cost of the package without DfT (cts) | - | |
| | **Cost (cts)** | | - | **sum of all the previous costs** |
| 5 | Specification / functional coverage | Coverage is the percentage of test time covered by the DfT with reference to the test sequences it | - | **0:** no coverage<br>**0.8:** 80% coverage<br>**1:** 100% coverage |
| | **Weighted cost (cts)** | | - | **cost / coverage** |

Although in the context of the TAMES-2 Project 9 criteria have been defined in the decision matrix in order to evaluate the efficiency of the different techniques, since some of them are related to the insertion of the converter into a System-on-chip, they will not be taken into account in this paper. This means that we will use the 5 criteria in the table to estimate a figure of merit for each of the test techniques that will be considered.

For each test technique, it is required to fill in the decision matrix with all the parameter values. Then, a cost is automatically computed. The resulting "Weighted cost" allows to determine if the technique is cost effective or not.

### *A. How to fill in the decision matrix*

**1. Test time in second.** To be able to associate a cost to this criterion, 2 parameters are necessary:

- The time needed to test the mixed signal function.
- The cost per second of the tester used. For instance, for a mixed-signal tester with high (110 dB) accuracy (e.g. Teradyne Catalyst), the tester cost is around 6 cts/s. For a mixed-signal tester with low (70 dB) or medium (90 dB) accuracy (e.g. SZ tester) or for a high-end digital tester (e.g. J750), the tester cost is around 4.5 cts/s. For a linear tester (e.g. TMT) with DC capabilities or for a low-end digital tester lower than 50 MHz (e.g. KTS), the tester cost is around 3 cts/s.

The associated cost is equal to the time needed to test the mixed signal function multiplied by the cost of the tester.

**2. Silicon area overhead in sq.mm.** To be able to associate a cost to this criterion, 2 parameters are needed:

- The silicon area overhead due to the DfT.
- The silicon cost. We will assume a default value of 10 cts/sq.mm.

The associated cost is equal to the area overhead multiplied by the cost of the silicon.

**3. Cost of design and risk of degradation of performance.** To be able to associate a cost to this criterion, it is necessary to estimate the design time of the DfT.

The associated cost is equal to the DfT design costs (time for the design of the DfT multiplied by the man.week cost, with a default value of 5k€) divided by the number of chips for amortization (with a default value of 2 million units).

**4. Package over cost due to additional pins.** To be able to associate a cost to this criterion, 2 parameters are necessary:

- The cost of the package that has to be used.

- The cost of the package that could be used without DfT.

The automatically computed cost is equal to the difference of cost between those 2 parameters.

**5. Specification/functional coverage.** This parameter value has to range from 0 to 1 and represents the percentage of test time covered by the DfT with reference to the test sequence it replaces.

No cost is associated to this parameter. However, this parameter is used to compute a resulting "Weighted cost" which is equal to the sum of all the previous costs divided by this coverage value.

## III. THE SENSOR INTERFACE DEMONSTRATOR

The testchip on which all the metodologies will be tested is a ΣΔ converter aimed to operate as a sensor interface. The structure of the circuit is shown in Fig. 1 and its specifications are:

- 17 bits of resolution
- $BW$ = 20kHz
- Clock frequency, $fs$ = 5.12MHz.
- Oversampling ratio, $M$ = 128.

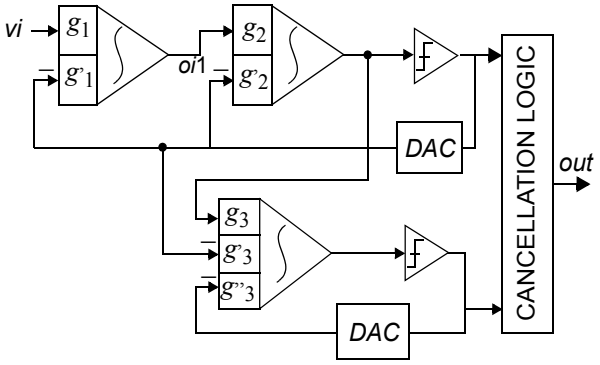


Figure 1. Block diagram of the 2-1 cascade ΣΔ modulator used for the comparison

Additional information about this circuit can be found at [1].

## IV. REFERENCE TEST PLAN

In order to establish a reference test plan for the circuits that enables the validation of the proposed techniques in terms of reduction in test time, the first important point to take into account is to determine a coherent way to measure the test time for each of the methods that will be analysed. In the context of this Project, the test time is measured according to the following rule:

$$T = N(T_{conv} + T_{over}) \quad (1)$$

where $T$ is the test time, $N$ is the number of samples needed for the test, $T_{conv}$ is the time needed to perform one measure and $T_{over}$ is the overhead time to move the data to CPU and perform the needed extra calculations to provide the test characteristic.

For the case of the sensor interface the key point of test is to cover both static and dynamic measurements.

Concerning dynamic requirements, the following measurements have to be performed:

- Signal over Noise Ratio: the SNR is computed thanks to an FFT. For SNR characteristics above 90 dB, a 8192-point FFT is sufficient. The estimated test time for this FFT is 0.3 s. Half of this time is due to the acquisition of the 8192 samples and the other half is due to FFT computation.
- Total Harmonic Distortion: the THD is also computed thanks to an FFT. However, the number of points of the FFT is directly linked to the THD characteristics that we want to measure. For example, 16384 points are necessary for measuring a -90 dB THD. Therefore, the estimated test time for this FFT ranges is 0.6 s.
- Efficient number of bits (ENOB). This measurement is obtained automatically from the FFT that is used to test the SNR or the THD. Thus, no additional time (unless some negligible computational time) has to be added to the total test time.

Then, for the case of static measurements, the following test measurements have to be performed:

- Integral non linearity, differential non linearity: INL and DNL are usually measured by means of an Histogram test applied when the input signal is a ramp (however, the same test can be performed using a sine wave, now requiring a larger number of samples). According to the specifications of our circuit, to test INL/DNL characteristics, $N$ can be estimated as $N = (2^{17} - 1)N_h M T_s$, where $N_h$ is the number of hits per code bin that, to achieve a resolution of, at least, 0.05 LSB, should be settled to 20, $M$ is the oversampling ratio and $T_s$ is the sampling period of the clock. Thus, the total required time to test static characteristics can be estimated as 65s.
  Static gain and offset can be calculated from the data achieved for the INL measurement with an almost negligible post-processing time. Thus, no additional time is devoted to this task.

## V. PRESENTATION OF THE CHOSEN DfT TECHNIQUES

After a detailed study of all the potential test techniques capable of dealing with high-resolution converters [2], the chosen test techniques for the Sensor interface have been the following:

### *A. FFT-INL.*

In order to test the static behaviour of the A/D converter, the FFT coefficients resulting after the application of the FFT test can be used to generate the coefficients of a polynomial that is the "smoothed" version of the DNL. The detailed implementation of this technique is given below, but in can be anticipated that both static and dynamic tests could be available in a relatively small amount of time (although it may exist a trade-off among accuracy and test time).

This methodology is based on two different ideas. The first one is the work introduced by J. M. Janik [3] about the estimation of non-linearities from complex spectrum.

There exists another work, introduced by F. Adamo et al. [4] which is based on the fact that the non-linear transfer characteristic of the ADC, g(x), can be seen as the cascade of a non-

linear function, gs(x), and the ideal quantization function quant(x), as illustrated in Fig. 2

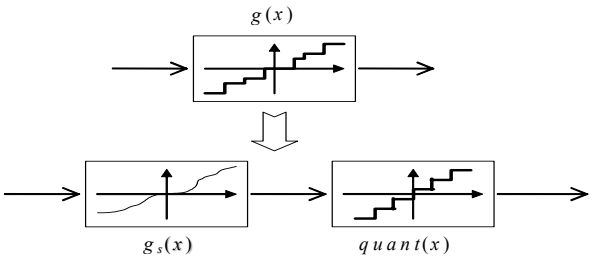


Figure 2. Transfer characteristic as the cascade of two functions

Based on these works, the methodology implemented to measure the INL of the ADC is attained in three steps:

1.) Apply a sinusoidal signal with a peak-to-peak amplitude close but without exceeding the full-scale range of the ADC. This signal has to be accurate enough to ensure that its noise and spurious harmonics do not contribute to the final measures and with a low frequency since the final objective is to determine a static characteristic.

2.) Apply the FFT to the output of the circuit and use these FFT coefficients to calculate the expansion of $g_s(x)$ in terms of the Chebyshev polynomials.

3.) Find the polynomial that approximates $g_s(x)$. This polynomial is a "smoothed" version of the INL.

### *B. Hierarchical-based.*

This technique has been fully explained in [5]. The basic idea here is to test the impact that the extra test circuitry and some specific reconfiguration schemes have on the circuit performance. Specifically, we are interested in the evaluation of the performances of the first integrator, since the impact of the defects in this integrator is more critical in the global performance than the defects in other blocks of the structure.

### *C. Wavelet-based.*

This test methodology is based on the application of the wavelet transform to the output of the converter when it is excited using a sine wave. Information about the instantaneous ENOB, SNR and INL can be obtained using less samples than those required for the standard Histogram technique. The application of the wavelet transform to the analysis and test of mixed-signal circuits has already been presented by T. Yamaguchi and M. Soma in [6].

The idea behind this method is that, in the case of an ideal ADC, if a sine-wave input is used, the output of the circuit should be also a sampled sine wave similar to the one at the input but for a possible change in amplitude and phase. Then, if a Hilbert pair resampler is applied to the output signal, the output of this block should be composed of a cosine and a sine wave. Calculating the modulus of this two signals, we should expect to obtain the amplitude of the output signal. However, if some distortion/errors are added by the operation of the circuit, there will be slight differences from this value that, in the case of using a very slow signal, should show up the influence of the circuit static non-linearity.

The proposal is illustrated in Fig. 3

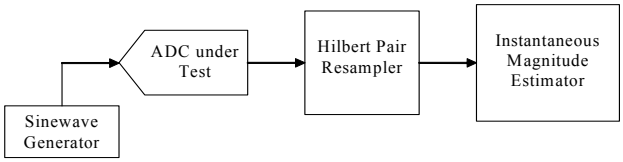


Figure 3. Application of the wavelet transform for static test

The methodology, as shown in Fig. 3, requires the application of a cosine wave to the ADC. At the output, the samples will present the contribution of both the input wave and the non-idealities of the converter.

The instantaneous magnitude of this complex signal contains the information of any step failure of the ADC under test, from where it can be measured a "instantaneous DNL" as well as the ENOB and the SNR.

These techniques will be compared to two reference test methods, the standard FFT to test the dynamic characteristics of the converter and the standard histogram test to measure its static characteristics.

## VI. EVALUATION OF THE DIFFERENT TEST TECHNIQUES

Below it is shown an initial version of the Decision Matrix concerning the methodologies mentioned in the previous Section. Notice that time estimations are not based on experimental results and may change once the implementation of the techniques is achieved.

In the table below, several comments are needed:

1.) The specification/functional coverage for the reference methods has been calculated according to the computational time required for the reference techniques. Thus, from a total estimated reference test time of around 68s, 65,5s correspond to static test, which results in approximately a 95% test coverage.

2.) For those techniques that result in measurements which are not directly related to reference test parameters, the test coverage has been estimated taking into account the kind of measurements that the techniques are able to provide.

3.) The test time for the FFT-INL and Wavelet approaches has been estimated according to the number of samples needed to perform the test and also considering the post-processing time as these techniques require from relatively complex post-processing algorithms.

4.) Those criteria related to the integration of the converter into a complete SoC have not been taken into account since there is no information available about the SoC in which the sensor could be integrated in the future. Therefore, the same

values have been given to all the test alternatives in the table to enable their realistic comparison.

| Criteria | FFT-Ref | | Histo-Ref | | FFT-INL | | Hierarc | | Wavelet | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Val | Cost | Val | Cost | Val | Cost | Val | Cost | Val | Cost |
| Test time in second | 1,2 | 7,2 | 65,5 | 393 | 35 | 210 | 0,35 | 2,1 | 22 | 132 |
| | 6 | | 6 | | 6 | | 6 | | 6 | |
| Silicon area overhead in sq.mm. | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 10 | | 10 | | 10 | | 10 | | 10 | |
| Design cost, risk … | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Packaging: diff … | 14 | 3,5 | 14 | 3,5 | 14 | 3,5 | 14 | 3,5 | 14 | 3,5 |
| Additional pins due to DfT | 30 | 0 | 30 | 0 | 30 | 0 | 31 | 1 | 30 | 0 |
| | 30 | | 30 | | 30 | | 30 | | 30 | |
| **Cost (cts)** | **10,7** | | **396,5** | | **213,5** | | **6,6** | | **135,5** | |
| Spec/ funct cov. | 0,1 | | 0,9 | | 1 | | 0,2 | | 0,8 | |
| **Weight cost** | **107,00** | | **440,56** | | **213,50** | | **33,00** | | **169,38** | |

## VII. CONCLUSIONS

Several remarks are needed in relation to the selection of the test methodologies selected at this stage of the Project:

- Hierarchical method is more devoted to a characterization test than a specification/functional test, since the information that can be extracted from it is not directly related to the parameters introduced in Section 4 (although it is clear from the analysis of the technique that both static and dynamic partial characterization of the first integrator is possible). Its implementation within the sensor interface aims two objectives. First to determine the degradation attained by the addition/ reconfiguration of the existing circuitry and second to demonstrate the validity of the approach.
- In the case of the Wavelet approach, there exists no direct relation between the "instantaneous DNL" as measured by the technique and the DNL obtained using the reference Histogram-based technique.
- For the FFT-INL approach, both static and dynamic tests are possible, although the INL characteristic is a smoothed version of what can be obtained using the classical approach. Current work is devoted to the characterization of this smoothed INL in terms of the reference parameter.

Methodologies 1 and 3 can be applied to the CUT in the form of a black-box approach. Therefore, no additional modification/reconfiguration of the A/D converter is needed. On contrary, the hierarchical-based requires some additional circuitry to be integrated on-chip: one analog buffer, some additional control logic and several switches.

Technique 1 is expected to provide full coverage, reducing the static test time significantly. However, the mathematical background of the technique and the required post-processing is quite high.

Technique 2 offers the opportunity to have a deeper knowledge on the internal circuit blocks behaviour. Thus, the technique seems more appropriate for functional test than for production test.

Technique 3 seems promising as compared to FFT analysis since the number of operations involved in the calculations is smaller than that required for the FFT. However, the practical implementation is more complex that of the FFT.

## ACKNOWLEDGMENTS

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