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Análisis, modelado y diseño de Convertidores Analógicos-Digitales de Aproximaciones Sucesivas (SAR-ADCs) con Redundancia Digital

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Analysis, modeling and design of Successive Approach Analog-Digital Converters (SAR-ADCs) with Digital Redundancy

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1 INTRODUCTION

During the last decade, the Successive Approximation Register Analog-to-Digital Converters (SAR ADCs) have shown impressive figures of merits in medium-resolution ultra-low power applications [1]–[4]. These converters are able to offer speed and accuracy with a simple architecture and do not require, in general, major design cost.

The basic task of these converters is to compare the analog input, stored in a sample-and-hold circuit (S&H), with an estimation of its value provided by a digital-to-analog converter (DAC) embedded in the architecture using a binary search algorithm. Due to the demands of speed, power consumption and low-cost, the use of a capacitor-based DAC (CDAC) in combination with latched-based comparators is a common design approach in this type of architecture [1]–[4].

In high-speed high-resolution applications the performance of these SAR ADCs is typically limited [5]–[7] by: 1) the non-linear behavior in CDAC due to the capacitor mismatch and parasites, 2) errors in comparator decisions caused by the incomplete signal settling in the CDAC or signal dependent offsets in comparator threshold [8]–[11], and 3) random noise (mainly, thermal and clock jitter). The first two sources of errors are systematic, and therefore, they are susceptible to be compensated.

To deal with capacitor mismatch in SAR ADCs, calibration has been a traditional approach since early 90's [12]. These techniques [12]–[21] use a calibration reference to obtain an estimation of the capacitor mismatch that later can be compensated in analog [12], [14]–[18] or digital domain [7], [13], [20]. As an example in [12], an auxiliary resistive ladder DAC is used for capacitor trimming. In [13], an extra CDAC is used instead.

Regarding to the errors in the comparator decisions, the digital redundancy concept has been proposed to deal with their associated limitations [14], [22]. In the conventional architecture without redundancy, the search algorithm resolves 1-bit per conversion cycle up to the complete desired resolution. The accuracy in comparison must be below the half the least significant bit (LSB) to avoid performance degradation, since any error during the binary search algorithm due to comparison mistake will be directly translated to output code. Redundancy addresses this problem based on signal processing, which in contrast to

calibration, does not require extra devices, and which is transparent to the user. The key concept in these methods is the implementation of a search algorithm in which the number of cycles is generally greater than the resolution of the converter. It uses a redundant numerical codification which defines a tolerance window around each comparator decision (redundancy interval), where mistakes in the comparator output can be corrected by the codification itself without need of interrupting the ADC operation.

The redundancy technique has been studied in many works [10]–[14], [20]–[24] and approached from various points of view. In [14], the concept of redundancy in SAR ADCs is theoretically evaluated and generalized for arbitrary radix codifications. This treatment is formally precise from the perspective of signal processing, but not for physical implementation. Thus, several aspects of relevant importance in the SAR ADC implementations are not properly covered. In the other way, there are some techniques [2], [10], [11], [13] apparently using different algorithms, which mainly focus on the practical realization.

In this work, an analysis of these SAR ADCs with redundancy has been carried out from theoretical and practical points of view [25], [26]. We will demonstrate that all these techniques are particular cases of a more general formulation. The proposed unified description reformulates the general redundancy concept using expressions which are closely related with hardware implementation, which can be particularized for the most relevant techniques in the state of the art.

In addition to the previous theoretical study, in this work a special attention has been paid to the physical implementation at the electrical level, including: a) an analysis at the architectural levels of several implementations with and without redundancy, b) development of electrical models for the building blocks in the SAR ADC including comparator, switches and SAR logic, c) an analysis of switching scheme in the CDAC, and d) implementation, verification and characterization of several case studies at the electrical level. Of particular importance in the practical implementation is the analysis of the feasibility of the capacitor scaling in the CDAC. To improve matching and maximize performance, the CDAC implementation requires using a common unit capacitance from which the rest of capacitances are derived [20], [27]. The resulting scale factors can lead to large aspect ratios between devices for resolution above 8 bits. This ratio difference could become problematic due to

technological issues (matching, noise, etc.), even making the design no feasible for high resolution. To deal with this drawback, an effective solution has been proposed in the bibliography [13], [28], [29] consisting in dividing the original CDAC into two or more arrays connected by bridge capacitances. This technique, called Split-capacitor DAC (Split-CDAC), allows scaling the LSB section by a factor, making them higher, and more suitable for physical integration, since lower aspect ratios with respect to the MSB capacitors are achieved. The key point of this new type of structure lies on the equivalent LSB capacitance referred to the MSB array through a bridge capacitor. For this reason, the sizing of this capacitance is crucial for a correct conversion.

In this work, we will analyze this effect proposing also a general formulation of Split-CDAC SAR ADCs with closed-form expressions for the CDAC sizing [28]. Explicit relationships of the impact of redundancy and bridge capacitance selections on the voltage excursion of the floating nets in the LSB array are derived. We will demonstrate that this excursion can be controlled, similarly that for the case without redundancy [28], [30], using an extra limiting capacitor in the LSB array, the optimum value of which is theoretically derived.

The contents in this document are structured as follows. In Section 2, the fundamentals of the SAR ADC are explained. Section 3 introduces the concept of redundancy and our proposed description. In this section, the proposed formulation will be verified in several implementations based on behavioral models and numerical simulations using MATLABTM. In Section 4, the validation will be complemented with electrical simulations of a realistic case study, within Design Framework II environment from Cadence[®], using macro- and Verilog-A models of their building blocks. Additionally, a review of the most commonly used switching schemes is included, as well as a comparison of their energy consumption. Section 5 shows the particularization of the theoretical description for the Split-CDAC architecture with several case studies at both behavioral and electrical levels. Finally, conclusions and future work are summarized in Section 6.

2 SUCCESSIVE APPROXIMATION REGISTER ADC

The Successive Approximation Register (SAR) ADC presents a simple architecture that implies, as shown in Fig. 1, a Sample-and-Hold circuit (S&H), a Digital-to-Analog Converter (DAC), a comparator, and a register and control logic to store the comparator output and acts over the DAC.

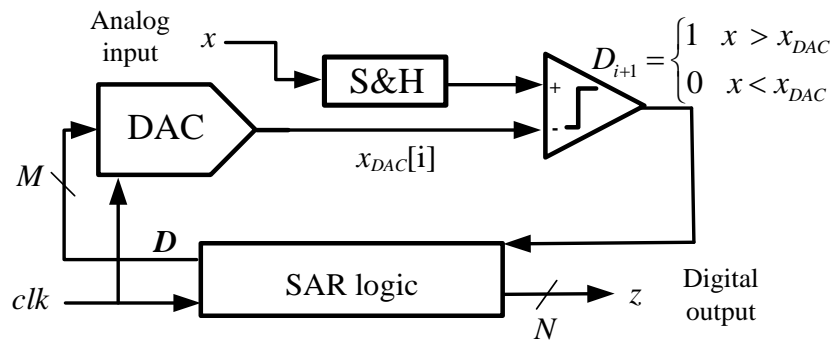


Fig. 1 Conceptual block diagram of a SAR ADC.

2.1 PRINCIPLE OF OPERATION

The general principle of operation is really intuition-closed: initially, the analog input signal, x , is sampled by the S&H, and the SAR logic is reset. Then, the stored input is compared with the initial voltage at the DAC (mid-scale, or zero in differential implementations) and the comparator decides the first most-significant bit (MSB), D_1 . With this information, the SAR logic decides the next configuration of the DAC for the following comparison. This process is repetitively done during M cycles to resolve the following bits up to the least-significant bit (LSB) one, D_M . In each step, the signal $x_{DAC}[i]$ in Fig. 1 represents the DAC estimation at the i -th conversion step, the value of which being defined by the SAR logic output \mathbf{D} according to the comparator outputs. In the final step, the stored comparator decisions (M in total) are processed by SAR correction logic to generate the ADC output code, z , with N bits of resolution. In a conventional SAR without redundancy, the number of cycles M is equal by definition to the wanted resolution N .

For illustration purpose, Fig. 2 shows the transient evolution of the DAC estimation in a 4-bit ADC without redundancy. As introduced before, the process starts with the comparison

of the sampled input voltage, x , which has an arbitrary analog value between the voltage references $[-R, R]$, with respect to the DAC reset voltage at mid-range, i.e. $x_{DAC}[1] = 0$ with $\mathbf{D} = 2^{N-1} = 8$ in the example. In this situation, as the input signal is positive, the comparator output becomes $D_1 = 1$, and the DAC estimation is updated to the mid-voltage of the remaining interval $[0, +R]$. In this case, $x_{DAC}[2] \approx R/2$ for the next iteration.

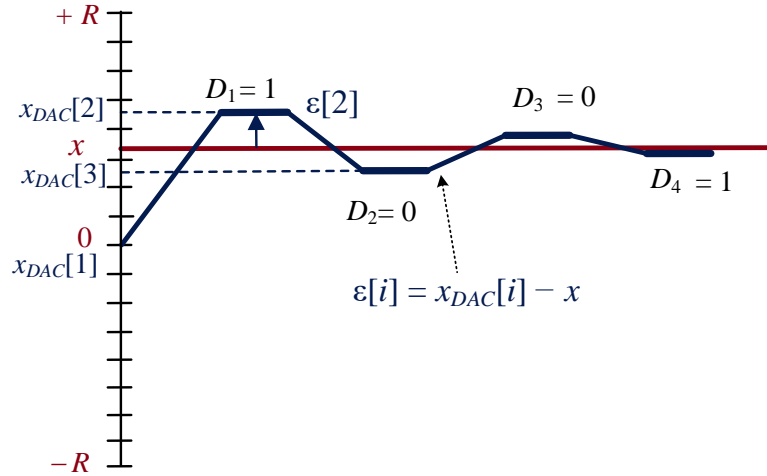


Fig. 2 Transient evolution of the DAC input estimation $\varepsilon[i]$.

As shown in Fig. 3, the estimation error, $\varepsilon[i] = x_{DAC}[i] - x$, is sequentially reduced toward zero. In the M -cycle, the value of $\varepsilon[M]$ must remain below the least significant bit (LSB) associated to the target resolution N for the final LSB bit estimation D_M ,

$$\varepsilon[M] < LSB = \frac{2R}{2^N} \quad (1)$$

Considering the information of D_M , the final quantization error is below the half the LSB as expected for an ideal ADC,

$$\varepsilon_q < \frac{LSB}{2} \quad (2)$$

To assure that the comparator accuracy does not limit performance, its accuracy must be below the quantization error. In a conventional ADC without redundancy, as shown in Fig. 3, this requirement must be maintained throughout the entire conversion time. According to the scheme in Fig. 1, the task of the comparator is determining if the sampled input signal is above or below the DAC output. This is completely equivalent, as shown in Fig. 3, to

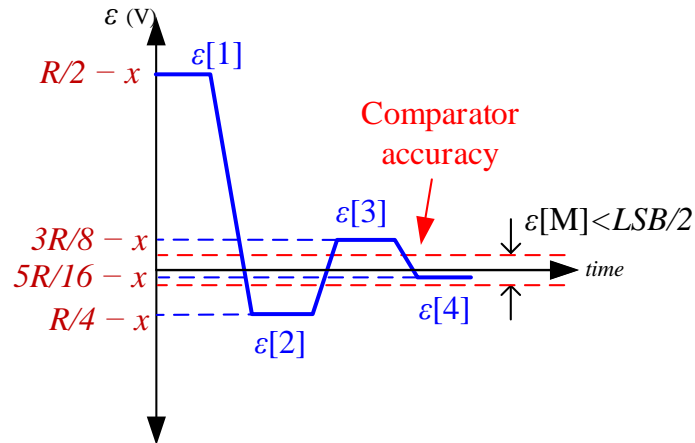


Fig. 3 Transient evolution of the error estimation $\varepsilon[i]$ and required comparator accuracy.

determine the sign of the estimation error $\varepsilon[i] = x_{\text{DAC}}[i] - x$. With this relationship, the building blocks in the SAR ADC can be re-allocated as shown in Fig. 4 to derive an equivalent realization of the SAR ADC.

In spite of its formal equivalence, the topology in Fig. 4 has several advantages for physical implementation. First, the comparator design is simplified since now all the comparisons are done with respect to the zero voltage. Second, and more important, the task of sampling, subtraction and DAC estimation can be simultaneously done in a charge-distribution topology based on capacitors with a single device [3], [10], [20], known in the bibliography as capacitor-based DAC (CDAC). Due to efficiency of this architecture, the use of a capacitor-based DAC (CDAC) is a common design approach in high-speed, low-power and low-cost applications [1]–[4]. In the following section we will analyze this structure with more details.

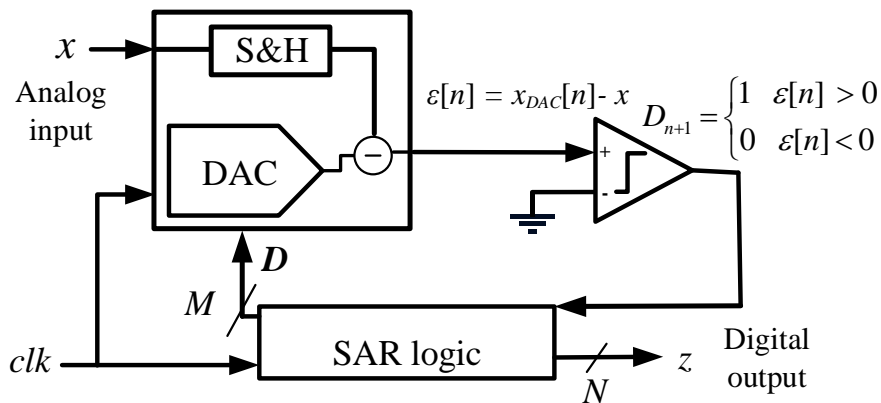


Fig. 4 Conceptual block diagram of a SAR ADC with CDAC.

2.2 IMPLEMENTATION BASED ON A CAPACITOR-BASED DAC (CDAC)

Fig. 5 shows a simplified diagram block of SAR ADC based on a fully differential implementation of the CDAC. This circuit comprises M capacitors $\{C_i\}$ and an optional capacitor C_0 to control the full-scale (FS) range $[-R, +R]$. The analog input is sampled at conversion starting in phase $\phi_{i,0}$. Then in each algorithm cycle, the comparator outputs D_i set the voltage at the different capacitors C_i , starting from the MSB capacitor to the LSB one, C_M . As described in Fig. 4, the DAC task is twofold: 1) to perform the sample and hold of the analog input $x = x_+ - x_-$, 2) to generate the estimation error, $\varepsilon[i]$, between the input signal and the CDAC output at each conversion step, i , according to the comparator output D_i . The SAR process must force, as shown in (1), the $\varepsilon[M]$ value to be below the N -bit LSB at the end of conversion. If this condition is not satisfied, the converter will not be able to obtain the digital output with N -bits precision.

In an ideal situation with N -bit resolution without redundancy, the CDAC must generate 2^N different levels for comparison within the full-scale $FS = 2 \cdot R$, being the capacitor binary scaled, and the number of cycles needed to carry out the conversion $M = N$. The final digital word z , at the end of the conversion process is obtained as the direct concatenation of the

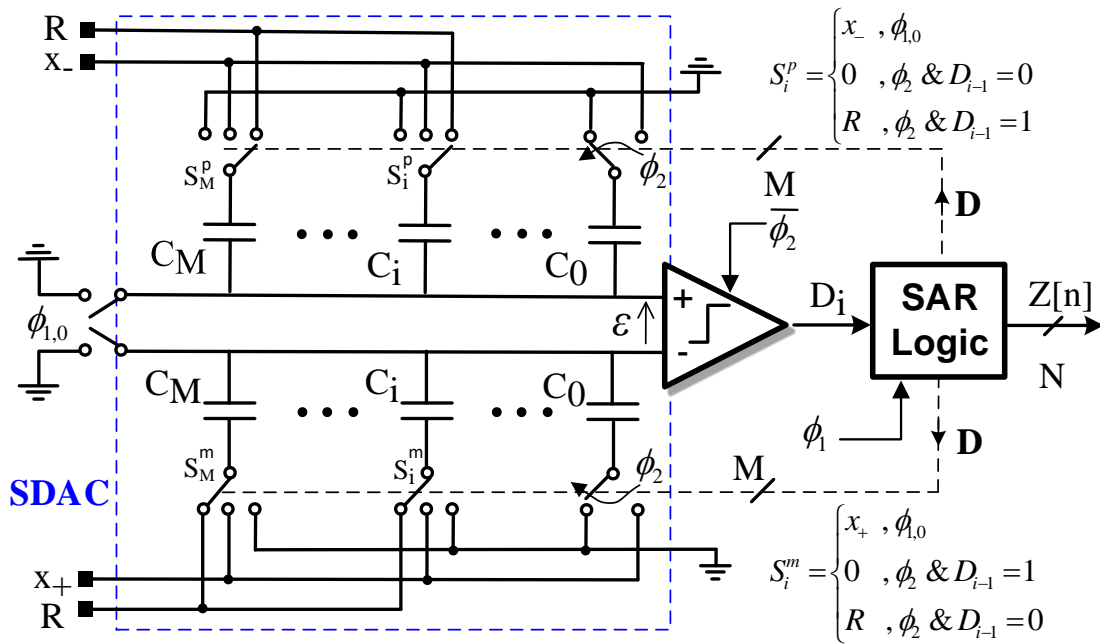


Fig. 5 Fully differential implementation of a SAR ADC. Phase $\phi_{1,0}$ is the initial sampling phase, and ϕ_2 is the ϕ_1 's complementary phase.

stored comparator output bits $z = \mathbf{D} = [D_1, D_2, \dots, D_{M-1}, D_M]$, simplifying the generation of the digital correction logic, generally given by the following expression,

$$z = \sum_{i=1}^M D_i W_i \quad (3)$$

since the digital weights, W_i , results also binary scaled.

2.3 CAUSES AND EFFECTS OF COMPARISON ERRORS

A major source of degradation in SAR conversion is the errors made by the comparator, as the final result of the conversion depends intrinsically on its output. This effect has three basis terms:

- The comparator errors itself: these include the time variant errors contribution in the offset due to the input signal dependent effects and noise sources (thermal, jitter, etc.).
- The errors associated to switches: signal dependent effects of the switches on-resistances and charge injection could also produce a contribution to the effective offset in comparison.
- The incomplete settling in the CDAC: this includes all the settling errors in the CDAC depending on the comparator output commutation after the sampling process.

Among these effects, the incomplete settling becomes dominant at high speed. As shown in Fig. 6, an incomplete settling means that the sampled signal does not have enough time to

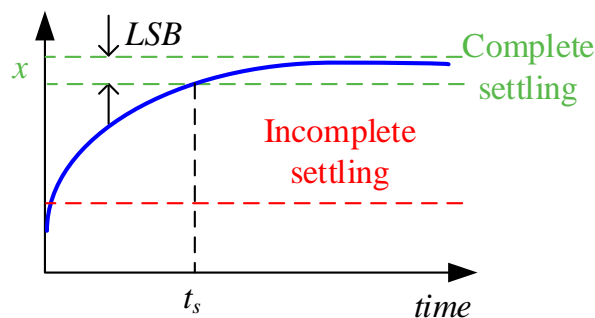


Fig. 6 Incomplete settling in the CDAC.

settle to the expected analog value in the quiescent situation. The greater the conversion frequency, the smaller the settling time t_s , and the greater the error is.

Independently of the origin of the comparison mistake, once an error has been made in a design without redundancy, it is impossible to recover the correct value at the output. Fig. 7 and Fig. 8 show this behavior in a 4-bit example without and with errors in the conversion, respectively. For sake of simplicity, the full scale $[-R,+R]$ has been defined between 0 and $2^N = 16$. In the first case (Fig. 7), all the comparator decisions are correct, and the result of the conversion process is right. However, the digital output depends strongly on the comparator output. Fig. 8 shows the same illustrative example with comparison errors. If an error occurs at the i -th cycle, a wrong additive term with value $D_i \cdot W_i$ is included at the output code in (3). This error level cannot be compensated by the classic SAR algorithm since, by definition, the sum of the remaining digital weights contributions are lower than the introduced error as theoretically demonstrated in the next section.

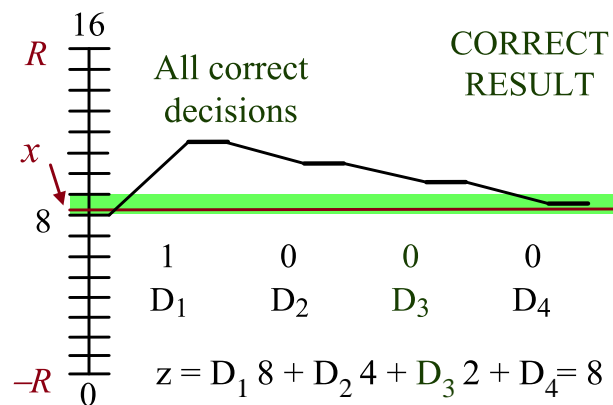


Fig. 7 4-bit SAR ADC algorithm binary radix.

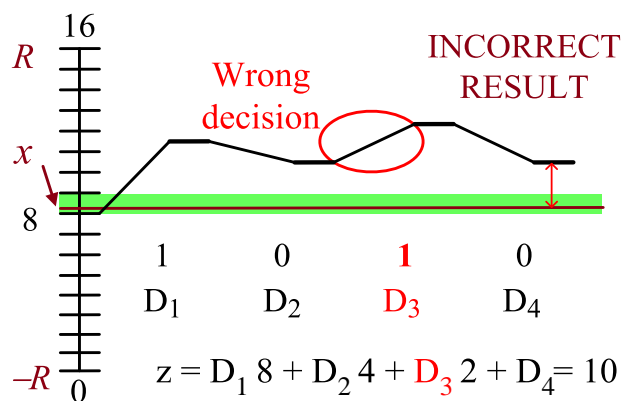


Fig. 8 4-bit SAR ADC algorithm binary radix with a comparison error in 3th cycle.

3 REDUNDANCY TECHNIQUES IN SAR ADC

The solution to deal with the previous problem is the use of redundancy [14], [22], [25]. These methods implement a search algorithm where the number of cycles, M , is generally greater than the resolution ($M > N$), introducing redundancy in the definition of the weighting coefficient in the correction logic, given by (3), in such a way that if an error in certain cycle occurs, the remaining cycles could recover the right estimation.

As highlighted in the introduction, in the bibliography the redundancy concept has been addressed from two different points of views. In [14], the concept of redundancy is theoretically evaluated and generalized for arbitrary radix codifications. This treatment is formally precise from the perspective of signal processing, but several aspects of relevant importance in SAR ADC implementations are not covered, such as: 1) the correspondence between capacitor scale factors and digital weighting coefficients, or 2) the need of eliminating the capacitor associated to the most significant bit to implement redundancy. In the other way, there are some work [2], [10], [11], [13], [20] apparently using different algorithms, which mainly focus on the practical realization. Thus, in [2], [10], [11], [13], arbitrary selection of the weighting coefficients are considered to allow an optimum distribution of the redundancy through the conversion steps. However, as we will see, this advantage is achieved at expenses of incrementing the correction logic requirements that implies more area and more power consumption (for instance, in [31] a ROM is used). To get rid of this overhead, several approaches have been proposed. A possibility is use of an extended binary codification [11], [15] aiming the simplicity of the conventional binary scheme on which the correction logic is simplified since the output code is obtained as the concatenation of the stored comparator output. These techniques create redundant decisions, to correct mistakes in comparator output, duplicating some of the capacitors in the DAC and using extra clock cycles, but it could imply a reduction of the effective full-scale to avoid overranging, as analyzed in [10], [11].

In this work, we will demonstrate that all these techniques are particular cases of a more general formulation. The proposed unified treatment reformulates the general redundancy concept using expressions which are closely related with hardware implementation, which can be particularized for the existing methods and it is independent on the considered switching scheme in the CDAC [1], [20], [32].

3.1 PROPOSED UNIFIED DESCRIPTION OF SAR ADC

In our proposed formulation, the correction logic in (3) is modified to include an additional constant term z_0 . The aim of this modification is to make explicit the presence of an offset in the generation of the digital output z (with N -bit resolution), depending on the practical CDAC implementation and codification,

$$z = z_0 + \sum_{i=1}^M D_i W_i \quad , \quad W_i \geq W_{i+1} \quad (4)$$

where, as in the conventional SAR ADC, $D_i = \{0,1\}$ is the comparator output bit, W_i are the digital weights (radix) and M is the number of cycles ($M = N$ just for the case without redundancy):

Considering the topology in Fig. 5, and establishing a bipolar implementation with $FS = [-R, R]$, the first capacitor C_1 can be omitted in the charge-merged architecture [14], [20], since the comparison of injected signal with the mid-range, $\varepsilon [1] = 0$, produces directly the Most-Significant-bit (MSB), D_1 .

Now, D_i controls the set voltage at the different capacitors C_{i+1} , where sub-index explicitly shows a displacement in the bit actuation. Taking in mind this possibility, herein assumed without lack of generality, the capacitor array can be designed based on a common unitary capacitor C and the capacitor ratio p_i , it is given by,

$$C_i = p_i C \quad ; \quad i = \{2, \dots, M\} \quad ; \quad C_1 = 0 \quad (5)$$

Fig. 9 shows the transient evolution of the DAC voltage estimation of analog input with a resolution $N = 4$ performed in $M = 4$ cycles. In the first cycle the input signal is compared with the mid-range producing the MSB. Depending on the comparator decision, D_1 , the DAC estimation in the next cycle $\varepsilon [2]$ is updated summing or subtracting in charge domain a certain voltage related to the capacitor scale factor, in the form,

$$\varepsilon[2] = \varepsilon[1] + (2D_1 - 1) p_2 \frac{RC}{C_t} \quad (6)$$

where $C_t = \sum C_i$ is the total capacitance in each branch.

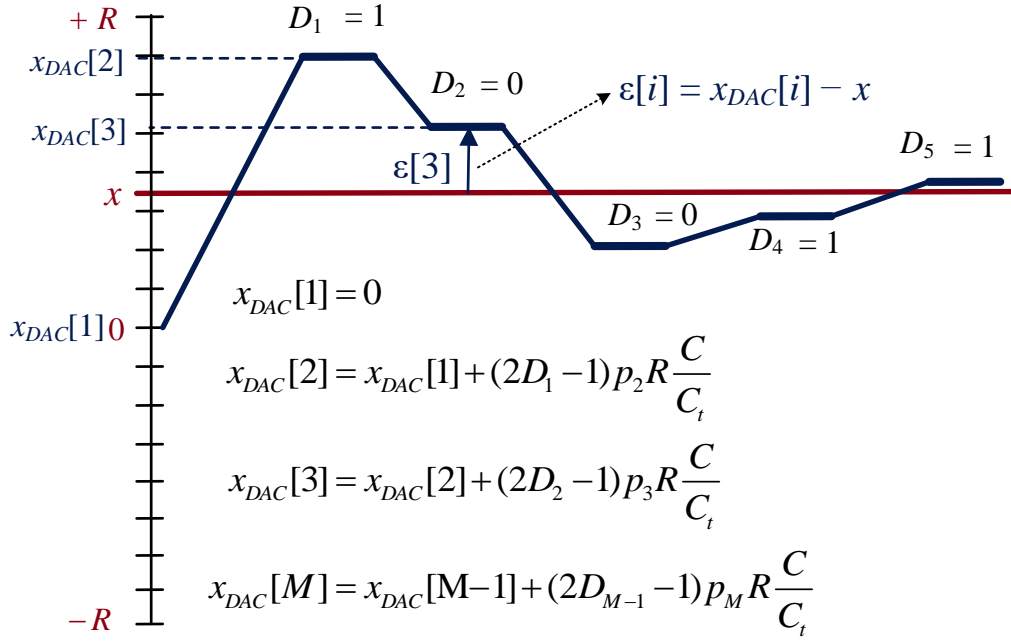


Fig. 9 Transient evolution of the DAC input estimation $\varepsilon[i]$.

Repeating the process, we can obtain the final DAC estimation as follows,

$$\varepsilon[M] = \left(\sum_{i=1}^{M-1} (2D_i - 1)p_{i+1} \right) R \frac{C}{C_t} \quad (7)$$

$$\text{with } C_t = C_0 + \sum_{i=2}^M C_i = C \left(p_0 + \sum_{i=2}^M p_i \right)$$

which corresponds to a digital counterpart, $\Delta z[M]$, measured in effective LSB (LSBe), as

$$\Delta z[M] = \sum_{i=1}^{M-1} (2D_i - 1)p_{i+1} \quad (8)$$

$$\text{with } \text{LSBe} = \frac{R}{\left(p_0 + \sum_{i=2}^M p_i \right)}$$

The ADC digital output after last cycle is:

$$z = p_1 + \sum_{i=1}^{M-1} (2D_i - 1)p_{i+1} + (D_M - 1) \quad (9)$$

where three different terms can be identified: a) the best approximation (8), $\Delta z[M]$, b) the digital contribution of latest residue, $\varepsilon[M]$, with the additive term $(D_M - 1)$, and c) a constant

term to get on offset binary codification, herein labeled p_1 . Adjusting the range of z to the nominal case $[0, 2^N - 1]$ by assigning the mid-range code 2^{N-1} to the zero-analog input ($x = 0$), the value p_1 is 2^{N-1} .

Comparing (4) and (9) the relationships between the capacitor scale factors p_i , the digital weights W_i and offset term z_0 in (4) can be obtained as,

$$W_i = 2p_{i+1}, W_M = 1 \quad \text{and} \quad z_0 = p_1 - \sum_{i=2}^M p_i - 1 \quad (10)$$

Evaluating expression (9) for the limit cases (e.g. when the comparator outputs D_i being all ones), the codification overrange, OR , defined by $z \in [-OR, 2^N - 1 + OR]$ as shown in Fig. 10, becomes,

$$OR = \sum_{i=1}^M p_i - (2^N - 1) = -z_0 \quad (11)$$

The proposed description makes an explicit distinction between the capacitor scale factors p_i in (5) and the digital weights W_i in (4) and (10). This study is fully general and valid for typical SAR algorithms without and with redundancy, such as: binary scaled, arbitrary weights, etc. In the following subsections this theoretical development is particularized for the most commons techniques in the state-of-the-art.

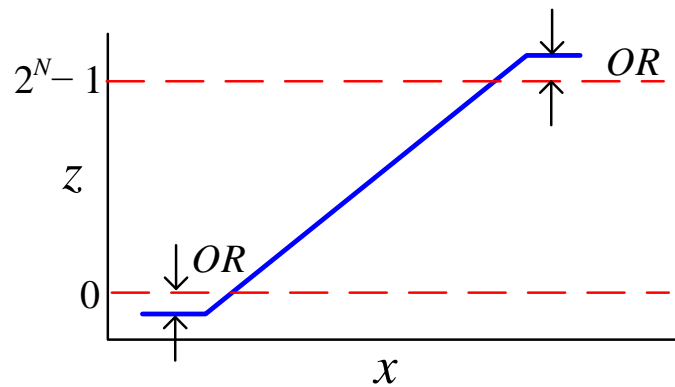


Fig. 10 Overrange in the transfer function of ADC

3.1.1 SAR ADC without Redundancy (Binary-scaled Weights)

In the conventional case without redundancy ($N = M$), the final output code z can be just obtained as the concatenation of the comparator output bit-stream $z \equiv [D_1, D_2, \dots, D_N]$ without the need of any arithmetic logic, therefore $W_i = 2^{N-i}$. Applying (10), the capacitor scale factors p_i results also binary weighted, $p_i = 2^{N-i}$, while according to (11), $z_0 = 0$.

Fig. 7 and Fig. 8 shows an illustrative example of this algorithm for the case with $N = 4$ without and with comparator errors. Notice that in presence of comparator decision errors (at D_3 in the example of Fig. 8), the output code z is not correctly generated. If an error occurs at the i -th cycle, a wrong additive term with value W_i is included at the output code in (4). This error level cannot be compensated by the SAR algorithm since the maximum magnitude of the remaining contribution is lower than the introduced error,

$$W_i = 2^{N-i} > \sum_{k=i+1}^N W_k = \sum_{k=i+1}^N 2^{N-k} = 2^{N-i} - 1 \quad (12)$$

The solution to deal with this problem is the use of redundancy as detail in next section.

3.1.2 SAR ADC with Redundancy (Arbitrary Weights)

The problems associated to the comparator decision mistakes can be compensated, as previously introduced, considering extra clock cycles in the search algorithm ($M > N$), in such a way that if an error in certain cycle occurs, the remaining cycles could recover the right estimation [14].

To allow correcting an error a i -th conversion step, the sum of remaining scale factors must be greater than a tolerable error of e_i (*LSBe* units). This is,

$$e_i \leq -W_i + \sum_{k=i+1}^M W_k = -2p_{i+1} + 1 + 2 \sum_{k=i+2}^M p_k \quad (13)$$

If q_i is defined as the amplitude of the redundancy interval, i.e. the safety interval within which a bad comparator decision can be effectively corrected, and it is evaluated this way,

$$\forall i \in [1, M-1], \quad q_i = -p_{i+1} + 1 + \sum_{k=i+2}^M p_k \quad (14)$$

Then, the tolerance error in (13) is bounded by $|e_i| \leq q_i$ (*LSBe*). Equation (14) establishes a fixed relationship between the selected scale factors and the tolerance redundancy interval suitable for design. Alternatively, given a wanted specification of tolerance q_i , the needed scale factors in the capacitor array can be determined resolving recursively from (14) in the form,

$$\forall i \in [2, M], \quad p_i = 2^{M-i} - q_{i-1} - \sum_{k=i}^{M-1} q_k 2^{k-i} \quad (15)$$

Both (14) and (15) are equivalent and can be considered as starting design equation for the SAR ADC sizing. However, given the importance of matching and feasibility of the CDAC, we recommend the use of (14), checking after that if the achieved level of redundancy is enough for the application. In this selection, the relationship between the total sum of coefficients p_i and the overrange OR (for a given resolution N) must be also considered according to (11) which can be alternatively expressed [14] as,

$$OR = 2^M - 2^N - \sum_{i=1}^{M-1} 2^i q_i \quad (16)$$

making evident than for a case without redundancy ($M = N$ and $q_i = 0$), there is not overrange.

Let us continue with a practical example showing how redundancy works. In Fig. 11a-b, two cases with $N = 4$ without and with comparison errors affecting the first bit D_1 are presented. The process starts from the mid-range, that is $p_1 = 2^{N-1}$. Notice that in contrast to the situation in Fig. 3b, the resulting redundant searching algorithm is immune to the comparator decision mistake. The immunity to the comparator decision error is achieved trading-off error tolerance and complexity of the digital correction logic. The implementation of (4) will generally imply the presence of a relatively complex arithmetic logic that may comprise adders and multipliers, or ROM [31]. To deal with hardware complexity, several techniques have been proposed [14], [20]. However, these methods are just specific implementations (aiming the reduction of the digital correction hardware), which can be described with the proposed unified description, as analyzed in the following section.

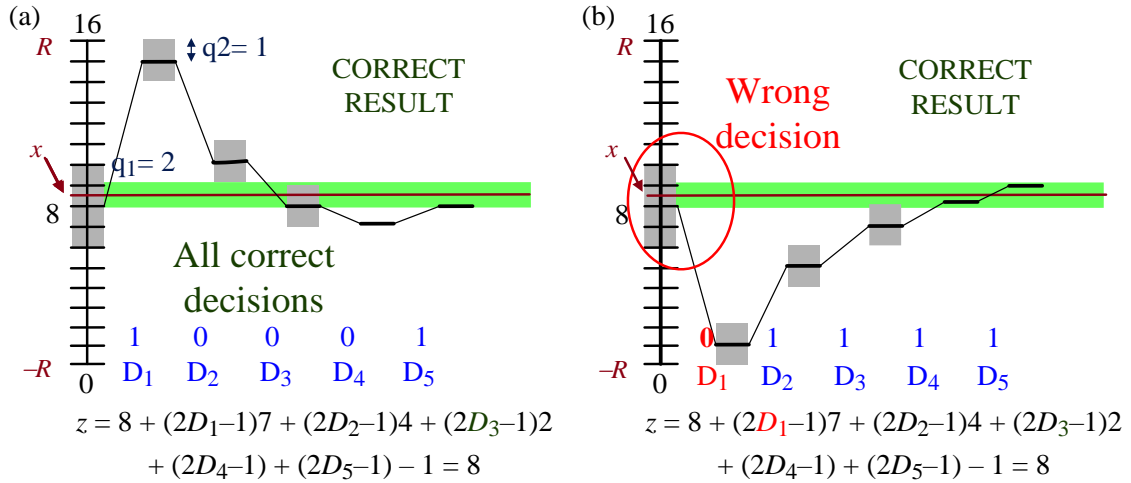


Fig. 11 4-bit SAR ADC algorithm with 5-cycle redundant non-binary radix: a) all correct decisions, and b) one wrong decision at 1st cycle. Example with: $\mathbf{p} = \{8, 7, 4, 2, 1, 1\}$ and $\mathbf{q} = \{2, 1, 1, 1, 0\}$.

3.2 ANALYSIS OF SAR ADC TECHNIQUES USING THE PROPOSED UNIFIED DESCRIPTION

This section analyzes some case studies with arbitrary redundant weights, as well as some of the most relevant SAR ADC techniques in the state-of-the-art [14], [22], [31]. Several implementations and simulation results are shown.

3.2.1 Arbitrary Redundant Weights

Let us particularize the general formulation in previous section for a first SAR ADC case study with $N = 10$ and $M = 12$. This case is directly applicable to SAR ADCs in [2], [10], [11], [13], the difference between them just found in the overrange in (16). Starting from the following analog scale factors, $\mathbf{p} = \{512, 321, 181, 101, 57, 32, 17, 10, 5, 3, 2, 1\}$, the DAC is sized using (5), and the implemented overrange OR becomes 219, since $\sum p_i = 1242$ exceeds the nominal range $[0, 1023]$. For this selection, according to (14), the redundancy interval vector is $\mathbf{q} = \{89, 48, 27, 14, 7, 5, 2, 2, 1, 0, 0\}$, establishing a tolerance in the comparator decision of 89 *LSBe* for the most significant bit D_1 .

The sizing process can be extrapolated for other designs with different resolutions. Fig. 12 shows the behavioral simulations results (output spectrum) for a 100Mps SAR ADC

with $N = 12$ and $M = 15$. In this design, the conventional capacitor scale factors, $\{2^{M-i}\}$, were adjusted by a multiplicative term $2^{N/M}$ under the constrain of getting a null overrange ($OR = 0$) with $\mathbf{p} = \{2048, 872, 501, 288, 165, 95, 54, 31, 18, 10, 6, 3, 2, 1, 1\}$ and $\mathbf{q} = \{304, 174, 99, 57, 32, 19, 11, 6, 4, 2, 2, 1, 1, 0\}$. A fully-differential implementation of the CDAC and the conventional switching scheme [20] was considered. Results for other switching scheme (see Annex I) such as the monotonic [1], [23], omitted in the figure, are in similar agreement. The uncertainty of each comparator decision was generated using random-variant offset with uniform distribution and amplitude equal to 50% of its redundancy window. The rest of error sources in the ADC model was disable to check the effectively of redundancy.

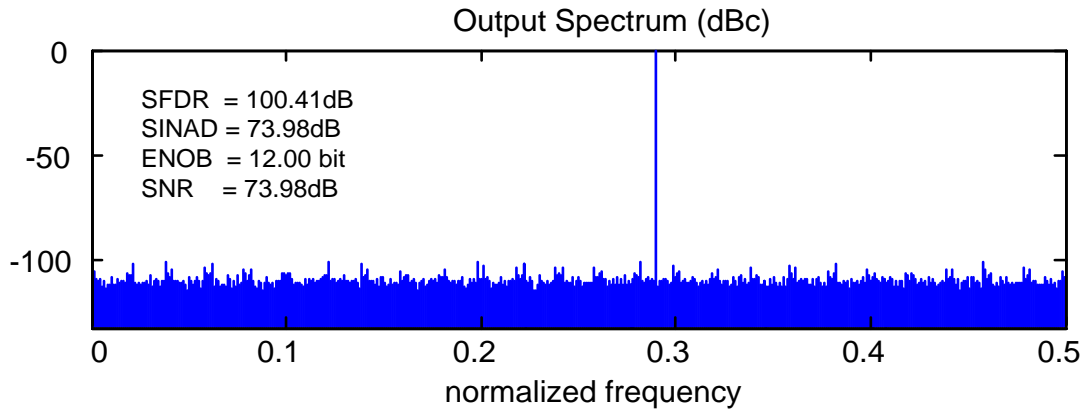


Fig. 12 Output spectrum of a 12-bit 100Msps SAR ADC case study with redundancy (arbitrary weights) in presence of comparator errors.

As expected, the output code is completely insensitive to the comparator errors and the effective number of bits ($ENOB$) is 12.0 bits. In this example, the spectrum was evaluated using a full-scale sinusoidal input signal ($FS=2V_{pp}$) and 29MHz frequency. The results in term of static performance (INL, DNL) are in agreement with the ideal behavior.

Fig. 13 shows a comparison of the input output characteristic of the ADC in two different situations. To make evident the effect of redundancy, a mismatch error in the capacitor scale factor \mathbf{p} are introduced in one of the cases resulting now $ENOB = 8\text{bits}$ and $|INL|_{max} = 4.5 \text{LSBe}$. Notice that without mismatch error, the effect of comparator uncertainty is unobservable, since it is completely ideal.

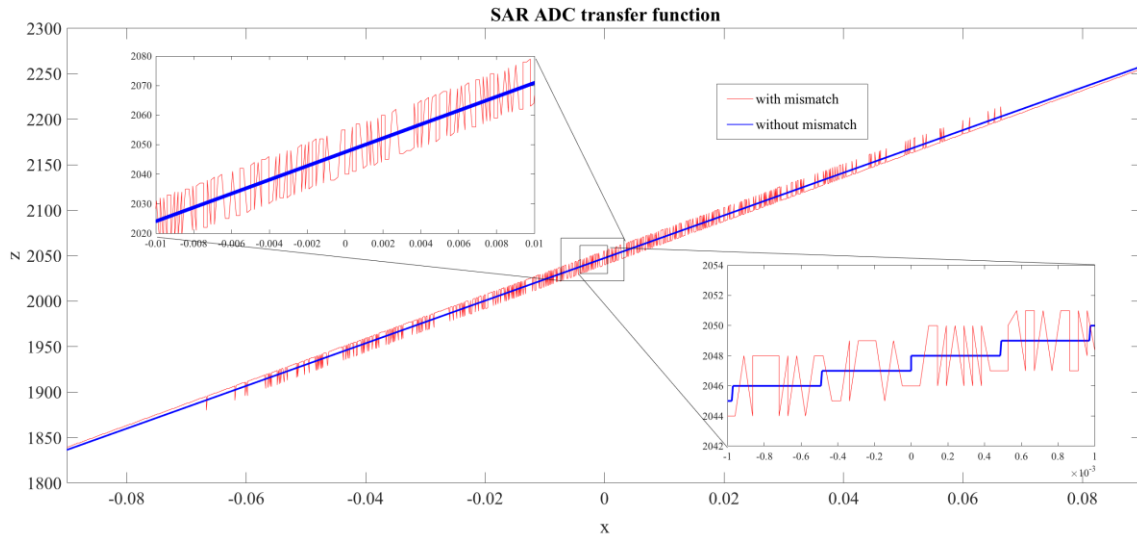


Fig. 13 Zoom-in of the input-output characteristic with and without capacitor mismatch errors.

3.2.2 Binary Extended Weights

The redundancy implementation of the previous method is achieved at expenses of incrementing the calibration logic requirements (area and power consumption). To get rid of this overhead, several approaches have been proposed. A possibility is use of an extended binary codification [11], [15] aiming the simplicity of the conventional binary scheme in section 3.1.1. The technique creates redundant decisions to correct mistakes in comparator output duplicating some of the capacitors in the CDAC and using extra clock cycles.

This extended binary option can be contemplated in our unified description introducing duplication in some of the capacitor scale factors. Let us exemplify this technique with a first case study in which the weights associated to the 3-rd and 7th bits are duplicated, that is: $\mathbf{p} = \{128, 64, 32, 32, 16, 8, 4, 2, 2, 1\}$ with $p_4 = p_3$ and $p_9 = p_8$ (i.e. $\mathbf{q} = \{34, 34, 2, 2, 2, 2, 2, 0, 0\}$). In this case, the weighting coefficients in the digital correction logic in (10) are greatly simplified. Actually, as shown in Fig. 14 the logic can be implemented by just considering a small arithmetic unit in which the bits associated to the redundant capacitors are binary shifted and added. In this situation, digital implementation (shown in Fig. 15) is moderate, since only multiplexers and a small set of half-adders and full-adders are required to obtain digital bits [10], [11]. The penalty is that, as in [11], a systematic overrange is always present

($OR = 34$) according to (11), since the sum of weights exceed the expected range for $N = 8$. To deal with this overrange, the input signal full-scale must be therefore scaled down a 12%.

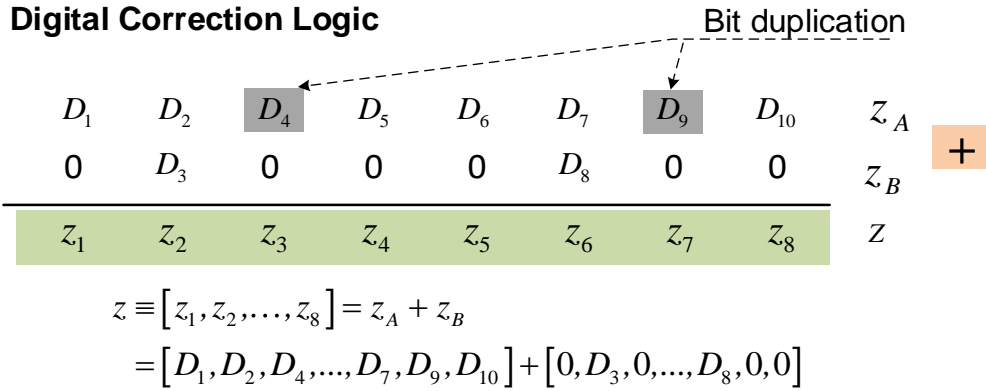


Fig. 14 Simplified implementation of the digital correction logic in the SAR ADC (binary extended weights) consisting in a binary shifted addition.

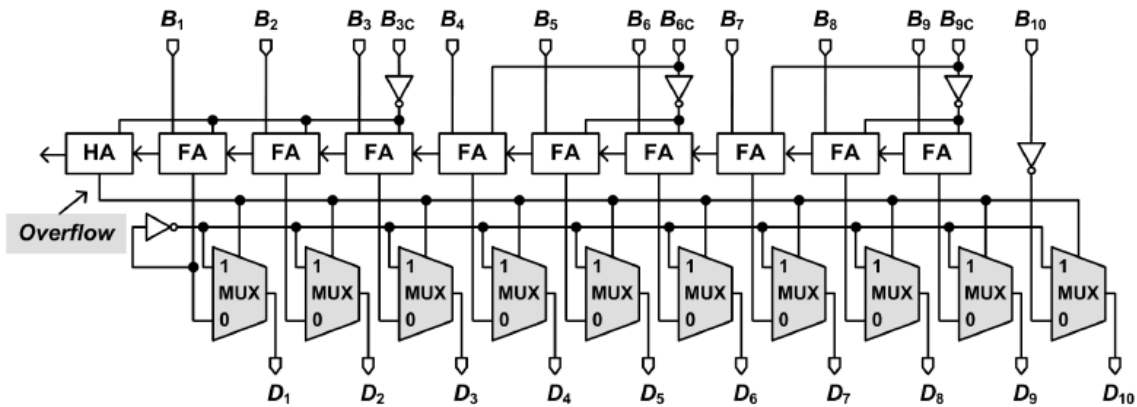


Fig. 15 Diagram of the implementation of the arithmetical logic in the SAR ADC (binary extended weights) implemented in [11].

3.2.3 Split-capacitor Technique for Redundancy

The drawback of the previous method in term of overrange can be dealt assuring the sum of the scale factors in (5) does not exceed the limit for a giving resolution. In [2], [10], this goal is achieved splitting the most significant capacitor (C_2 , since C_1 is omitted) and distributing its contribution among the SAR ADC queue. These techniques can be

straightforward analyzed with the proposed description using just additional terms in the capacitor scaled vector.

As an example, let us consider a situation with $N=10$ and $M=13$, in which $C_2 = p_2' C$ is split in four sections ($M-N+1=4$) located in the 2nd, 4th, 8th, and 11th positions, i.e. $p_2' = p_2 + p_4 + p_8 + p_{11}$. With this definitions, the effective capacitor scale factors become $\mathbf{p} = \{512, 192, 128, 64, 56, 32, 16, 8, 7, 4, 2, 1, 1\}$ and all the results in section 3.1 are directly applicable. As an example, using (14), the redundant intervals are given by $\mathbf{q} = \{128, 64, 64, 16, 8, 8, 8, 2, 1, 1, 1, 0\}$.

4 ELECTRICAL SIMULATION OF SAR ADC WITH REDUNDANT WEIGHTS

In this section, the proposed formulation in Section 3 is used to generate weighting coefficients and scaling factor in the capacitor-based DAC (CDAC). As case of study, the design of a 1.8V 12-bit SAR ADC based on merged-capacitor architecture [33] is considered. The topology uses three extra cycles, i.e. $N = 12$ -bit and $M = 15$, for dealing with comparison errors due to incomplete settling in the DAC and random/signal-dependent offsets in the comparator itself. To simplify the hardware associated to the digital correction logic, a binary decomposition of the weighting coefficients [2], [10] was considered as explained in Section 3.2.3.

Contents in this section are distributed as follows. In Section 4.1, an analysis of switching scheme and its power consumption in the CDAC is carried out. Section 4.2 shows the detail on the CDAC sizing and architecture. We continue in Section 4.3 with the temporization of the SAR logic, showing the advantages of the asynchronous implementation versus the classical synchronous logic. Finally, some details on the proposed modeling approach and the verification results at the electrical level are presented in Section 4.4.

4.1 SWITCHING SCHEMES IN THE CDAC

The way in which the comparator output acts over the switches, known in the bibliography as switching scheme [1], [20], [33]–[36], has crucial implications for energy consumption and for the required time for conversion. However, it is important to note that the final residue at each conversion step during the SAR binary search algorithm has to be the same in all them for an equivalent conversion, being the optimum selection depending on extra considerations. In [20] some switching schemes are reviewed and an energy consumption comparative is carry out to discriminate the more suitable for a specific implementation.

In the following sections, a review of the most relevant switching schemes in the state of the art are presented taking into account the implications for the CDAC as well as the consumption per conversion step.

4.1.1 Conventional Switching Scheme

Fig. 16 shows an illustrative example of the conventional switching scheme. In this scheme, the analog input signal is sampled in the bottom plates of the capacitors. Later, the most significant capacitor is switched to R (GND) in the positive (negative) branch and the comparison start: if $D = 1$ the switch maintains the configuration, if $D = 0$ the switch goes to R (GND). The energy drawn from voltage source R per switch in each capacitor can be calculated as follows:

$$E_i = \int_{0^+}^T i_{C_i} \cdot R dt = -R \cdot \int_{0^+}^T \frac{dQ_{C_i}}{dt} dt = -RC_i \cdot \int_{0^+}^T d\varepsilon_i \quad (17)$$

$$= -RC_i \cdot [(\varepsilon_i(T) - \varepsilon_{BP}(T)) - (\varepsilon_i(0) - \varepsilon_{BP}(0))]]$$

where ε_{BP} is the voltage set by the switch at the bottom plate of the capacitor, and T is the elapsed time for voltages settling. Particularizing (17) for a M cycles conversion process, we can get a closed expression for the mean consumption as follows:

$$E_{conv} = CR^2 \sum_{i=1}^M 2^{M+1-2i} 2^i - 1 \quad (18)$$

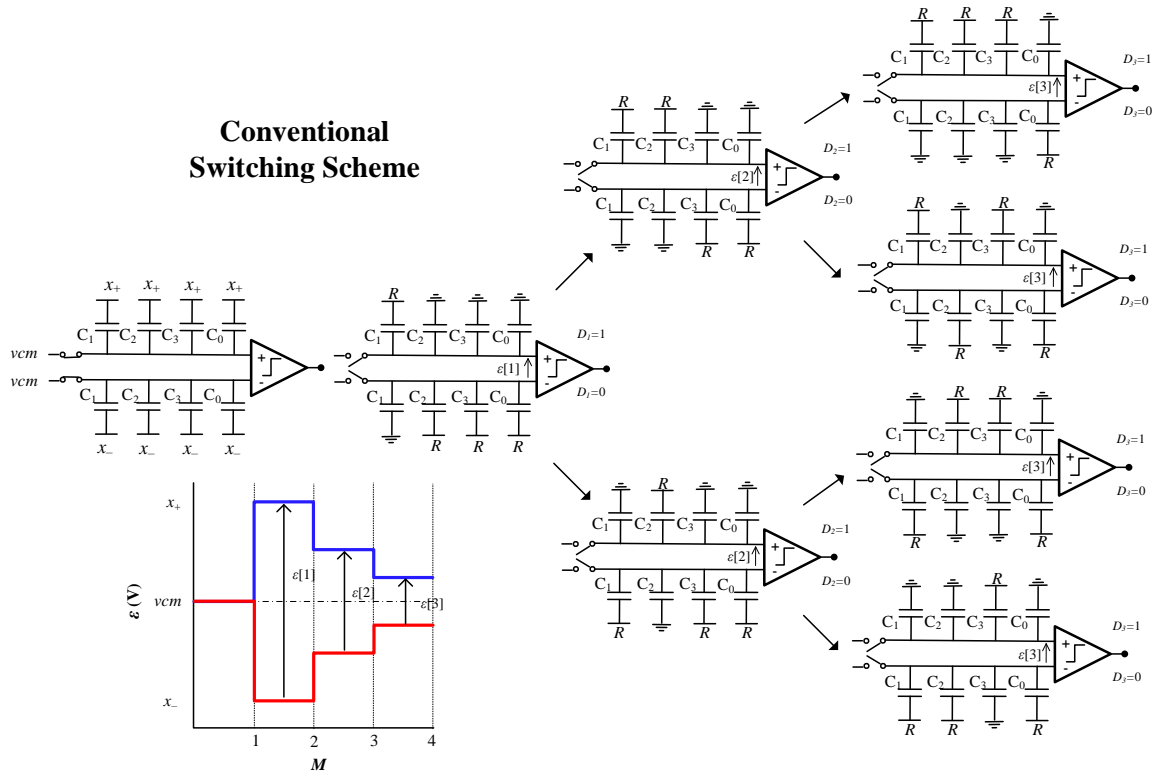


Fig. 16 Conventional switching scheme and voltages excursions for a 3 bit SAR ADC

4.1.2 Merged Capacitor Switching Scheme

An alternative to the conventional scheme, aiming the reduction of commutation power, is proposed in [33]. This approach, called merged capacitor switching algorithm (MCS), samples the analog input signal on the top plates of the capacitors. As shown in Fig. 17, the first comparison occurs immediately after sampling and it does not require any charge redistribution. Successively, if comparator output is “1” (or equivalent, “0”), the largest capacitor in the positive (negative) array, C_2 , is settled to GND (R).

In contrast to the conventional switching scheme in Section 4.1.1, which requires M capacitors to carry out a conversion process with M cycles, the MCS algorithm can achieve a M cycles conversion process with $M - 1$ capacitors since the first bit is decided directly with the primary input acting on the comparator. This method drastically reduces, with almost null cost, the total capacitors size and the energy consumption, since the first comparison in the conventional scheme usually requires more than 75% of the total energy consumption [20].

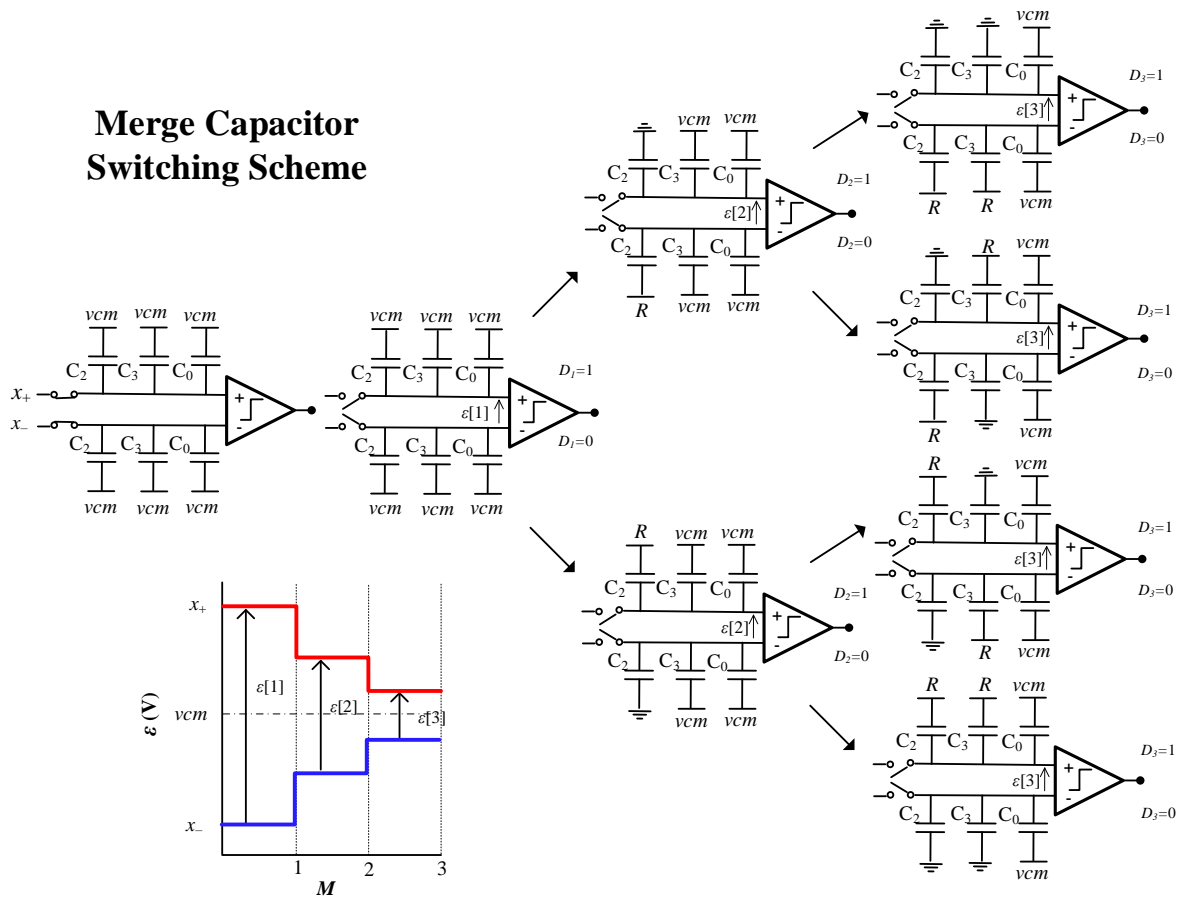


Fig. 17 Merged capacitor switching scheme and voltages excursions for a 3 bit SAR ADC

Following the same theoretical analysis than in (17), the average energy consumption for this algorithm is given by,

$$E_{MCS} = CR^2 \sum_{i=1}^{M-1} 2^{M-3-2i} \cdot (2^i - 1) \quad (19)$$

4.1.3 Inverted Merged Capacitor Switching Scheme (IMCS)

The Inverted Merged Capacitor (IMCS) switching scheme in [20] is a variation of the previous technique to minimize the sensitivity to the parasitic capacitances at the comparator inputs and signal dependence of charge injection. To achieve this goal, the comparator input is reset at the sampling phase with an extra cycle, called inversion phase in Fig. 18, to eliminate the dependence on the parasitics in this net. After this cycle, the conversion

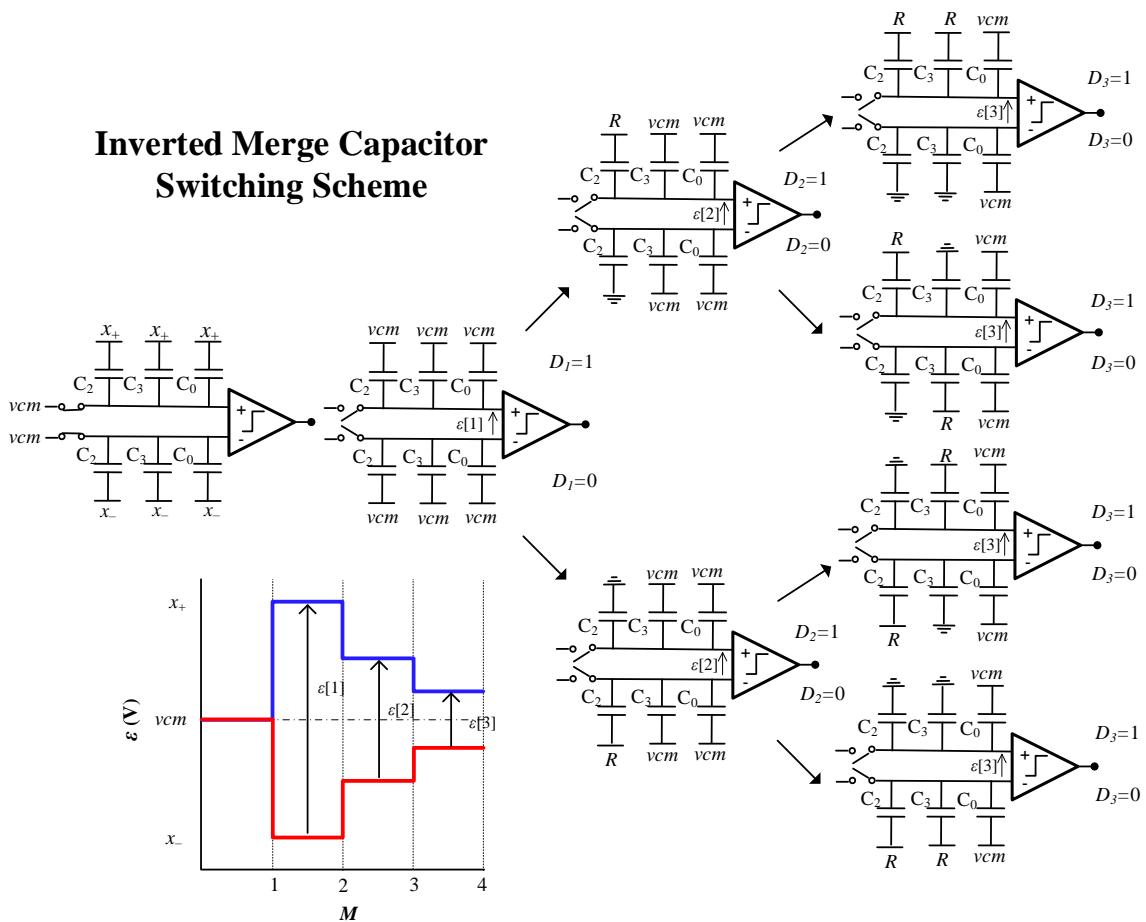


Fig. 18 Inverted merged capacitor switching scheme and voltages excursions for a 3 bit SAR ADC

proceeds is the same than in Section 4.1.2 considering that the switch actuation is inverted. That is: if $D_i = 1$, the largest capacitor in the positive (negative) array is settled to R (GND), and vice versa.

4.1.4 Monotonic Switching Algorithm

This algorithm was presented in [1] as a solution to reduce the energy consumption in the conversion process using a pseudo-differential strategy. This scheme samples the input signal as in Section 4.1.2, but the capacitors bottom plates are connected to R in both branches. The first comparison is performed directly on the sampled voltage at the comparator input, and therefore, this technique could be sensitive to its non-linear parasitic capacitance. According to the comparator output, if $D_1 = 1$, then C_2 is connected to ground in the negative branch, keeping the same capacitor in positive branch connected to R.

As shown in Fig. 18, the voltage at the positive array is always decreased monotonically, minimizing the power consumption associated to the bit commutation. Thus, the expression

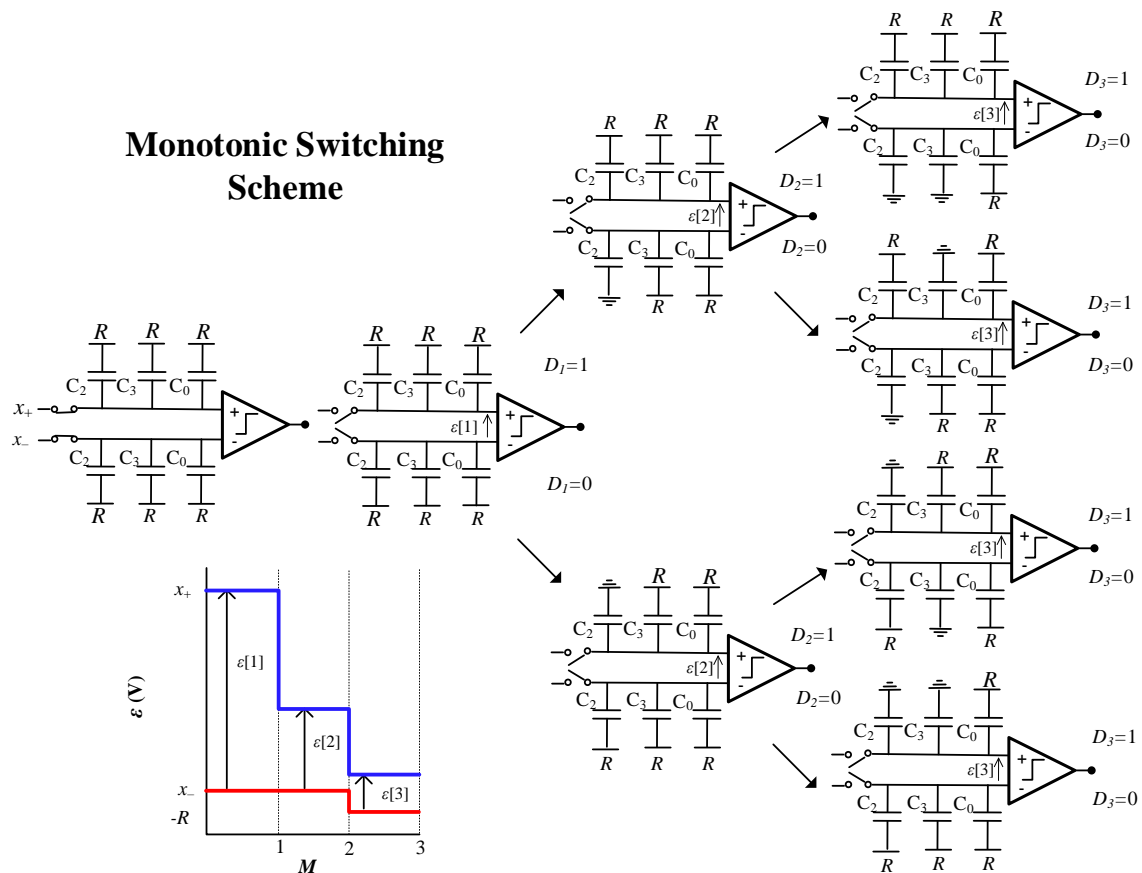


Fig. 19 Monotonic switching scheme and voltages excursions for a 3 bit SAR ADC

for the average consumption becomes:

$$E_{monotonic} = CR^2 \sum_{i=1}^{M-1} 2^{M-2-i} \quad (20)$$

In spite of its power efficiency, this algorithm has the drawback related with different values at the comparator input in the first and final cycle, and therefore, being indicated for relatively low effective resolution.

4.1.5 Other Switching Schemes

The search for other switching schemes, trying to improve the accuracy, speed, energy consumption in the CDAC, is very intense and various jobs have been reported in the last years [1], [20], [33]–[36]. The work in [34] presents a switching scheme, called split-capacitor switching scheme, to solve the problems of the monotonic approach with the unbalanced energy consumption in the transition from R to GND. This is effectuated splitting the largest capacitor into a sub-capacitors array. This sub-array is connected to R in the first cycle while the remaining capacitors are connected to GND. A modification of previous method is proposed in [35] called energy-saving switching algorithm which connect all bottom plates to GND in the first cycle and only the transition to R depending the comparator output is done. In [36] a new method called detect-and-skip switching scheme (DAS) is developed. The DAS scheme tries to anticipate the largest capacitor switch decision, when the input is small, to further reduce power consumption.

4.1.6 Switching Energy Consumption Comparative

This section presents a comparative of the most relevant switching schemes in the state-of-the-art to obtain an intuitive view of the different algorithms in terms of power consumption. Fig. 20 shows mean energy consumption depending on the number of processing steps M . In this figure, MCS and IMCS schemes are able to achieve the highest energy efficiency. The method proposed in [36] cannot be evaluated in a closed-form because its consumption depends on the input signal.

Giving the advantages in terms of switching activity, the merged capacitor switching (MCS) presented in 4.1.2 is selected as the default switching scheme in the case studies herein presented. The reasons that have motivated this choice are: 1) drastic reduction of consumption with respect to the other schemes considered, 2) elimination of the most significant capacitor (it only requires $M - 1$ capacitors) with the consequent advantages in terms of area.

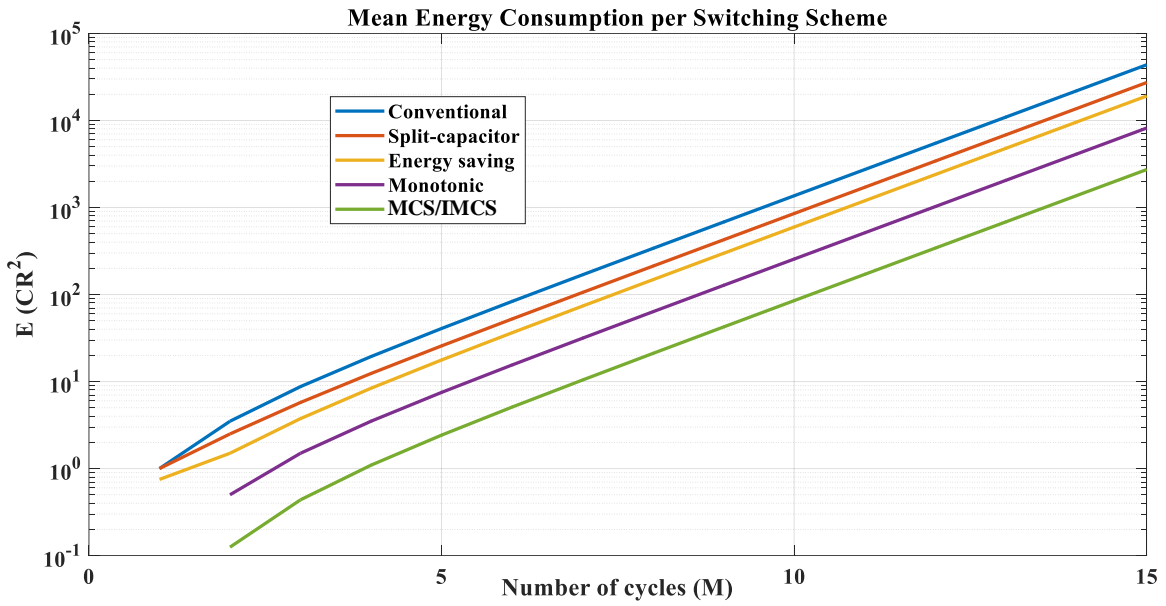


Fig. 20 Comparative of power consumption between switching algorithms.

4.2 CDAC SIZING AND ARCHITECTURE

Once selected the switching scheme, in this section we are going to determine the capacitor scaling factors according to the redundancy scheme in section 3.2.3 with $N = 12$ and $M = 15$. The proposed design process starts from the capacitor scaling factors without redundancy for a 12-bit implementation:

$$\mathbf{p}' = [2^{11}, 2^{10}, 2^9, 2^8, 2^7, 2^6, 2^5, 2^4, 2^3, 2^2, 2^1, 2^0] \quad (21)$$

Then, using the expressions in section 3.1, one of the scaled factor is binary decomposed, e.g.: $2^{10} = (2^9 + 2^8) + (2^7 + 2^6 + 2^5 + 2^4) + (2^3 + 2^2 + 2^1 + 2^0) + 1$, and its contribution distributed among the array, in the form:

$$\mathbf{p} = [2^{11}, (2^9 + 2^8), 2^9, 2^8, (2^7 + 2^6 + 2^5 + 2^4), 2^7, 2^6, 2^5, 2^4, (2^3 + 2^2 + 2^1 + 2^0), 2^3, 2^2, 2^1, 1, 2^0] \quad (22)$$

being the capacitors size given by,

$$C = [768, 512, 256, 240, 128, 64, 32, 16, 15, 8, 4, 2, 1, 1]C \quad (23)$$

where the unitary capacitor is $C = 5 \text{ fF}$, and notice that the most significant capacitor C_1 is omitted.

With this selection, the remaining aspect in the architectural description of the CDAC is the topology of the data multiplexer dedicated to set the different voltages at the bottom plates in the capacitors as a function of the stored comparator outputs. According to the MCS scheme in section 4.1.2, if the comparator output is “1” (“0”) in a specific processing phase, the associated capacitor must be connected to GND (R). Fig. 21 shows the details of the proposed multiplexer implementation to allow this task in the positive branch (the results for the negative branch are complementary). This block receives the information from the output of the comparator, D , and according to the following table defines the voltage at the bottom plate of the capacitor (bottomcap), in the form:

<i>clkph</i>	CLKS	Bottomcap
1	1	<i>vcm</i>
1	0	$\bar{D} \cdot R$
0	1	<i>vcm</i>
0	0	<i>vcm</i>

where *vcm* is the common mode.

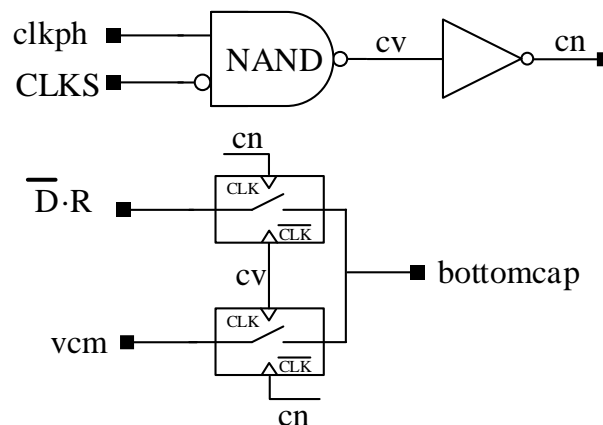


Fig. 21 Data multiplexer implementation in the CDAC.

4.3 TEMPORIZATION IN THE SAR LOGIC: SYNCHRONOUS VS ASYNCHRONOUS

The CDAC switches and the comparator have to be controlled by a digital logic that sets the clock phases, which control: 1) the sampling process, 2) the comparator phase, 3) the CDAC data multiplexer operation at each conversion cycle.

This control can be synchronous [37] when an external clock sets all the mentioned operations, or asynchronous if the comparator decides when the next cycle starts. Asynchronous implementation [1] is more suitable for medium-high speed implementations, since self-temporization optimizes the available time in each step. This control the asynchronous operation the comparator generates a signal (*valid*) when the output is valid, i.e. when the decision is complete. This allows the sampling signal (CLKS) to be set to the minimum time that maximizes conversion speed.

In [37], a synchronous implementation that combines phase generation and memory to store the raw code in *D*-type Flip Flops (DFF) during the conversion process was proposed. This structure, shown in Fig. 22, has some speed problems due to the activation of the clocks in the storage register, which can cause delays and loss of information when the clock edges arrive too close in time.

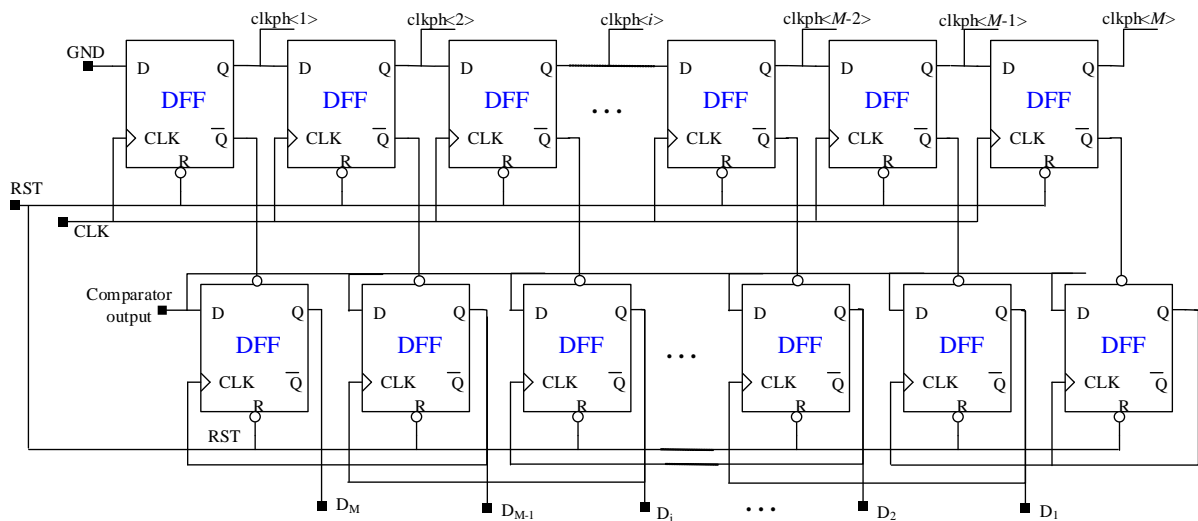


Fig. 22 Implementation of phase generator and register in a synchronous SAR ADC used by [37].

To overcome this drawback, the diagram of an asynchronous phase generator and control logic in Fig. 23 can be used [1]. In this scheme, the *D*-type Flip Flops (DFF) array which generates the different phases (*clkph<i>*) is controlled by the rising edge of the *valid* signal when the comparison in each step is resolved.

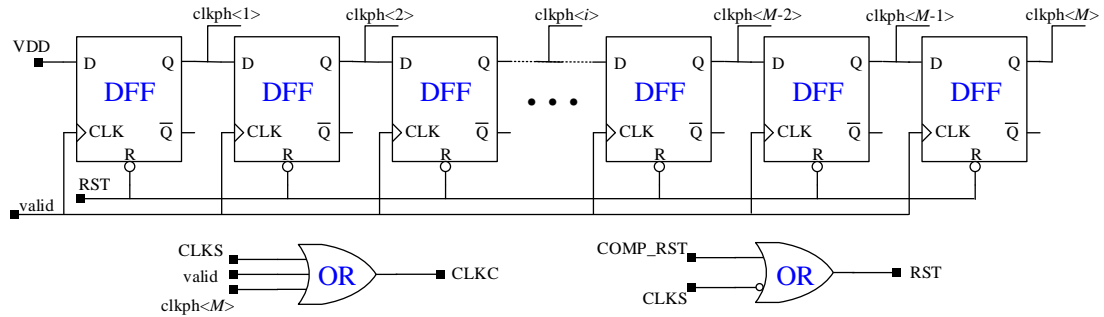


Fig. 23 Diagram of the implementation of the control logic and phase generator in the SAR ADC.

According to the scheme, in Fig. 24 the internal clock phase generation is shown. The *valid* signal will present a variable pulse width depending on the comparator decision time. This signal is generated by a NAND gate connected to the comparator outputs which triggers the SAR logic when comparison takes place, that is, the two outputs of the comparator are opposite.

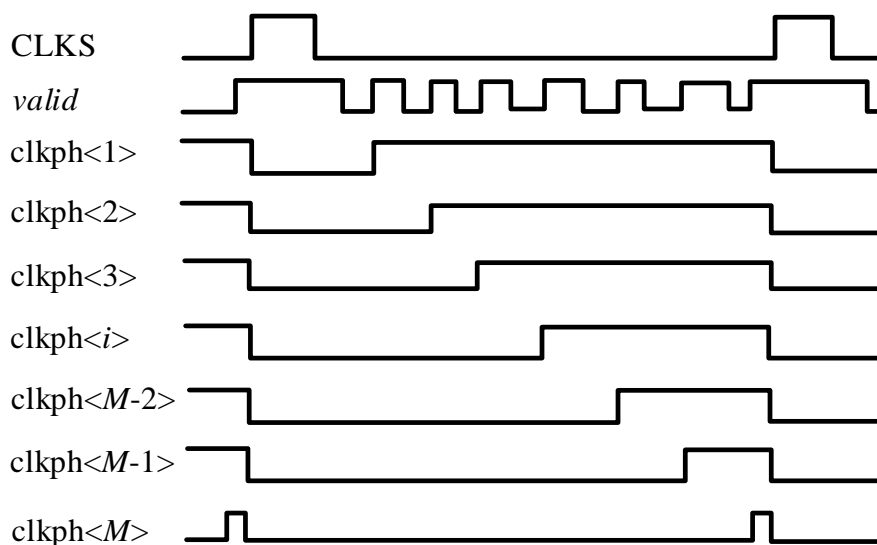


Fig. 24 Clock phases in an asynchronous implementation of SAR ADC.

4.4 ELECTRICAL VERIFICATION OF THE CASE STUDY

This section presents the electrical verification results for the considered case study: a 1.8V 12-bit 10MHz SAR ADC with 3.6Vpp input range with three extra redundant bits for dealing with conversion errors ($N=12$ and $M=15$). As commented before, the design considers a fully differential topology based on the merged-capacitor architecture in section 4.1.2 using macro-models for switches, logic and comparators with realistic values for the logic delays and signal dependent comparator errors. This case study can be considered as the initial description and verification at the architectural level for a future integration in a 180nm CMOS process. In case of need, the results herein obtained can be easily adapted to other technological nodes.

The contents in this section are distributed as follows. In Section 4.4.1, some details on the modeling and verification strategy are drawn. Section 4.4.2 presents the simulations results of the case study including the dynamic characterization of the topology in term of effective number of bits. These results has been done entirely within the design Framework II environment from Cadence[®]. Finally, in section 4.4.1 a discussion of the maximum frequency of operation in the asynchronous SAR ADC implementation is presented.

4.4.1 Modeling and Verification Strategy

The verification of the demonstrator has been done using a hierarchical approach in which the main building blocks in the structure were described at relatively low-level. These include:

- Low-level implementation of the CDAC with macro-models of switches, circuit implementation of the data multiplexer. The logic gates in the multiplexer were realistic modelled using verilog-A to speed up simulations.
- Low-level description of the asynchronous scheme in Fig. 23, where all the logic gates in its implementation (DFF, NAND, OR, etc.) were also modeled in verilog-A.
- Functional description of digital correction logic and comparator.

As example, the behavioral model of the comparator incorporates two steps: firstly, when comparator control signal (CLKC) goes up, the two outputs are reset to “1”. Then, a delay for the decision is incorporated depending exponentially on the input amplitude [38]. The transient dependence of the output becomes:

$$\Delta v_{out_i}(t) = \Delta \varepsilon_i \cdot e^{t/\tau_L} \quad (24)$$

where $\Delta \varepsilon_i$ is the differential voltage at the comparator input, t is the elapsed time, and τ_L is the time constant intrinsic to comparator structure.

Considering that the output is established when the differential voltage is above the midrange, the elapsed time until this value is obtained as,

$$t_p = \tau_L \ln \left(\frac{(R - GND)}{\Delta \varepsilon_i} \right) \quad (25)$$

4.4.2 Simulation Results

This section presents some simulations results of the case study once the architecture and models were debugged using a hierarchical approach. Fig. 25 shows some details on the control signals associated to the asynchronous implemented temporization. The figure includes all clock phases, the comparator control signal (CLKC), and external reset signal

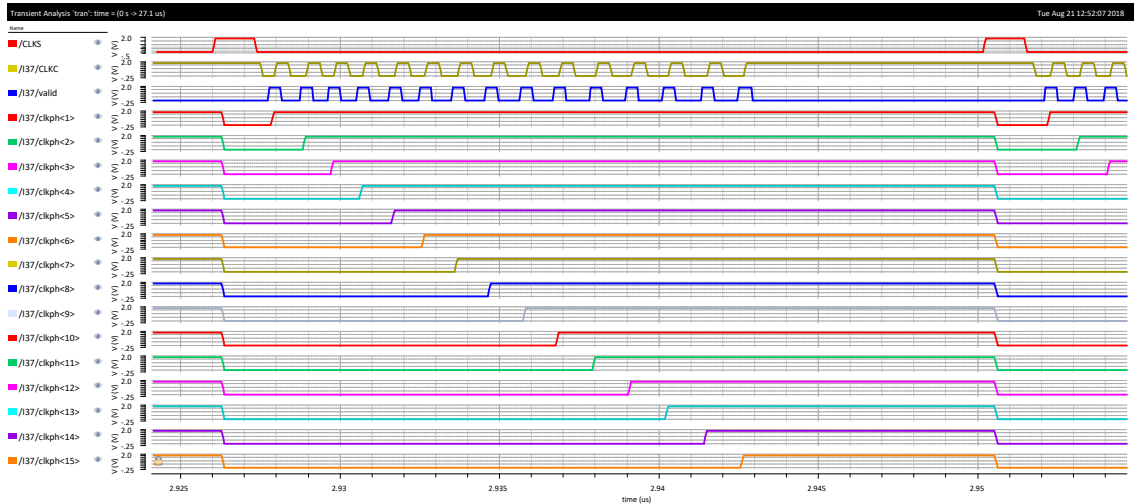


Fig. 25 Clock Phases in SAR ADC.

(CLKS) during two conversion cycles. We can see that there is a total agreement with the expected ideal behavior in Fig. 24.

To characterize the ADC, it is necessary to analyze the digital output response in the frequency domain. To carry out this, a Fast Fourier Transform (FFT) is done. Fig. 26 shows the output spectrum of this simulation. From the spectrum, the SNDR in dB units can be calculated, as a figure of merit to determine the quality of the ADC, as follows:

$$SNDR(dB) = 10 \cdot \log_{10} \left(\frac{P_{f_1}}{\sum_{\forall f_i \neq f_1}^{f_n} P_{f_i}} \right) \quad (26)$$

where P_{f_1} is the power of the main harmonic in the spectrum, and $\sum_{\forall f_i \neq f_1}^{f_n} P_{f_i}$ is the sum of the power corresponding to all other frequencies.

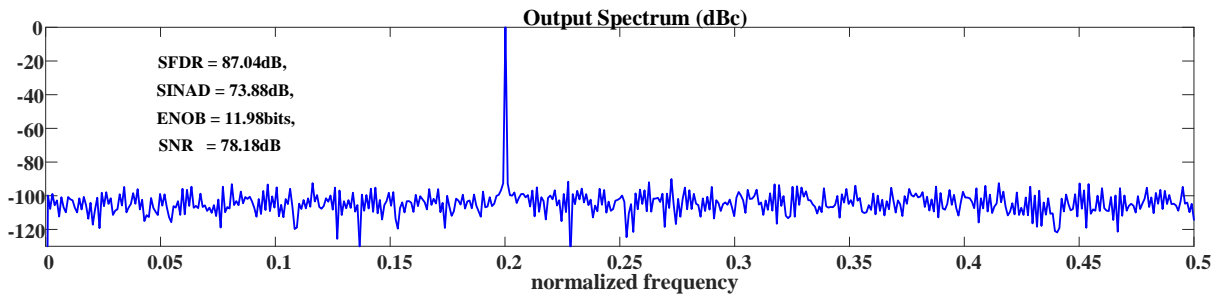


Fig. 26 Output spectrum of a 12-bit 10Msps SAR ADC with 2MHz input signal.

With the previous measurement, the Effective Number of Bits (ENOB) is evaluated in the form:

$$ENOB(bits) = \frac{SNDR - 1.76}{6.02} \quad (27)$$

As expected for an ADC with redundancy, the ENOB is not affected by the errors in comparison and the ENOB achieves almost the ideal 12 bit-level.

4.4.1 Analysis of Operation Speed in Asynchronous SAR ADCs

To conclude the analysis of the case study, a analysis of the maximum operation frequency is addressed. As can be observed in Fig. 25, the conversion process finishes 7.71ns before a new cycle of CLKS starts. This means that the frequency of CLKS can be incremented. To obtain an estimation of the maximum increment, it is necessary to evaluate the required time to complete all the steps in worst case conditions. Notice if this limit is exceed, as is shown in Fig. 27, the conversion cycle ends prematurely and the last conversion phase is erroneously eliminated, producing a faulty behavior of the SAR ADC.

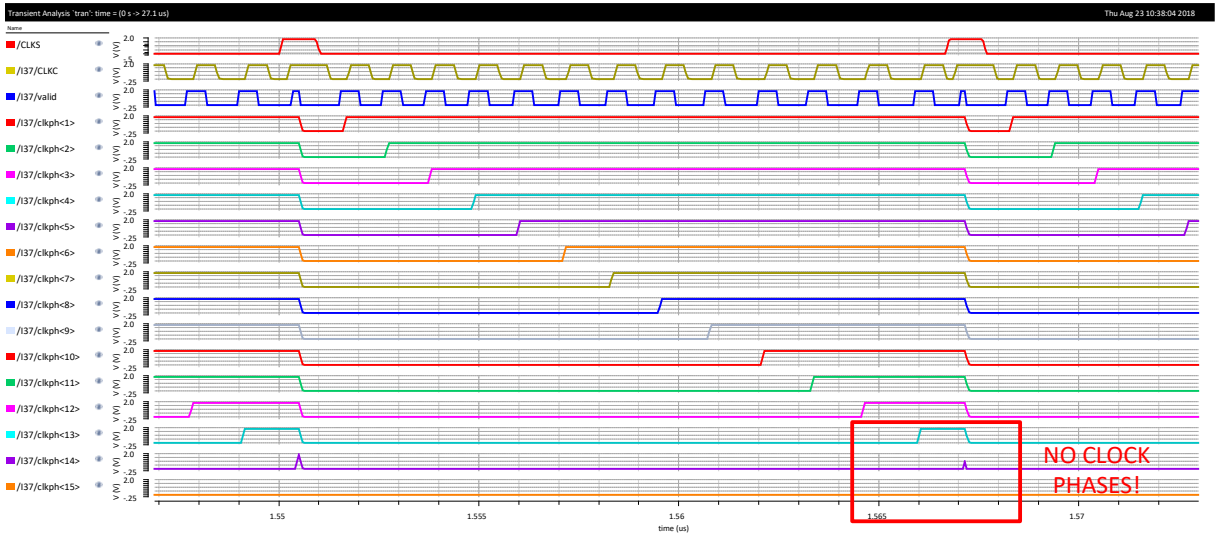


Fig. 27 Excessive CLKS frequency in SAR ADC.

Taking into account the worst case conditions for settling, as shown in Fig. 28, a theoretical expression of the minimum time spent per conversion step is derived, in the form:

$$T_{cycle} = t_{CLKS_u} + \sum_{i=1}^M t_{ph,i}, \text{ where } t_{ph,i} = t_{set} + t_{comp,i} + t_{hold} \quad (28)$$

where t_{set} comprise the delays associated with the logic and the time that spend the comparator in reset phase, t_{comp} is the comparator time depending on the input amplitude, t_{hold} is the time required by the SAR logic after the valid signals is triggered.

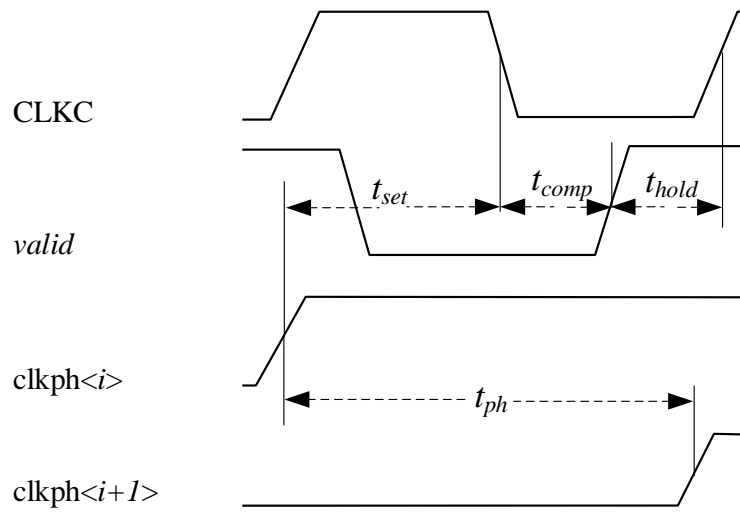


Fig. 28 Spent time per clock phase.

5 REDUNDANCY TECHNIQUES IN SAR ADCS BASED ON SPLIT-CAPACITOR DACS

This section generalizes the proposed unified description in Section 3 [14], [25] for SAR ADCs based on split-capacitor DACs (Split-CDACs). To improve matching and maximize performance, the design of SAR ADCs based on CDACs requires, as previously mentioned, using a common unit capacitance from which the rest of capacitances are derived [3], [20], [31]. The resulting scale factors can lead to large aspect ratios between devices for resolution above 8 bits. Actually, for a conventional N -bit case-study, as in the merged-capacitor topology [33], the most-significant bit (MSB) capacitor could be 2^{N-2} times greater than the least-significant bit (LSB) one. This ratio difference could become problematic due to technological issues (matching, noise, etc.), even making the design no feasible for high resolution.

To deal with this limitation, the Split-CDAC architecture [2], [13], [24], [28], [30], [39]–[41] divides the original CDAC into two or more arrays connected by bridge capacitances. This technique allows scaling the LSB section by a factor, making them higher, and more suitable for physical integration, since lower aspect ratios with respect to the MSB capacitors are achieved. The key point of this new type of structure lies on the equivalent LSB capacitance referred to the MSB array through a bridge capacitor. For this reason, the sizing of this capacitance is crucial for a correct conversion

In this work [28], we will analyze this effect proposing a general formulation of Split-CDAC SAR ADCs with closed-form expressions for the CDAC sizing. This formulation is suitable for conventional designs without redundancy, i.e. binary weighted CDAC with 2-radix correction logic as in [3], but it is also valid for designs with redundancy [13], based on an arbitrary selection of the weighting coefficients in the correction logic [20]. Explicit relationships of the impact of redundancy and bridge capacitance selections on the voltage excursion of the floating nets in the LSB array are derived. We will demonstrate that this excursion can be controlled, similarly that for the case without redundancy [30], using an extra limiting capacitor in the LSB array, the optimum value of which is theoretically derived.

5.1 PROPOSED UNIFIED DESCRIPTION FOR SAR ADC WITH SPLIT-CDAC

Fig. 29 shows a fully differential implementation of a SAR ADC with Split-CDAC. The topology has two sections, labelled MSB and LSB arrays, separated by the bridge capacitor C_s . It includes M different capacitors $\{C_i\}$ and an optional capacitor C_0 to control the full-scale (FS) range. The aim of the limiting capacitance C_x is related to controlling the excursion at the LSB array. Similarly than the classical CDAC, the analog input is sampled at the beginning of the conversion process in phase $\phi_{1,0}$ in both the MSB and LSB arrays. Then in each algorithm cycle, the comparator outputs D_i set the voltage at C_i , starting from the most significant, C_2 , to the least significant one, C_M . The SAR process must force the differential voltage at the comparator input ε to be below the N -bit quantization error at the end of conversion.

In the Split-CDAC case, the weighting coefficients W_i in (4) can be also related to the scale capacitor factor on the array with respect to the unitary capacitance C as in (5). To perform the sizing of the CDAC, let us define the index m , to indicate the position of the bridge capacitor C_s . This device separates the MSB and LSB arrays between C_m and C_{m+1} as shown in Fig. 29. To reduce the ratio between the two arrays, we introduce an arbitrary scale factor $k > 1$ in the coefficients p_i of the LSB capacitances in the form:

$$\begin{cases} C_i = p_i C & , i = \{2, \dots, m\} \\ C_j = k \cdot p_j C & , j = \{m+1, \dots, M\} \end{cases} \quad (29)$$

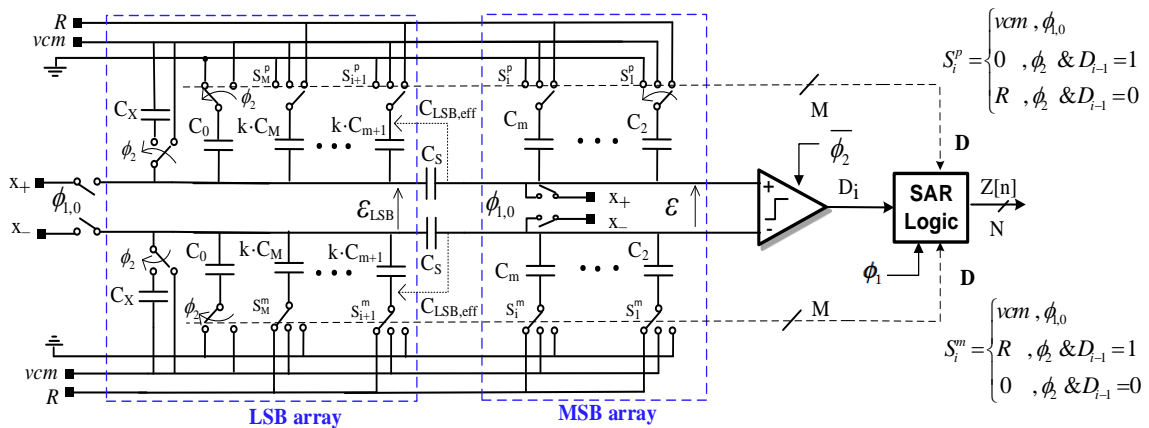


Fig. 29 Fully differential implementation of a SAR ADC with Split-CDAC. Phase $\phi_{1,0}$ is the initial sampling phase, and ϕ_2 is the ϕ_1 ' complementary phase.

Assuming that the total effective capacitance $C_{LSB,eff}$ of the LSB array referred to the MSB array is the actual C_{LSB} scaled down by the same factor k ,

$$C_{LSB,eff} \equiv \frac{C_s \cdot C_{LSB}}{C_s + C_{LSB}} = \frac{1}{k} C_{LSB} \quad (30)$$

the value of the bridge capacitor will be,

$$C_s = \frac{1}{k-1} \cdot C_{LSB} = \frac{k}{k-1} \cdot \left(\sum_{j=m+1}^M p_j + p_x + p_0 \right) \cdot C \quad (31)$$

where it has been used that $C_0 = k \cdot p_0 \cdot C$ and $C_x = k \cdot p_x \cdot C$. With these definitions and following the transient evolution in the Split-CDAC, similarly than in Fig. 9 for the no-split case in section 3.1, the final output code becomes:

$$z = 2^{N-1} + \sum_{i=1}^{m-1} (2D_i - 1) p_{i+1} + \sum_{i=m}^{M-1} (2D_i - 1) p_{i+1} + (D_M - 1) \quad (32)$$

Comparing (4) and (32) as it was done before, the digital weighting coefficients in the correction logic and offset term become:

$$\begin{aligned} W_i &= 2p_{i+1} \quad (i < M), \quad W_M = 1 \\ z_0 &= \left(2^{N-1} - \sum_{i=2}^M p_i \right) - 1 = p_0 - 1 \end{aligned} \quad (33)$$

leading to a general description suitable for Split-CDAC SAR ADCs without [30] and with redundancy [13], [41], as particularized in sections 5.2.1 and 5.2.2.

Analogously the expression for the transient evolution of differential voltage between floating nodes of LSB array results,

$$\begin{aligned} \varepsilon_{LSB}^{(n)} &= -\rho x + \mu Q_e \left(\frac{1}{k} \sum_{i=1}^{n-1} (2D_i - 1) p_{i+1} + k_t \sum_{j=m}^{n-1} (2D_j - 1) p_{j+1} \right) \\ &\quad , n \in [1, M] \end{aligned} \quad (34)$$

where, as conventionally, sums are null when super index are less than initial index, and the following parameters are used:

$$\begin{cases} Q_e = \frac{2R}{2^N} = \frac{R}{\mu C_t / C} \\ \mu = 1 - \frac{C_S C_x}{C_{LSB}^T C_t} = \frac{1}{1 + p_x / 2^{N-1}} \\ \rho = 1 - \frac{C_S C_x}{C_{LSB}^T C_t} \left(\frac{C_S}{C_{LSB}^T} + \frac{C_t}{C_S} \right) = 1 - (1 - \mu) \left(\frac{1}{k} + k_t \right) \\ k_t = \frac{C_t}{C_S} = \left(1 - \frac{1}{k} \right) \frac{1}{1 - \mu \cdot p_{MSB} / 2^{N-1}} \quad , p_{MSB} = \sum_{i=2}^m p_i \end{cases} \quad (35)$$

with total capacitances associated to SAR ADC and its MSB and LSB arrays given by,

$$\begin{aligned} C_t &= C_{MSB} + C_{LSB,eff} \\ C_{MSB}^T &= C_{MSB} + C_S \quad , C_{LSB}^T = C_{LSB} + C_S \end{aligned} \quad (36)$$

5.2 ANALYSIS OF SPLIT-CDAC SAR ADCS USING THE PROPOSED UNIFIED DESCRIPTION

5.2.1 SAR ADC with Binary-Weighted Split-CDAC

Similarly than for the non-split SAR ADC in section 3.1.1, in a Split-CDAC SAR ADC without redundancy, i.e. with a 2-radix codification, $W_i = 2^{N-i}$ in (31) ($N = M$), the digital output code z is obtained as the concatenation of the comparator output bits $z \equiv [D_1, D_2, \dots, D_N]$. Applying (33), the capacitor scale factors p_i results also binary weighted, $p_i = 2^{N-i}$. For the MSB array, this implies a binary scaling of the unitary capacitance C according to (29). For the LSB array, if k is selected as integer, the capacitors can be easily derived from a common C . Obviously, a trade-off in terms of matching is also present, since the factor k defines the bridge capacitances C_s in (31).

To show the generality of the proposed model formulation, let us consider a practical implementation of a binary weighted 1.8V 12-bit SAR ADC with $\mathbf{p} = [2^{11}, 2^{10}, 2^9, 2^8, 2^7, 2^6, 2^5, 2^4, 2^3, 2^2, 2^1, 2^0]$, null limiting capacitor ($C_x = 0$) and a full-scale $FS = 3.6V_{pp}$ ($R = 1.8V$). The parameters m and k in the Split-CDAC are 2^2 and 2^3 , respectively; that is, according to (29), $\mathbf{C} = [2^{10}, 2^9, 2^8, 2^{7+3}, 2^{6+3}, 2^{5+3}, 2^{4+3}, 2^{3+3}, 2^{2+3}, 2^{1+3}, 2^{0+3}]C$. With this selection, the bridge capacitor in (31) becomes $C_s = 292.57C$. At each conversion step, the output of the internal CDAC nodes can be evaluated according to (34).

Fig. 30 shows the voltage excursion in the end of conversion process as a function of the input signal. Notice that if C_x is not added to CDAC, the voltages ε_{LSB} can exceed the full-scale limits. This behavior could affect to the final resolution and reliability of the switches, since the margin for its correct operation is stressed. As we will analyze in section 5.3, the excursion of the LSB array voltages can be controlled, similarly than for the binary case [30] (but with some particularities), with the addition of capacitor C_x .

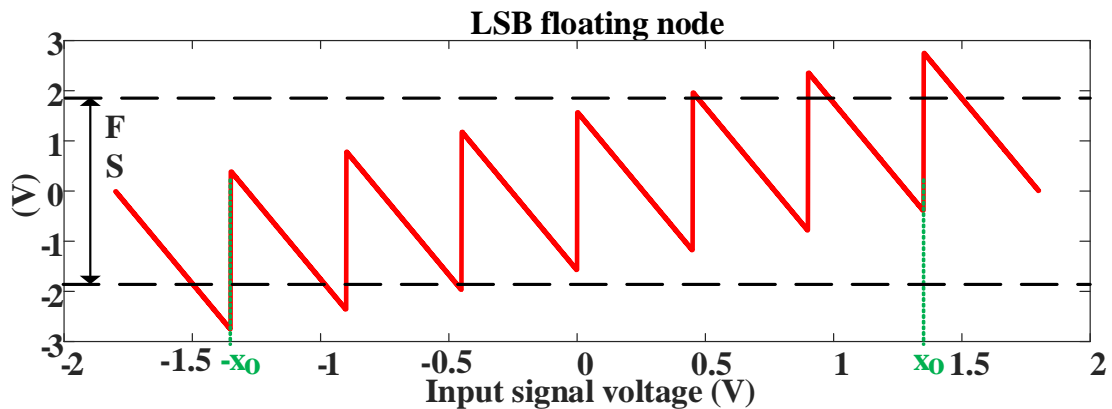


Fig. 30 Voltage excursion of the LSB floating node at the end of conversion process as a function of the input signal voltage in a binary 12-bit Split-CDAC SAR ADC with $m = 4$.

In addition to the excursion of the LSB, the design of split SAR ADC must assure a proper settling in the CDAC in all the steps of the algorithm. Actually, if an error in the comparator decision occurs due to incomplete settling (as well as signal dependent on resistance of switches and comparator noise), the output code z will not be correctly generated, as it was explained in previous sections. Fig. 31 shows the output spectrum of a full-scale sinusoidal input signal at 98% of the Nyquist's frequency when random time-variant uncertainty in the comparator decisions is considered. For sake of clarity, the rest of errors in the SAR ADC model are omitted. In spite of the model simplicity, we can observe a drastic degradation in the ENOB down to 9.02 bits (ideally 12 bits). The performance degradation can be justified analyzing the relationship between weights W_i in (33). If a comparator decision error occurs at the i -th cycle, a wrong additive term with value W_i will be included at the output code z in (4). This error cannot be compensated by the binary SAR algorithm without redundancy [14], [25], since again the maximum magnitude of the remaining contributions is lower than the added error, as shown in (12).

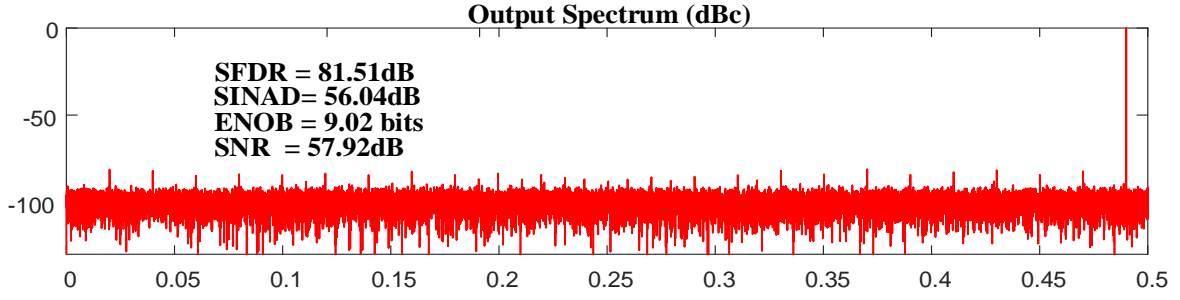


Fig. 31 Output spectrum of a 12-bit Split-CDAC SAR ADC case study with arbitrary weights and random comparator offset.

5.2.2 SAR ADC with Split-CDAC with Redundancy

The solution to the previous drawback is the inclusion of redundancy [2], [13], [33], [41]. As it was shown in section 3, the key concept in these techniques consists in adding extra conversion cycles in the SAR process ($M > N$) to compensate comparison mistakes at the SAR algorithm allowing a correct generation of the output code z in (4). To achieve this goal, a redundant-base codification is implemented satisfying the following condition,

$$W_i < \sum_{k=i+1}^M W_k \quad (37)$$

Actually, if a comparator decision error occurs at the i -th cycle, the magnitude of the error W_i is by definition lower than the sum of remaining weight factors, and therefore, the algorithm can recover the correct value. The maximum tolerable error e_i in the conversion is precisely given by the difference between these two terms, in the form:

$$e_i \leq -W_i + \sum_{k=i+1}^M W_k = -2p_{i+1} + 1 + 2 \sum_{k=i+2}^M p_k \quad (38)$$

Attending to this relationship, the amplitude measured in LSBs of the redundant interval $|e_i| \leq q_i$ will be given by,

$$\forall i \in [1, M-1], \quad q_i = -p_{i+1} + 1 + \sum_{k=i+2}^M p_k \quad (39)$$

Equation (39) in combination with (29) provides suitable design expressions for the Split-CDAC sizing. The design process can start with an *a priori* selection of the capacitor scale factors p_i , checking after that if the given redundant intervals for dealing with conversion errors are valid for the application. In the selection of scale factors p_i , we should consider according to (33) that in presence of redundancy, the range of codification could exceed the standard N -bit limits, i.e. $z \in [0, 2^N - 1]$. Evaluating (32) for the extreme values (e.g. when D_i are all logical ‘1’), the codification overrange, $z \in [-OR, 2^N - 1 + OR]$, can be evaluated as:

$$OR = -z_0 = 1 - p_0 \quad (40)$$

To validate the proposed Split-CDAC formulation, let us introduce a second 12-bit SAR ADC with three extra cycles for dealing with conversion errors ($N = 12$ and $M = 15$). According to the selected scale factors $\mathbf{p} = [2048, 872, 501, 288, 165, 95, 54, 31, 18, 10, 6, 3, 2, 1, 1]$, and the split parameters ($m = 4, k = 4, C_x = 0$), the capacitor sizes are determined as function of the unitary capacitance from (29), in the form: $\mathbf{C} = [872, 501, 288, 660, 380, 216, 124, 72, 40, 24, 12, 8, 4, 4]C$. With these values, according to (31) the bridge capacitance C_s becomes $516.00C$, the OR in (40) is 0, and the redundant intervals according to (14) are: $\mathbf{q} = [304, 174, 99, 57, 32, 19, 11, 6, 4, 2, 2, 1, 1, 0, 0]$. Fig. 32 shows the results for this case study. In the simulation, comparison errors are considered introducing random-variant offsets in the comparator with uniform distribution and amplitude equal to 65% of its redundancy interval. Thanks to redundancy, these errors are completely compensated (ideal ENOB = 12.0 bits). The voltage excursion at the end of conversion process is shown in Fig. 33. Similarly than in Fig. 30, the maximum voltage ranges exceeds the ADC full scale ($FS = 2R = 3.6V_{pp}$). We can observe, however, that due to redundancy the excursion is below the situation in the binary case ($3.8V_{pp}$ against $5.5V_{pp}$).

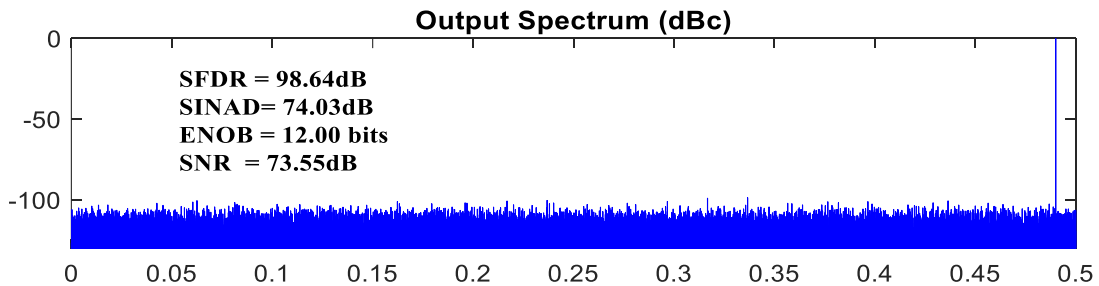


Fig. 32 Output spectrum of a 12-bit Split-CDAC SAR ADC case study with arbitrary weights and random comparator offset.

In the following section we will demonstrate that this behavior is completely general, i.e. the binary case is always more pessimistic.

5.3 LSB VOLTAGE EXCURSION LIMITATION

In the binary case, the characteristic of the voltage excursion ε_{LSB} at the LSB array, defined by (34), shows a segmented behavior. The extreme voltage excursion appears at in the first and last segments on last conversion cycle, $n = M$. In particular, the maximum and minimum voltages correspond to two levels of the input signal, labelled $\{-|x_o|, +|x_o|\}$ in Fig. 30, the value of which being related to number of bits in the MSB,

$$x_o = \mp R \pm \frac{2R}{2^{m-1}} = \mp \left(1 - \frac{1}{2^{m-2}}\right) R = \mp a \cdot R \quad (41)$$

where an exponent less than m , is related to the suppression of capacitor C_1 in the merged-capacitor topology [30].

The determination of the specific voltage excursion at these levels, $\varepsilon_{\text{LSB,peak}} = |\varepsilon_{\text{LSB}}^{(M)}(\pm x_o)|$ can be easily estimated with (34), since at these inputs, the digital code words are known. Specifically, the maximum and minimum values occur when codes are:

$$\begin{aligned} \text{for } +|x_o| &\rightarrow \mathbf{D} \equiv [(11\dots1 \underset{(m-1)}{1}) \parallel (\underset{(m)}{0} \ 0\dots 00)] \\ \text{for } -|x_o| &\rightarrow \mathbf{D} \equiv [(00\dots0 \underset{(m-1)}{0}) \parallel (\underset{(m)}{1} \ 1\dots 11)] \end{aligned} \quad (42)$$

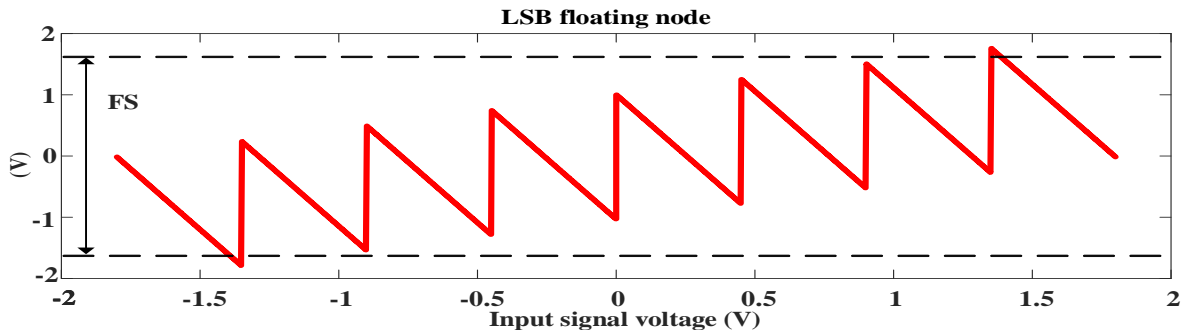


Fig. 33 Voltage excursion of the LSB floating node at the end of conversion process as a function of the input signal voltage in a 12-bit Split-CDAC SAR ADC case study with arbitrary weights and $m = 4$.

Due to symmetry, let us analyze in detail only one of the cases. Using (34) with (41) and (42) results:

$$\varepsilon_{LSB,Peak} = \rho a R + \mu Q_e \left(\frac{1}{k} (-p_{MSB} + p_{LSB}) + k_t p_{LSB} \right) \quad (43)$$

The case without overranging ($\varepsilon_{LSB,Peak} \leq R$) is evaluated now in in this general description:

$$\varepsilon_{LSB,Peak} = \rho a R + \mu Q_e \left(\frac{1}{k} (-p_{MSB} + p_{LSB}) + k_t p_{LSB} \right) \leq R \quad (44)$$

with $p_{LSB} = \sum_{j=m+1}^M p_j$

Solving (44) for the unknown p_x using definitions in (35), a theoretical approximation is obtained as follows:

$$p_x > a \cdot 2^{N-1} - p_0 - \left(a + \frac{1}{k} (1-a) \right) p_{MSB} \quad (45)$$

Particularizing the proposed procedure for the binary example in Fig. 30, we obtain that the voltage excursion on the LSB can be controlled ($\varepsilon_{LSB,Peak} \leq R$) with $C_x > 1080C$ ($p_x > 135$), with a final bridge capacitor of $C_s = 447.0114C$.

In the case with redundancy, the voltage excursion at the LSB array also shows a segment behavior as shown in Fig. 33, but the limits between segments are not equally distributed within the full scale, since they depend on the scale factors. However, as can be derived from (37), assuming the same number of bits in the LSB array, by the definition the total capacitance in the LSB array is greater than for the binary case, and hence its excursion is strictly lower. Therefore, the limit in section 5.2.1, particularized for the new \mathbf{p} selection, can be still used for the Split CDAC sizing as pessimistic scenario.

5.4 ELECTRICAL VERIFICATION OF THE PROPOSED FORMULATION

The proposed formulation has been satisfactorily validated by electrical simulations. As case study a 1.8V 12-bit 20MHz SAR ADC with 3.6Vpp input range and three extra cycles for dealing with conversion errors ($N=12$ and $M=15$) are considered (split parameters $m = 8$, k

= 32). The design considers a fully differential topology based on the merged-capacitor architecture in [33] using macro-models for switches, logic and comparators with realistic values for the logic delays, signal dependent comparator errors and switches resistors.

To simplify the hardware complexity of the correction logic, a binary decomposition of the scaling factors according [2] is implemented. The proposed design process starts with a selection of the capacitor scaling factors without redundancy: $\mathbf{p}' = [2^{11}, 2^{10}, 2^9, 2^8, 2^7, 2^6, 2^5, 2^4, 2^3, 2^2, 2^1, 2^0]$. Then, one of the scaled factor is binary decomposed, e.g.: $2^{10} = (2^9 + 2^8) + (2^7 + 2^6 + 2^5 + 2^4) + (2^3 + 2^2 + 2^1 + 2^0) + 1$, and its distributed among the SAR array, in the form: $\mathbf{p} = [2^{11}, (2^9 + 2^8), 2^9, 2^8, (2^7 + 2^6 + 2^5 + 2^4), 2^7, 2^6, 2^5, 2^4, (2^3 + 2^2 + 2^1 + 2^0), 2^3, 2^2, 2^1, 1, 2^0]$.

To conclude, the final capacitor sizes are determined according to the values of m and k as function of the unitary capacitance in the form $\mathbf{C} = [768, 512, 256, 240, 128, 64, 32, 512, 480, 256, 128, 64, 32, 32]C$ and $C_x = 1448.8C$ with $C = 5\text{fF}$. With these values, according to

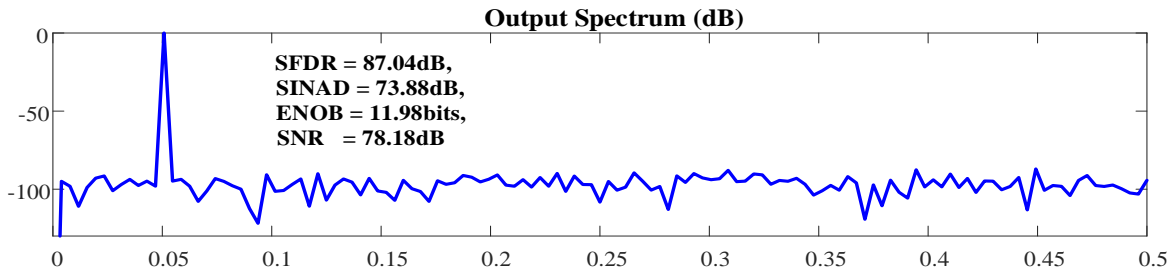


Fig. 34 Output spectrum of a 12-bit Split-CDAC SAR ADC in an electrical simulation with split capacitor redundant weights.

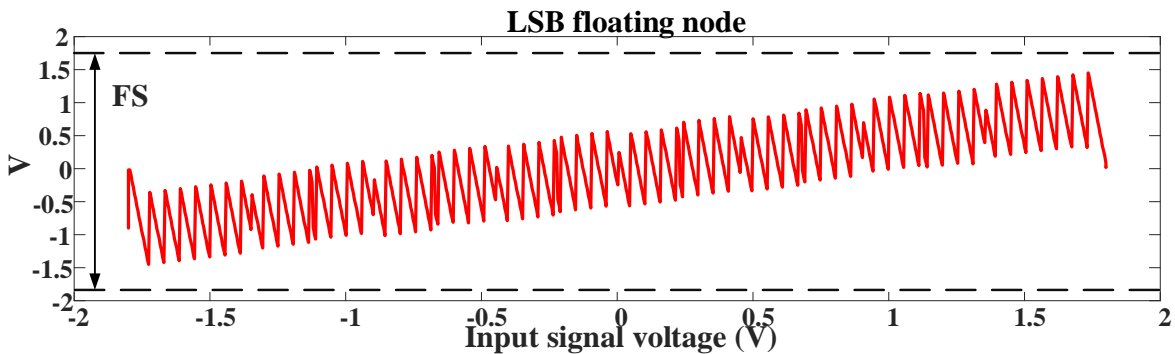


Fig. 35 Voltage excursion of the LSB floating node at the end of conversion process as a function of the input signal voltage in a 12-bit Split-CDAC SAR ADC in an electrical simulation with redundant weights and $m = 8$.

(31) the bridge capacitance C_s becomes $96.2823C$, $OR = 0$, and the redundant intervals according to (39) are: $\mathbf{q} = [512, 256, 256, 32, 16, 16, 16, 16, 2, 1, 1, 1, 1, 0, 0]$.

Fig. 34 and Fig. 35 show the output spectrum and dependence of the LSB excursion on the analog input in the same conditions. A total agreement with theoretical expressions (omitted due to space limitations) has been achieved.

6 CONCLUSIONS AND FUTURE WORK

This work analyzes the effect of redundancy in Successive Approximation Register (SAR) ADCs with charge-based DAC (CDAC) from both theoretical and practical point of views. A general hardware-based model formulation has been proposed with emphasis in its physical implementation which can be particularized, as demonstrated in the document, for the most relevant techniques in the state of the art. The proposed unified description differentiates between capacitor scale factors and binary weights in the digital correction logic, getting close to the physical implementation of the subtracting DAC. The proposed description is fully general (suitable for different switching schemes), and it can incorporate second order effects, such as mismatch between capacitors.

Based on this description, the redundancy concept, effects and implication have been illustrated through some simulation examples at behavioral and electrical levels in several case studies without and with redundancy considering both the non-split and split CDAC architectures. These analyses include:

- Theoretical study, modelling and simulation of different redundancy schemes including: arbitrary selection of weighting coefficients, extended binary codification and split-capacitor technique. These techniques are the most common in the bibliography.
- Evaluation of the dependence between the digital weights selection and the associated redundant intervals for dealing with comparison errors.
- Development of a guide procedure for the complete sizing of capacitors in the CDAC.
- In the case of the split CDAC architecture, a theoretical study of the voltage excursions in the CDAC arrays has been carried out without and with redundancy. Closed-form expressions suitable for design are derived to determine the bridge capacitance and the optimum limiting capacitor which avoids overranging in the LSB array to ensure that node voltages are kept into the ADC full-scale limits.

These aspects have been complemented with the analysis of other relevant aspects for physical ADC implementation and verification (modelling, simulation and characterization):

- Switching schemes: different switching schemes have been analyzed and compared in terms of energy consumption. This analysis has concluded that the switching schemes based on the merged capacitor approach are the most efficient.
- Synchronous vs Asynchronous SAR logic: SAR ADCs with synchronous timing, i.e. an external clock sets each conversion phase, are widely used in the literature. However, this approach presents certain problems since the operation frequency is upper limit by the greater delay in comparator for the worst case input amplitude. To overcome this drawback, an asynchronous implementation can be considered. This implementation allows the converter to automatically adjust its internal phases to increase the operating speed when it is possible. Taking into account the advantage of this solution, in this work the control logic and clock phase generation have been studied and designed for an asynchronous implementation.
- Modelling: to support the verification, several macro- and Verilog-A models have been developed for the basic building blocks in the SAR ADC, including comparator, switches and the SAR and digital correction logic.
- Characterization of ADCs: study of the characterizations methods for ADCs, including the evaluation of standardized dynamic (ENOB, THD, etc.) and static (INL,DNL) parameters. Based on this, several behavioral and electrical simulations have been done to verify the case studies.

FUTURE WORK

To conclude this report, a summary of the research aspects that will be contemplated as future work is provided below. These include:

- The analysis of existing calibration techniques for discerning the best approach for a future integration.
- A theoretical study of the impact of mismatch and noise in CDAC in the performance of the SAR ADC.
- The development of a design methodology which incorporates all the previous considerations.
- The validation of this methodology with a silicon demonstrator.

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