Using CAD Tools for the Automatic Design of Low-Power ΣΔ Modulators

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ABSTRACT - This paper illustrates the use of a CAD methodology to design a high-resolution 2nd-order ΣΔ modulator with optimized power consumption.The fabricated prototype in 0.7μm CMOS technology features 16.4-bit resolution at 9.6-kHz DOR and consumes only 1.71mW operating at 5-V power supply.[1]

1. Introduction

ΣΔ modulators (ΣΔM) have been demonstrated as basic building blocks for robust design of high-resolution interfaces in mixed-signal ASICs, taking advantage of their reduced analog content and large tolerance to the circuitry non-idealities [1]. ΣΔM-based A/D converters have widened their application range from instrumentation up to video frequencies [2]-[10], and today, they dominate the non-multiplexed ADC application for signal-bandwidth below 1MHz [11].

Table 1 summarizes the current state-of-the-art on ΣΔMs. The quality of each modulator is evaluated using a Figure-Of-Merit (FOM) proposed recently for A-to-D conversion ICs [12]. This FOM combines the resolution in bit, the digital output rate (DOR = sampling rate divided by M) and the power consumption of a ΣΔM as follows:

$$FOM = \frac{\text{Power (W)}}{2^{\text{resolution (bit)}} \times DOR(\text{Hz})} \times 10^{12} \qquad (1)$$

Because the size of modulator is usually much smaller than the size of the digital filter, the occupation area of the former is not considered in this expression. The FOM (in picojoules) is the energy needed per conversion. Table 1 includes the ΣΔMs with FOM smaller than 5 in the last six years. The smallest FOM corresponds to a 4th-order ΣΔM in a BiCMOS technology [2]. For 2nd-order single-bit modulators, the smallest FOM's are about 4pJ [7][8]. The first operates with only 1.5V supply to provide 12bit@6kHz using a 0.7μm CMOS technology. The second operates at 5V and obtains 16bit@50kHz.

Since at these performance edges the operation of ΣΔM is limited by non-idealities other than quantization (thermal noise, incomplete settling, finite opamp-gain, opamp non-linearity, mismatches, jitter, etc. [1]) a large wealth of knowledge and intensive optimization are required to map the high-level specifications of ΣΔMs into low FOM ICs. Both tasks result in large design cycles which often reduce the economic success of industrial mixed-signal ASICs.

To alleviate this problem a number of CAD tools and methodologies have been proposed during the last few years [3][13][14]. Unfortunately, only a few of these methodologies have been demonstrated through real working state-of-the-art prototypes. This paper uses the methodology proposed by the authors in [3] to design a 2nd-order ΣΔM whose measurements featured 16.4bit@9.6-kHz DOR with a FOM of only 2pJ. This modulator has been fabricated in a 0.7μm CMOS technology to be used as the front-end of an energy metering mixed-signal ASIC requiring to accomplish these specifications with minimum possible power consumption.

2. CAD Tools for the design of ΣΔMs

Fig.1 shows the operation flowgraph in the design of ΣΔM ICs. It comprises three different synthesis levels: (a) Modulator level: architecture selection and modulator sizing; (b) Cell level: topology selection and cell sizing; and (c) Layout level: full-custom layout of the modulator. In addition, supervisory simulations should be performed between each couple of levels – usually behavioral simulation between the modulator and cell levels; electrical simulations between the cell and layout lev-

Table 1: Summary of reported ΣΔ Modulators with FOM < 5

	# Bits	DOR (kHz)	Power (mW)	Process / Supply	Architecture	FOM (pJ)
Yin and Sansen 94 [2]	15.8	1500	180	2μm BiCMOS / 5V	Cascade 2-1-1	2.1
Medeiro et al. 95 [3]	14.8	160	10	1.2μm CMOS / 5V	Cascade 2-2	2.2
Nys, Henderson 96 [4]	19	0.8	1.35	2 μm CMOS / 5V	2nd-Order, 3bit	3.2
Rabii, Wooley 96 [5]	15	50	5.4	1.2 μm CMOS / 1.8V	Cascade 2-1	3.3
Yin et al. 93 [6]	15.7	320	65	1.2μm CMOS / 5V	Cascade 2-1	3.9
Peluso et al. 96 [7]	12	6	0.1	0.7μm CMOS / 1.5V	2nd-Order	4.1
Brandt et al. 91 [8]	16	50	13.8	1μm CMOS /5V	2nd-Order	4.3
Baird and Fiez 96 [9]	13.7	1000	58	1.2μm CMOS / 5V	4th-Order, 4bit	4.5
Brandt, Wooley 91[10]	12	2100	41	1μm CMOS / 5V	Cascade 2-1, 3bit	4.8

[1] This work has been supported by the European Union under ESPRIT Project 8795-AMFIS.

els and electrical simulation of the complete modulator including the extracted layout parasitics in the end of the design cycle.

The CAD methodology presented in [3] uses a set of dedicated tools to support the most time consuming activities related to the design of switched-capacitor ΣΔM ICs, namely:

- *Architecture Selection*: Depending on the modulator specifications, high-order and or multibit ΣΔMs with low oversampling ratio, or simpler architectures with larger M can be selected to minimize the power dissipation. This is realized with the help of a tool called SDOPT. This tool contains behavioral descriptions relating modulator performance specifications and design parameters for a large catalog of architectures, with single-bit and multi-bit quantizers.
- *Modulator Sizing*: The same tool is used to automatically obtain optimum specifications for the building blocks in accordance to the modulator specifications. This is done by combining detailed equations relating the circuit imperfections and the noise they introduce at the modulator output, and a statistical optimization algorithm based on simulated annealing.
- *Behavioral Simulation:* An advanced sigma-delta simulator (ASIDES) is used to validate the modulator sizing. This program incorporates a large number of building blocks (integrators, comparators, multibit quantizers, D/A converters, etc.) that can be combined in a netlist to define arbitrary modulator topologies. Each block can be considered ideal or defined by a detailed behavioral model that contemplates many of the non-idealities due to the circuit imperfections.
- *Cell Sizing*: A cell level optimizer (FRIDGE) enables the automatic sizing of the building blocks to fulfill their terminal specifications with minimum power dissipation and occupation area. This tool is based on electrical simulation and optimization.

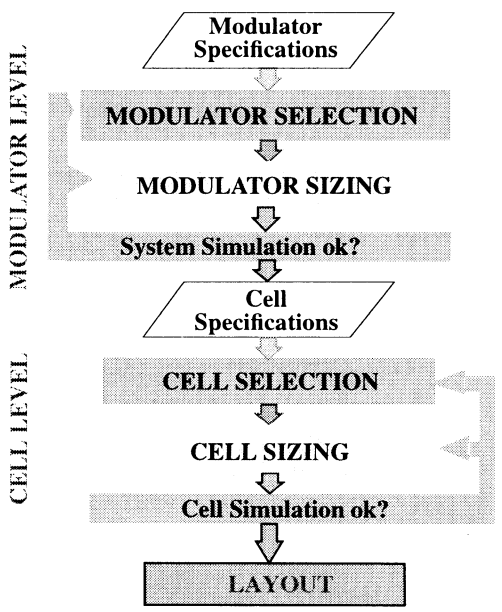

Fig. 1: Operation flow in ΣΔM design.

3. Architecture selection

At this level a set of simplified equations are used to evaluate the power consumption of available single-bit ΣΔM architectures. The benefit of multi-bit quantization regarding power consumption [4][9][10] is difficult to generalize due to the diversity of the techniques used to attenuate the influence of the DAC non-linearity and will not be considered here.

Let us consider three sources error at the modulator output: quantization, thermal noise and incomplete settling. Assume also that the incomplete settling noise power, P_{St}, is controlled to be well below the other error sources. Thus, for given resolution, b bit, the dynamic range (DR) is evaluated as

$$DR = 3 \cdot 2^{2b-1} = \frac{V_r^2/2}{P_Q + P_{Th}} \qquad (2)$$

where V_r represents the reference voltage (full-scale input) of the modulator; and P_Q and P_{Th} are the in-band power of quantization and thermal noise, respectively. The two noise powers in (2) can be approximated as functions of only three design parameters: modulator order, L, oversampling ratio M, and integrator sampling capacitor C_i,

$$P_Q \cong \frac{(2V_r)^2}{12} \frac{\pi^{2L}}{(2L+1)M^{2L+1}} \qquad P_{Th} \cong \frac{kT}{MC_i} \qquad (3)$$

where k is the Boltzman constant and T is the absolute temperature. Note that in (3) quantization noise has been supposed to be an additive white noise and that the thermal noise of the first integrator has been considered dominant as compared to the other integrators in the modulator loop [1]. Using (2) and (3) it is possible to calculate a lower bound for the sampling capacitor for given DR, M, and L. An absolute lower bound must be imposed regarding layout requirements. Once C_i is known, the equivalent load of the first integrator opamp is evaluated as

$$C_{eq} \cong C_i + C_p + C_l\left(1 + \frac{C_i + C_p}{C_o}\right) \qquad (4)$$

where C_p and C_l are the parasitics at the opamp input and output respectively, and C_o is the feedback capacitor of the SC integrator. All these capacitors can be related to C_i. To accomplish the previous assumption $P_{St} \ll P_Q, P_{Th}$ the unity gain frequency of the opamp, given approximately by $g_m/(2\pi C_{eq})$, must be large enough as to provide a good settling of the integrator output voltage. For instance we can choose $g_m/(2\pi C_{eq}) = 10 f_S$, where f_S represents the sampling frequency. This expression can be used to estimate the transconductance needed in the opamps.

At this point, one more assumption is needed to estimate the power consumption: Let be the opamp a folded-cascode OTA with the same current, I_B, flowing through the differential pair, through the output branches and through the biasing stage. Thus, the total current spent by one opamp is $4I_B$. The current I_B depends on the required g_m as $I_B = g_m^2/(2\beta)$, where β is the transconductance parameter of the input transistors. Once the tail current per opamp has been estimated, the static power can be calculated as

$$P_{WS} = 4I_B V_{supply} L \quad (5)$$

On the other hand the dynamic power dissipated to commute a capacitor C_i between the reference voltages can be approximated by $P_w = (2V_r)^2 C_i f_S$. Using fully-differential circuitry there are 6 commuting C_i per integrator (assuming $C_o = 2C_i$). Thus, the dynamic power of the analog part of a Lth-order modulator can be approximated by,

$$P_{WD,\,\text{analog}} = 6L(2V_r)^2 C_i f_S \quad (6)$$

In addition the dynamic power of the modulator digital part (quantizer, flip-flop and gates) has to be taken into account. However, that power strongly depends on the number of quantizers in the modulator as well as on the specific circuitry used to implement them. As a gross approximation we shall use the following expression:

$$P_{WD,\,\text{digital}} = 10N \cdot 5\text{mW}\,(1\text{ns}) f_S \quad (7)$$

where N denotes the number of quantizers (latch + flip-flop + small logic), each of them with 10 equivalent inverters commuting with a power peak of 5mW within 1ns. The value of N depends on the modulator architecture: It is one for single loop modulators and larger for cascade modulators. We will suppose a value $N = L/2$.

These equations have been included into the ΣΔM sizing tool, SDOPT, and used to estimated the FOM of several single-bit ΣΔMs architectures, from $L = 2$ to $L = 6$ to achieve 17bit@10-kHz DOR. The results are given in Fig.2. Note that the lowest FOM is featured by the 2nd-order loop with oversampling ratio close to 300. According to these results, the 2nd-order single-loop ΣΔM of Fig.3 with oversampling ratio equal to 256 was selected.

4. Switched-capacitor implementation

The modulator has been implemented using fully-differential SC circuits. Asides its robustness, this technique provides good suppression of the common-mode interferences. The integrator weights have been selected to minimize the required output-swing (OS) and speed of the two integrators. By using $g_1 = g_1' = g_2' = 0.25$ and $g_2 = 0.5$, the voltage swing at the integrator output is reduced so that the OS can be clipped at only the reference voltage, instead at twice the reference voltage as required using the clas-

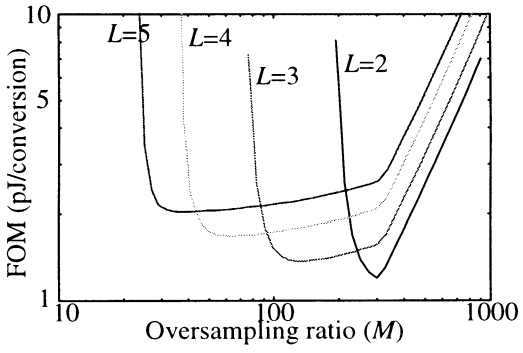

Fig. 2: Estimated FOM to obtain 17bit @10-kHz DOR

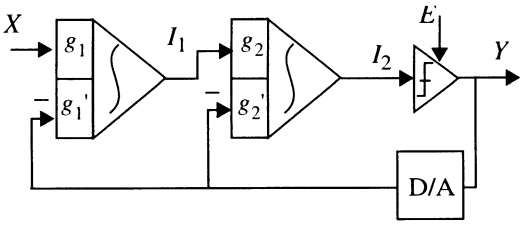

Fig. 3: Block diagram of the 2nd-order ΣΔM

sical choice $g_1 = g_1' = g_2 = g_2' = 0.5$. Fig.4 shows the SC fully-differential second-order ΣΔM. Note that the opamp of the first integrator includes a chopper compensation technique to cancel its offset and low-frequency noise. The second integrator has two branches to implement two different weights g_2 and g_2'. This is not necessary in the first integrator where the weights of the input and feed-back paths are the same. Modulator timing consists of two non-overlapped phases, two delayed versions of them used to avoid signal-dependent feed-through errors, and chopper phases.

The specifications for the building blocks and other design parameters at the modulator level have been calculated using SDOPT obtaining the values shown in Table 2. The reference voltages has been set to ±1.5V (differential value) to have a margin respect to the maximum modulator input signal which equals 1V. The power of noise and distortion contributions in the baseband are given in the end of the Table 2. Note that the incomplete settling noise is the dominant error source – the transconductance and output current of the opamp have been chosen as low as possible to minimize the power consumption. Other noise

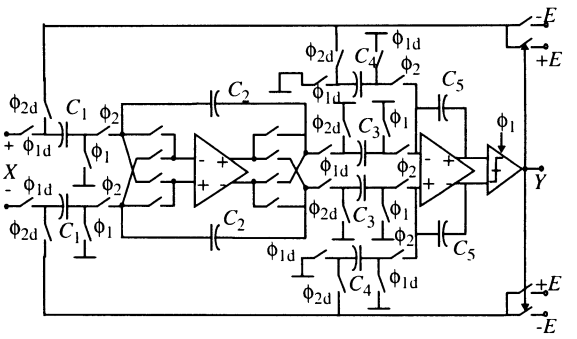

Fig. 4: SC fully-differential 2nd-order ΣΔM

sources, including quantization, have approximately the same influence. The total inband noise power referred to the full-scale input leads to a *DR* of 98.3dB which is large enough to ensure more than 16-bit effective resolution.

Table 2: Modulator sizing results

Specs		value
	Topology	2nd-order
	Sampling frequency (MHz)	2.46
	Oversampling ratio	256
	Reference voltages (V)	±1.5
	C_1, C_3 (pF)	1
	C_2 (pF)	4
	C_4 (pF)	0.5
	C_5 (pF)	2
	Capacitor non-linearity (p.p.m.)	≤ 50
	MOS switch-ON resistance (kΩ)	2.0
	Maximum clock jitter (ns)	≤ 2.0
	DC-gain (dB)	≥ 66
	DC-gain non-linearity (V^{-2},%)	≤ 20
	Transconductance (μA/V)	196
	Maximum output current (μA)	≥ 30
	Total output swing (V)	≥ 4.0
	Input noise density (nV/sqrt(Hz))	≤ 20
	Parasitic input capacitor (pF)	≤ 0.2
	Hysteresis (mV)	≤ 70
	Resolution time (ns)	≤ 50
Resolution & Noise power contributions		
Dynamic range: 98.3dB (Equivalent to 16.04bit)		
Quantization noise:		-108.7dB
Thermal noise:		-107.1dB
Incomplete settling noise:		-99.3dB
Jitter noise:		-118.1dB
Harmonic distortion:		-107.0dB

Behavioral simulations have been performed using ASIDES to validate the modulator sizing. In these each basic block is described through a model containing the non-idealities obtained from SDOPT. Fig.5 shows the output spectrum of the modulator and its signal-to-(noise+distortion) ratio (SNDR) as a function of the input amplitude. These results confirm the correctness of the specifications for the building blocks.

Since the maximum output current and the DC-gain requirement are not very demanding, a single-stage class-A amplifier is preferred. In particular, the fully-differential folded-cascode architecture of Fig.6 has been selected for the opamps that form the integrator core. A nmos-input topology is preferred to a pmos-input as long as flicker noise is not relevant (provided that chopper is activated) and white noise is. The opamp core is formed by transistors M_1 to M_{11} while the biasing stage comprises transistor M_{12} to M_{14}. A low-distortion current steering common-mode feedback net (CMFB) has been used (transistors M_{15} to M_{24}) [15]. This architecture has been

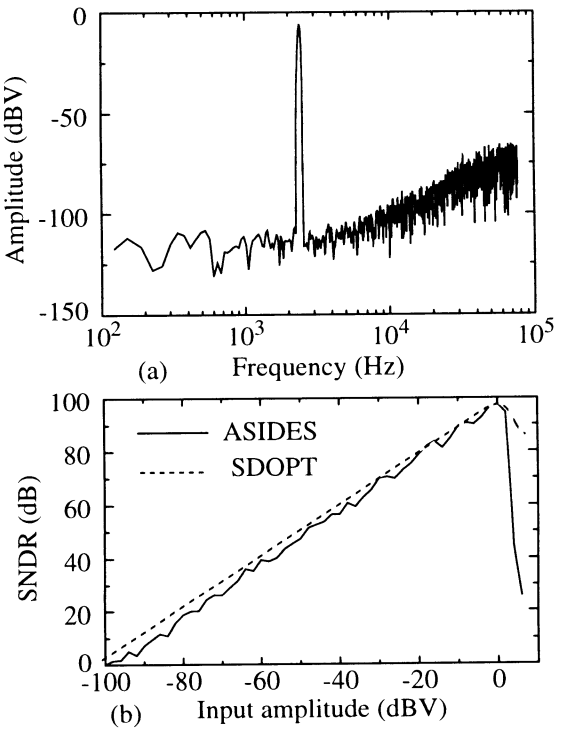

Fig. 5: Behavioral simulations: (a) Output spectrum for a 0.5-V@1.2-kHz input. (b) SNDR vs. input level

automatically sized using FRIDGE to fulfill the specifications of Table 2 within a temperature range of [-25°, 85°] and for power supply range of [4.75V, 5.25V], which after 25min. CPU-time provided the sizes displayed in Table 3. *Ibias* was set to 30μA.

Table 4 summarizes the simulated and measured performance. Measurements correspond to the average value in eight samples of the opamp prototype.

Table 3: Sizes for the opamp (in microns)

Trans.	W/L	Trans.	W/L
$M_{1,2}$	70.5/2	M_{14}	2/4
$M_{3,4}$	15.8/2	M_{15}	15/2
M_5	37/2	M_{16}	37.2/2
$M_{6,7}$	20.5/2	$M_{17,18}$	2/4.5
$M_{8,9}$	78.8/1.2	$M_{19,20}$	2/4.5
$M_{10,11}$	78.8/1.2	$M_{21,22}$	37.2/2
M_{12}	5/5	$M_{23,24}$	15/2
M_{13}	5/5	M_{25}	37.2/2

Table 4: Summarized performance of the opamp

Specs.	Sim.	Meas.	Unit.
DC-gain	85.1	80	dB
gm	196	210	μA/V
GB (1.2pF)	20.7	-	MHz
PM (1.2pF)	70	-	Degree
Input noise	17	-	nV/√Hz
OS	5	5	V
Output Current	30	-31,29.2	μA
Supply current	127	129	μA

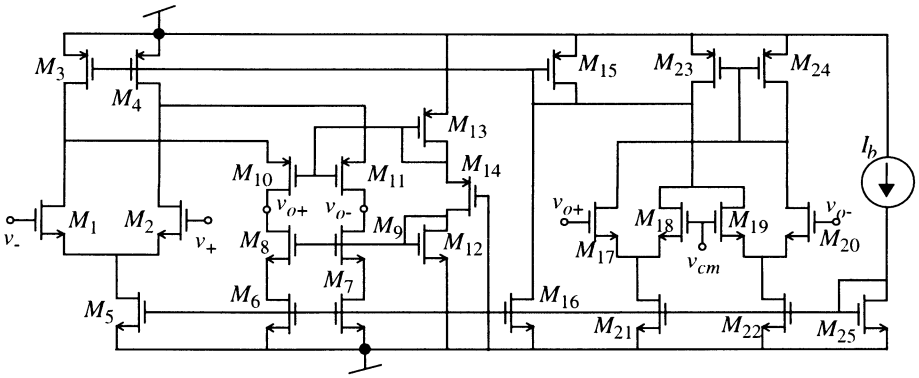

Fig. 6: Fully-differential folded-cascode OTA

Since the hysteresis requirement is not very demanding while the resolution time is (see Table 2) a regenerative latch (Fig.7) is selected for comparator core. This is activated in phase ϕ_1 and a nor-gate SR flip-flop (not shown) is provided to hold the output data during the phase ϕ_2. The latch has been sized using FRIDGE to fulfill the specifications in Table 2. Sizes, obtained after 10min. CPU-time, are displayed in Fig.7. The simulation results are shown in Table 5. Measurements (also shown in Table 5) present a minor deviation in the hysteresis which does not degrade the modulator performance.

Table 5: Summarized performance of the comparator

Specs.	Sim.	Meas.	Unit.
Hysteresis	0	28	mV
Offset	-10	-27	mV
Resolution time	9	9.4	ns

5. Experimental results

The 2nd-order ΣΔM has been integrated in a 0.7μm CMOS single-poly technology. The full-custom layout, which was done manually, incorporated techniques to minimize the coupling of the switching noise through the substrate [16].

Fig.8 shows a microphotograph of the modulator prototype which presents an active area of 0.42mm^2 and consumes 1.71mW from a 5-V power supply. A two-layer board was fabricated to measure the performance of the modulator [17] with separated analog and digital ground planes, decoupling capacitors and

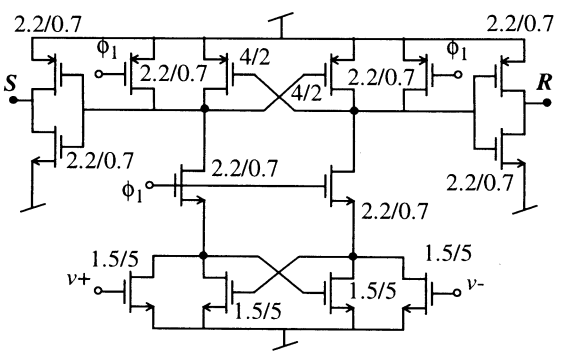

Fig. 7: Regenerative latch used in the comparator

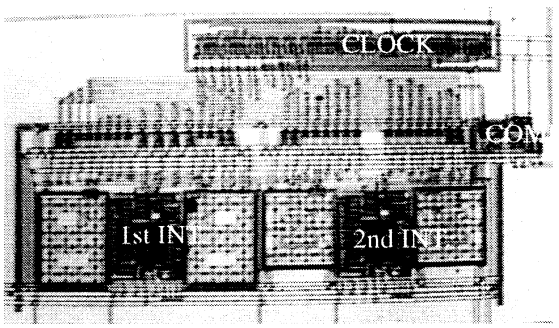

Fig. 8: Microphotograph of the second-order ΣΔM. The clock phase generator is also shown

signal filtering, to attenuate the switching noise in the analog signal and biasing traces. The modulator was evaluated using a high-quality fully-differential programable input signal source (THD <-100dB). A digital data acquisition system was used to generate the clock signal and to acquire the serial modulator output at the clock rate. Data were acquired automatically by controlling the test set-up with proprietary *C* routines and transferred to a workstation to perform the decimation filtering using MATLAB. Fig.9(a), shows the modulator output spectrum for 0-dBV@1.25-kHz input tone. Note that the noise floor is flat (-115dBV) and no large noise patterns are observed. Fig.9(b) shows the output spectrum with no input with chopper enabled and disabled.

Fig.10 shows the SNR and SNDR for an input tone of 1.25kHz and M = 256 as a function of the input level. *DR* is over 100dB with a SNR-peak of 94.2dB corresponding to 1.2-V input and a SNDR-peak of 91.8dB for 0.8-V input. Measurements of *DR* vs. M for given clock rate, see Fig.11, show that for M = 256 the modulator is just on the limit between the quantization noise limited region (slope=15dB/octave) and the white noise limited region (3dB/octave) – a consequence of the dominance of the incomplete settling noise. The modulator performance is summarized in Table 6 for three oversampling ratios M =128, 256 and 512. Note that, for the nominal value of M = 256, the FOM of the modulator is only 2pJ/conversion which is lower than those

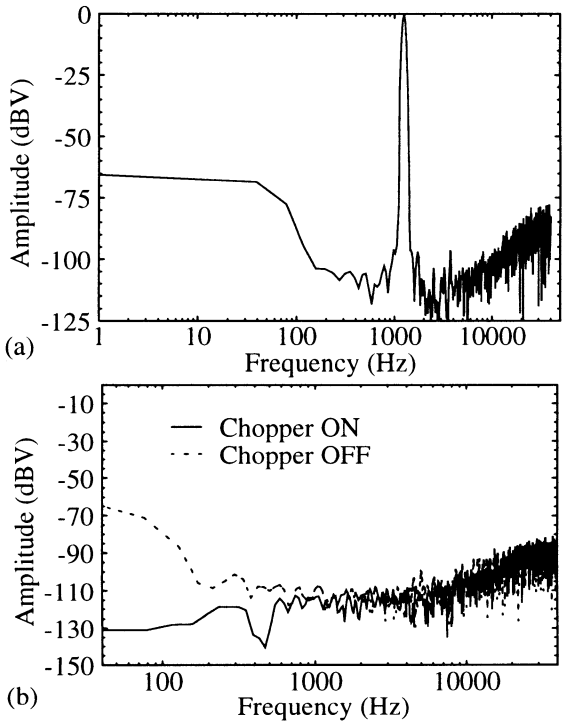

Fig. 9: Measured ouput spectrums: (a) for 0-dBV@1.25-kHz input and chopper off; (b) with no input and chopper off/on

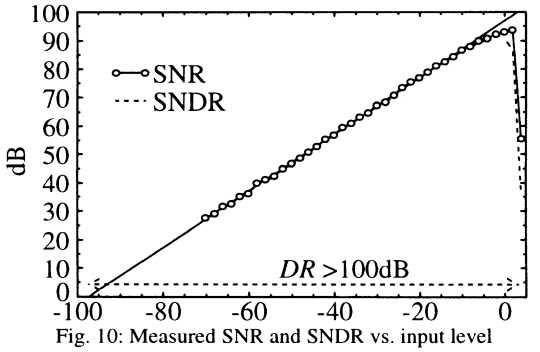

Fig. 10: Measured SNR and SNDR vs. input level

in Table 1. However the FOM increases for the two other values of M. This means that the modulator has been optimized for the nominal oversampling ratio and, although it is possible to obtain better resolution with higher values of M, the FOM increases as well.

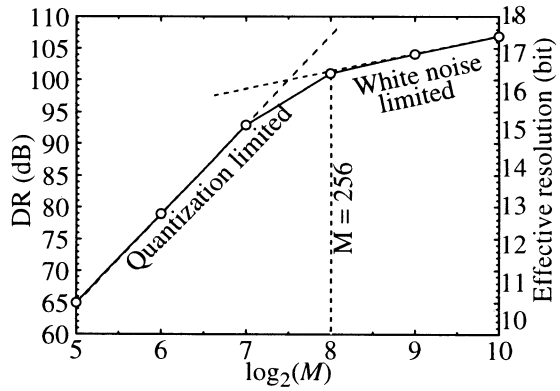

Fig. 11: Measured dynamic range vs. oversampling ratio

6. Conclusions

A 2nd-order ΣΔM featuring 16.4-bit at 9.6-kHz DOR has been fabricated in 0.7μm CMOS technology. The use of CAD tools which include optimization issues in the synthesis tasks has enabled the reduction of the power comsumption of the modulador to only 1.71mW. This perfomance places the fabricated prototype between those with smallest FOM reported to now.

Table 6: Summarized performance of the ΣΔM

	M=128	M=256	M=512	Unit
Resolution	15	16.4	17.1	bit
DR	92	100.2	105	dB
SNR-peak	84.4	94.2	101	dB
SNDR-peak	84.3	92	99	dB
DOR	19.2	9.6	4.8	kHz
Power	1.71			mW
Active area	0.42			mm^2
FOM	2.7	2.0	2.5	pJ

7. References

[1] J. C. Candy and G. C. Temes (editor): *Oversampling Delta-Sigma Data Converters*. New-York, IEEE Press 1992.

[2] G. Yin and W. Sansen: "A High-Frequency and High-Resolution Fourth-Order ΣΔ A/D Converter in Bi CMOS Tech.". *IEEE J. of Solid-State C.*, Vol. 29, pp. 857-865, August 1994.

[3] F. Medeiro, B. Pérez-Verdú, A. Rodríguez-Vázquez and J. L. Huertas: "A Vertically-Integrated Tool for Automated Design of ΣΔMs", *IEEE J. of Solid-State C.*, Vol 30, pp. 762-772, July 1995.

[4] O. Nys and R. Henderson: "A Monolithic 19bit 800Hz Low-Power Multi-bit ΣΔ CMOS ADC using Data Weighted Averaging". *Proc. ESSCIRC96*, pp. 252-255, September 1996.

[5] S. Rabii and B. A. Wooley: "A 1.8V 5.4mW, Digital-Audio ΣΔM in 1.2μm CMOS", *in Proc. IEEE ISSCC96*, pp. 228-229, 1996.

[6] G. M. Yin, F. Stubbe and W. Sansen, "A 16-bit 320kHz CMOS A/D Converter using 2-Stage 3rd-Order ΣΔ Noise-Shaping", *IEEE J. of Solid-State C.*, Vol.28. pp.640-647, June 1993.

[7] V. Peluso, M. Steyaert and W. Sansen: "A Switched Opamp 1.5V-100μW ΣΔ Modulator with 12 bits Dynamic Range", *Proc. ESSCIRC96*, pp. 256-259, September 1996.

[8] B. P. Brandt, D. W. Wingard and B. A. Wooley: "Second-Order Sigma-Delta Modulation for Digital-Audio Signal Acquisition", *IEEE J. of Solid-State C.*, Vol. 23. pp. 618-627, April 1991.

[9] R.T. Baird and T.S. Fiez: "A Low Oversampling Ratio 14-b 500KHz ΔΣ ADC with a Self-Calibrated Multibit DAC". *IEEE J. of Solid-State C.*, Vol. 31. pp. 312-320, March 1996.

[10] B. F. Brandt and B. A. Wooley: "A 50-MHz Multibit ΣΔ Modulator for 12-b 2-MHz A/D Conversion", *IEEE J. of Solid-State C.*, Vol. 26, pp. 1746-1756, December 1991.

[11] E.J. Swanson: "Analog VLSI Data Converters - The First 10 Years". *Proc. ESSCIRC95*, pp. 25-29, Sept. 1995.

[12] F. Goodenough: "Analog Technologies of all Varieties Dominate ISSCC". *Elec.Design*, Vol. 44, pp. 96-111, February 1996.

[13] H. C. Chang, E. Felt and A. Sangiovanni-Vicentelli: "Top-down constraint-driven design methodology based generation of a second-order ΣΔ-A/D converter", *Proc. IEEE CICC95*, pp. 25.5.1-15.5.4, 1995.

[14] M. F. Mar and R. W. Brodersen: "A Design System for On-Chip Oversampling A/D Interfaces", *IEEE Trans. on VLSI Systems*, Vol. 3, pp. 345-354, September 1995.

[15] J. F. Duque-Carrillo: "Control of the Common-Mode Component in CMOS Continuous-Time Fully Differential Signal Processing", *Analog Circuits and Signal Processing*, Vol. 4, pp. 131-140, 1993.

[16] Y. Tsividis: "*Mixed Analog-Digital VLSI Devices and Technology*", MacGraw-Hill, New York 1996.

[17] J. L. LaMay and H. J. Bogard: "How to Obtain Maximum Practical Performance from State-of-the-Art Delta-Sigma Analog-to-Digital Converters", *IEEE Trans. on Instrumentation and Measurements*, Vol. 41, pp. 861-867, December 1992.

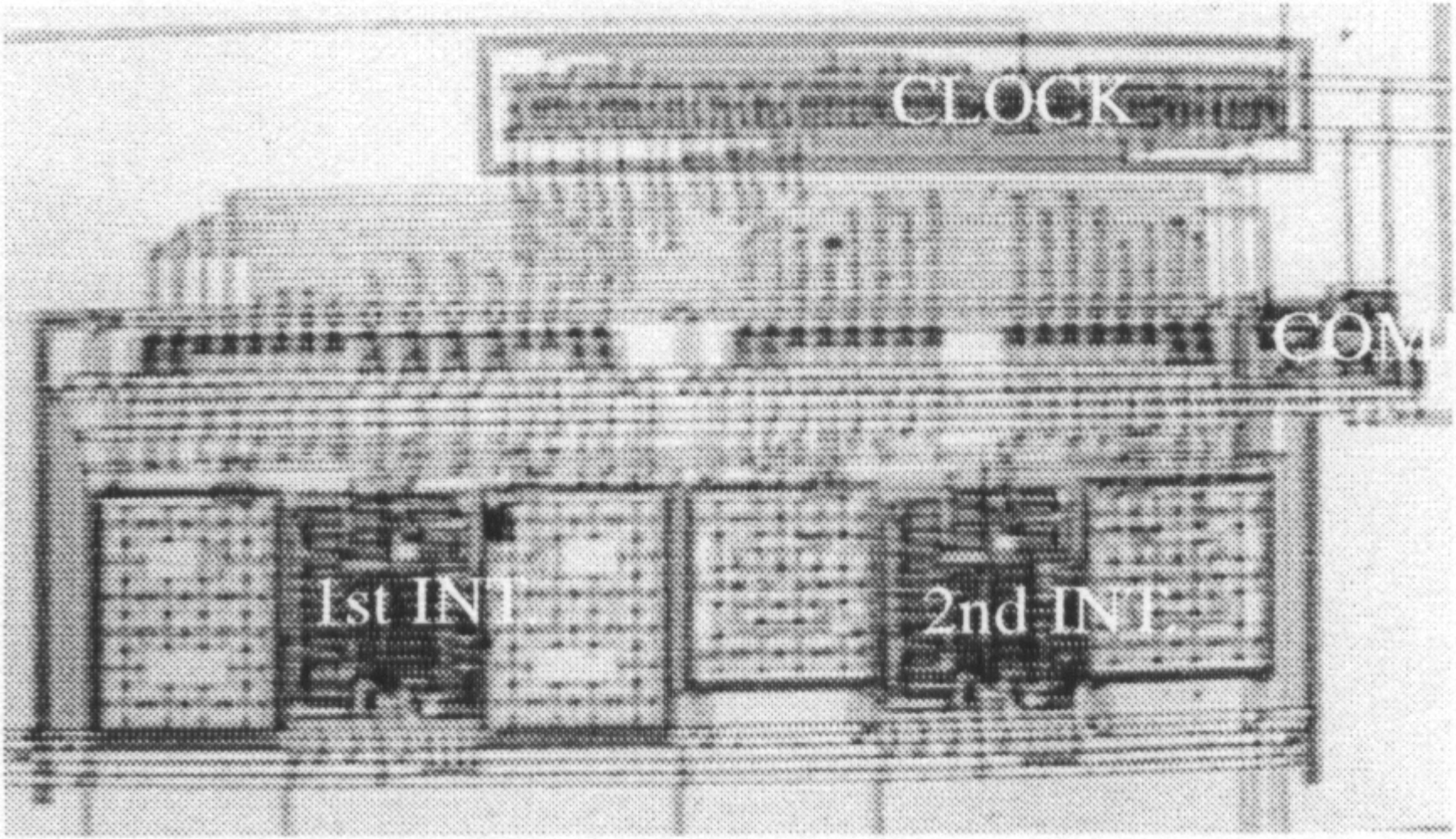

Fig. 8: Microphotograph of the second-order ΣΔM. The clock phase generator is also shown