Harmonic Distortion in Fully-Differential Switched-Current Sigma-Delta Modulators

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Abstract

This paper presents a systematic analysis of the harmonic distortion in ΣΔ modulators (ΣΔMs) implemented with fully-differential switched-current (SI) circuits. Closed form expressions are derived for the third-order harmonic distortion in both lowpass and bandpass ΣΔMs. For the latter, the third-order intermodulation distortion is also deduced. Time domain behavioral simulations validate our approach.(*)

1. Introduction

The trend towards the realization of mixed-signal systems on chip has motivated exploring analog design techniques compatible with standard, digital CMOS technologies. This is the case of switched-current circuits (SI) [1], which during the last ten years have been used for different analog functions, including filtering [2] and A/D conversion [3]. Particularly, several SI ΣΔMs have been reported, for lowpass signals [4] [5], as well as for bandpass signals [6].

Performances reported to date for SI ΣΔMs are lower than for state-of-the-art SC ΣΔMs [7]. For instance, [5] obtains 13-bit for lowpass voice band signals, while [6] obtains 9-bits for bandpass signals in the AM bandwidth. Among other reasons, such lower performances are motivated by larger influence of SI non-idealities, as compared to SC ones, and by incomplete modeling of their influence [8][9][10][11]. Particularly, harmonic distortion is recognized as one of the most important SI performance-degrading nonlinearities.

Error mechanisms responsible for harmonic distortion include: threshold voltage mismatch, non-linear finite output-input conductance ratio, charge injection, and settling error. Their influence on memory cell distortion has been analysed elsewhere [8][9]. However, only the charge injection error analysis has been extended to lowpass SI ΣΔMs [10]. Based on the harmonic distortion analysis of SI blocks, this paper presents closed-form equations for third-order distortion coefficients of SI integrators, resonators and both lowpass and bandpass ΣΔMs. The analyses presented here have been validated by time-domain behavioral simulations [11] and are illustrated through results pertaining to the harmonic distortion due to charge injection and non-linear output-input conductance ratio.

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2. Non-linear modeling of the memory cell operation

Fig.1 shows a simple, second-generation memory cell. Ideally, the output current is a half-delayed inverted version of the input †

$$i_{o,n} = -i_{i,n-1/2} \tag{1}$$

According to [1], its main non-idealities are: finite output-input conductance ratio error (represented by ε_g), incomplete settling error (ε_s), charge injection error (ε_q) and thermal noise. In the presence of these errors, the output current can be generically expressed as

$$i_{o,n} = I_{off} - (1-\xi_1) i_{i,n-1/2} + i_{th} + i_H(i_{i,n-1/2}) \tag{2}$$

where I_{off} stands for the offset current at the output, ξ_1 is the linear gain error, i_{th} is the thermal noise contribution and i_H represents the non-linearity.

We will assume that the memory cell reaches the steady state before the end of the sampling phase and, consequently, settling error ε_s will not be considered. Besides, thermal noise and offset current, will not be included in our analysis because they do not contribute to the harmonic distortion. Regarding i_H, it will be expressed as a polynomial function of the input current i_i [8][9]

$$i_H = -\sum_{k=2}^{\infty} \xi_k i_{i,n-1/2}^k \tag{3}$$

where ξ_k have different expressions for each error.

Taking into account the above considerations, expression (2) can be simplified into,

$$i_{o,n} = -(1-\xi_1) i_{i,n-1/2} - \sum_{k=2}^{\infty} \xi_k i_{i,n-1/2}^k \tag{4}$$

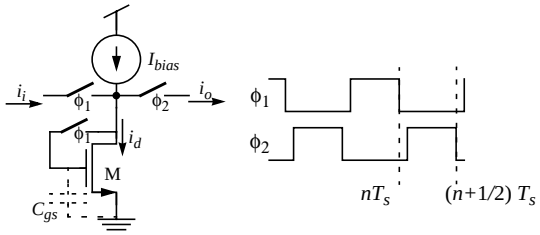

Fig. 1: Second-generation current memory cell.

†. We use the notation $i_{o,n}$ to represent $i_o(nT_s)$, where T_s is the sampling period.

For illustration purposes, Table 1 shows ξ_1, ξ_2 and ξ_3 when the memory cell is degraded by charge injection [9], and non-linear output-input conductance ratio error. For the latter, it has been assumed that the memory transistor transconductance depends on the input signal as $g_m = g_{mQ}\sqrt{1 + i_i/I_{bias}}$, with g_{mQ} being the operating-point transconductance. In Table 1, $(V_{gs} - V_T)_Q$ represents the quiescent excess overdrive voltage; V_{off} is the offset introduced by the charge injected; C_{sw} is the memory switch capacitance; g_{out} is the output conductance and A_V is the gain of the amplifier stage used either to reduce the output conductance (in regulated-cascode memory cells), or to increase the input conductance (in folded regulated-cascode memory cells). Note that $A_V = 1$ for the simple memory cell.

Assuming that the input current of the memory cell in Fig.1 is a sinusoidal signal of amplitude I_i, the output current will contain harmonics of the input signal frequency f_i. The k-order harmonic distortion, HD_k, is defined as the ratio of the output signal amplitude at frequency kf_i to the linear output amplitude. For our analysis, we will assume fully-differential memory cells. Thus, even powers of the input current in (4) can be considered negligible. On the other hand, assuming that the third-order harmonic is dominant, (4) can be simplified into

$$i_{o,\,n} \cong -(1-\xi_1)i_{i,\,n-1/2} - \xi_3 i^3_{i,\,n-1/2} \qquad (5)$$

In this case, the Total Harmonic Distortion (THD) is approximately equal to HD_3 and given by

$$THD \cong HD_3 = \frac{\xi_3}{4(1-\xi_1)} I_i^2 \qquad (6)$$

3. Harmonic distortion in fully-differential SI integrators

Fig.2 shows the schematic of a fully-differential LDI SI integrator. It is composed of two cells, and an output stage. In the following, it will be assumed that the operation of the memory cells is described by (5). Although these memory cells are simple, our analysis can be extended to enhanced memory cells – cascode, regulated-cascode or folded regulated-cascode – by conveniently changing the expressions of ξ_1 and ξ_3.

The operation of the integrator is as follows. After clock phase ϕ_1, which goes on for nT_s, the differential drain current of the memory cell 2, is given by

Table 1: ξ_1, ξ_2 and ξ_3 for some errors in the memory cell.

	ε_g	ε_q
ξ_1	$\frac{g_{out}(V_{gs}-V_T)_Q}{A_V I_{bias}}$	$\frac{-C_{sw}/C_{gs}(V_T+2(V_{gs}-V_T)_Q)-V_{off}}{(V_{gs}-V_T)_Q}$
ξ_2	$\frac{g_{out}(V_{gs}-V_T)_Q}{2A_V I_{bias}^2}$	$\frac{-V_T(C_{sw}/C_{gs})-V_{off}}{4I_{bias}(V_{gs}-V_T)_Q}$
ξ_3	$\frac{-3g_{out}(V_{gs}-V_T)_Q}{8A_V I_{bias}^3}$	$\frac{V_T(C_{sw}/C_{gs})+V_{off}}{8I_{bias}^2(V_{gs}-V_T)_Q}$

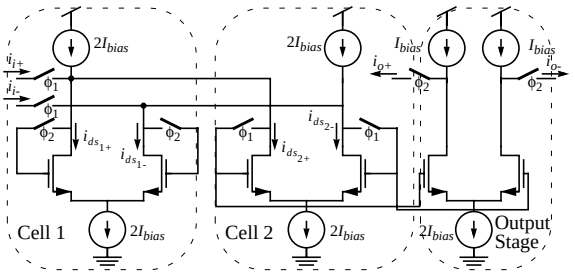

Fig.2. Fully-Differential LDI SI integrator.

$$i_{ds_{2,\,n}} \equiv i_{ds_{2+,n}} - i_{ds_{2-,n}} \cong$$
$$\cong (1-\xi_1)(i_{i,\,n} - i_{ds_{1,\,n-1/2}}) + \xi_3 (i_{i,\,n} - i_{ds_{1,\,n-1/2}})^3 \qquad (7)$$

where $i_{ds_{1,\,n}} \equiv (i_{ds_{1+,n}} - i_{ds_{1-,n}})$ represents the differential drain current of memory cell 1.

After clock phase ϕ_2,

$$i_{ds_{1,\,n+1/2}} \cong (1-\xi_1)(-i_{ds_{2,\,n}}) + \xi_3 (-i_{ds_{2,\,n}})^3 \qquad (8)$$

Assuming that the output stage (represented in Fig.2 as a simple current mirror) is ideal, the output current of the integrator is given by

$$i_{o,\,n+1/2} = -i_{ds_{2,\,n}} \qquad (9)$$

From (7), (8) and (9) it can be derived that the output current of the integrator is

$$i_{o,\,n} \cong (1-\xi_1) i_{x,\,n} + \xi_3 i^3_{x,\,n} \qquad (10)$$

where

$$i_{x,\,n} = -i_{i,\,n-1/2} + (1-\xi_1) i_{o,\,n-1} + \xi_3 i^3_{o,\,n-1} \qquad (11)$$

Assuming that $\xi_1, \xi_3 |i_{o,\,n}|^2 \ll 1$ and performing a Taylor series expansion of (10), obtains

$$i_{o,\,n} \cong (1-2\xi_1) i_{o,\,n-1} - (1-\xi_1) i^*_{i,\,n} \qquad (12)$$

where

$$i^*_{i,\,n} \cong i_{i,\,n-1/2} - \frac{\xi_3}{(1-\xi_1)} (i^3_{o,\,n-1} + i^3_{o,\,n}) \qquad (13)$$

Thus, the analysis of an SI integrator formed by memory cells with non-linear errors can be accomplished considering an integrator formed by memory cells with linear gain errors whose input signal is equal to (13). The equivalent distortion at the integrator input can be estimated by analysing the harmonic content of such an expression.

For this purpose, let assume that the input current is a sinusoidal signal of amplitude I_i and frequency f_i. In this case, the output current of the integrator will be a periodic signal, being the amplitude of its fundamental harmonic approximately given by

$$I_o \cong I_i \left| \frac{-(1-\xi_1) z^{-1/2}}{1-(1-2\xi_1) z^{-1}} \right|_{z\,=\,e^{j2\pi f_i T_s}} \qquad (14)$$

On the other hand, we will suppose that the output of the integrator can be approximated by its first harmonic, so that

$$i_{o,n} \cong I_o \cos(2\pi f_i n T_s) \tag{15}$$

where T_s is the sampling period. Substituting (14) and (15) in (12) and performing a Fourier series expansion, it can be shown that the third-order harmonic is

$$i_{3f_i,n} \cong \frac{\xi_3 I_o^3}{4(1-\xi_1)}[\cos(6\pi f_i n T_s) + \\ + \cos(6\pi f_i (n-1) T_s)] \tag{16}$$

The amplitude of the third-order harmonic at the integrator input derived from (16) is

$$A_{H,3} \equiv \left| i_{3f_i,n} \right| \cong \frac{\xi_3 I_o^3}{2(1-\xi_1)} \left| \cos(3\pi f_i T_s) \right| \tag{17}$$

The amplitude of the third-order harmonic referred to the integrator output can be obtained by multiplying (17) by the module of the integrator transfer function

$$A_{H,3}^{out} = \frac{\xi_3 I_o^3}{4(1-\xi_1)} \left| \cot(3\pi f_i T_s) \right| \tag{18}$$

The third-order harmonic distortion referred to the integrator output is calculated by dividing the above expression by I_o, giving

$$HD_3 \equiv \frac{A_{H,3}^{out}}{I_o} = \frac{\xi_3 I_i^2}{16(1-\xi_1)} \left| \frac{\cot(3\pi f_i T_s)}{[\sin(\pi f_i T_s)]^2} \right| \tag{19}$$

The above expression has been derived for the general case and hence, it can be used to predict the harmonic distortion in SI fully-differential integrators due to any error except for the settling.

As an application, let assume that the integrator in Fig.2 is ideal except for the charge injection error. The theoretical prediction of the third-order harmonic distortion for this integrator is computed by substituting the corresponding expressions of ξ_1 and ξ_3 (see Table 1)†† in (19).

Fig.3 plots HD_3 vs. C_{sw}/C_{gs} and compares the theoretical model with time-domain simulations using the SI behavioral simulator described in [11]. In this example: $(V_{gs}-V_T)_Q = 0.1V$, $V_{off} = 0$ (commom mode signal), $V_T = 1V$ and $I_{bias} = 200\mu A$. Note that, both the linear and the non-linear gain errors increase with C_{sw}/C_{gs}. Their effects on the harmonic distortion are well predicted by the model. On the other hand, the influence of the integrator gain is also considered by changing the input signal frequency. Several values of f_i have been applied showing a good agreement with simulations.

††. These expressions correspond to a single-ended memory cell. For the case of fully-differential, ξ_1 has the same value and $\xi_3 \rightarrow \xi_3/4$.

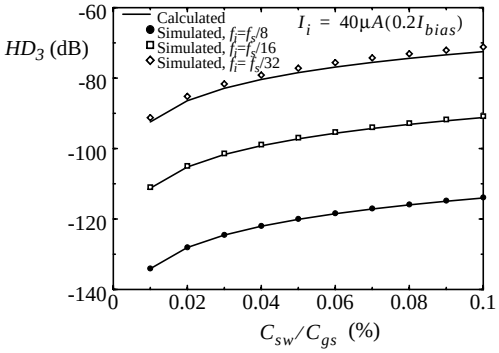

Fig. 3: Third-order harmonic distortion in Fully-Differential LDI SI integrators due to non-linear ε_q. HD_3 vs. C_{sw}/C_{gs}.

4. Harmonic distortion in SI lowpass ΣΔ modulators

Fig.4 shows the block diagram of a second-order lowpass ΣΔ modulator (2ndLPΣΔM) based on LDI integrators. Modelling the quantizer as an additive white noise source $E(z)$ [12], the z-domain modulator output is given by

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \tag{20}$$

where $X(z)$ and $Y(z)$ represent the input and the output of the modulator. In the ideal case, the Signal Transfer Function ($S_{TF}(z)$) and the quantization Noise Transfer Function ($N_{TF}(z)$) are respectively given by

$$S_{TF}(z) = z^{-1} \qquad N_{TF}(z) = (1-z^{-1})^2 \tag{21}$$

For our analysis, the following considerations have been taken into account:

- The harmonic distortion referred to the modulator input is equal to the harmonic distortion referred to the modulator output. This is because the gain of $S_{TF}(z)$ is unity.
- The harmonic distortion referred to the first integrator input is added directly to the input signal. Thus, it is not attenuated in the base band. On the contrary, the contribution of the second integrator to the harmonic distortion is attenuated by the gain of the first integrator. For this reason, only the first integrator contribution has to be considered for the analysis.

Assuming that the transfer function of the first integrator is given by (14), it can be shown that the erroneous signal transfer function of a modulator like that shown in Fig.4 is given by

$$S_{TF}^{err}(z) \cong \frac{(1-\xi_1)z^{-1}}{1 + 2\xi_1 z^{-1} + \xi_1 z^{-2}} \tag{22}$$

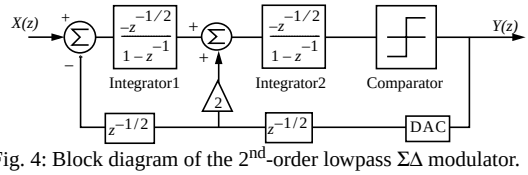

Fig. 4: Block diagram of the 2nd-order lowpass ΣΔ modulator.

On the other hand, obviating the quantization noise, and assuming that $f_i T_s \ll 1$, the expressions for the first integrator input and output amplitudes are respectively given by

$$I_i(z) \cong 4\pi(1-4\xi_1) f_i T_s X(z) \tag{23}$$

$$I_o \cong \frac{I_i}{2\pi f_i T_s} = 2(1-4\xi_1)X(z) \tag{24}$$

Substituting (24) in (17) and dividing the result by the amplitude of the modulator input signal $A = |X(z)|$, obtains the third-order harmonic distortion at the modulator output as follows:

$$HD_3 \cong 4\xi_3(1-11\xi_1)A^2\left(1-\frac{3\pi}{2M}\right) \tag{25}$$

where $M \equiv f_s/(2f_i)$ represents the oversampling ratio.

The above expression has been validated by time-domain behavioral simulation. Fig.5 illustrates the harmonic distortion of the modulator in Fig.4 assuming that their memory cells are ideal except for the charge injection error. Fig.5(a) compares the predictions of (25) with simulations by plotting HD_3 as a function of the ratio C_{sw}/C_{gs}. In this figure, the DAC reference current is $I_{DAC} = I_{bias}/2$ while the input amplitude is $A = I_{DAC}/2$. Fig. 5(b) shows a simulated output spectrum for $(V_{gs}-V_T)_Q = 0.1V$ and $C_{sw}/C_{gs} = 0.08\%$. The predicted data for the third-order harmonic distortion is $HD_3 = -86$ dB which agrees with the simulated data ($HD_3 = -85$ dB).

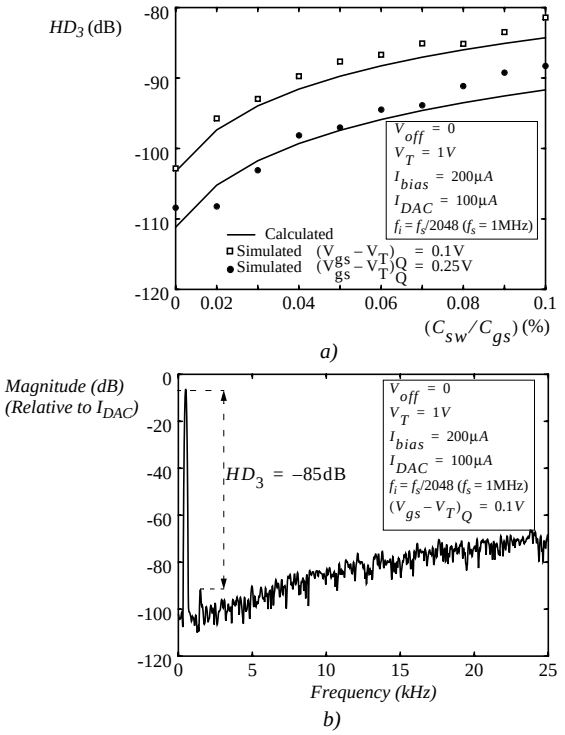

Fig. 5: HD_3 at the output of a 2nd order lowpass ΣΔ modulator due to ε_q. a) HD_3 vs. C_{sw}/C_{gs} for different values of $(V_{gs}-V_T)_Q$. b) Output spectrum corresponding to $(V_{gs}-V_T)_Q = 0.1V$ and $C_{sw}/C_{gs} = 0.08$ % (Input amplitude equal to -6dB DAC reference current I_{DAC}).

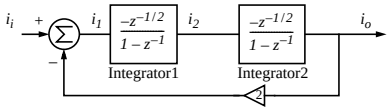

Fig. 6: LDI Loop Resonator.

5. Harmonic distortion in SI bandpass ΣΔ modulators

A. Harmonic distortion in SI resonators

Most of bandpass ΣΔ modulators reported in the literature obtain their architecture by applying the transformation $z^{-1} \rightarrow -z^{-2}$ to the corresponding low-pass ΣΔ modulators [12]. As a consequence of this transformation, the original integrators become resonators with a transfer function given by

$$H(z) = \frac{z^{-a}}{1+z^{-2}} \tag{26}$$

The value of a depends on the transfer function of the original integrator. There are many filter structures which implement (26) [12]. Fig.6 shows the block diagram of one based on LDI integrators. This structure is advantageous as compared to the others because it remains stable under changes in the loop coefficients.

Let assume that the integrators which form the resonator in Fig.6 are implemented as shown in Fig.2. In the presence of non-linear errors, they can be described by (12) and, hence, the difference equations which describe the behavior of the resonator are

$$i_{2,n} \cong -(1-\xi_1)i_{1,n-1/2} + (1-2\xi_1)i_{2,n-1} + \\ + \xi_3 i_{2,n}^3 + \xi_3 i_{2,n-1}^3 \tag{27}$$

$$i_{o,n} \cong -(1-\xi_1)i_{2,n-1/2} + (1-2\xi_1)i_{o,n-1} + \\ + \xi_3 i_{o,n}^3 + \xi_3 i_{o,n-1}^3 \tag{28}$$

where i_1 and i_2 are respectively the input and the output of the first integrator in the loop (see Fig.6) while i_i and i_o are respectively the input and the output of the resonator.

Solving for $i_{2,n}$ in (28), substituting it in (27) and assuming that $\xi_1, \xi_3|i_{o,n}|^2 \ll 1$, result in the following difference equation

$$i_{o,n} \cong (1-2\xi_1)i'_{i,n} - (1-4\xi_1)i_{o,n-2} \tag{29}$$

where

$$i'_{i,n} = i_{i,n-1} + \frac{\xi_3}{1-2\xi_1}[i_{o,n}^3 - i_{o,n-2}^3 + \\ (i_{o,n} - i_{o,n-1})^3 + (i_{o,n-1} - i_{o,n-2})^3] \tag{30}$$

Assuming that i_i is a sinusoidal signal of amplitude I_i, i_o will be a periodic signal, being the amplitude of its fundamental harmonic

$$I_o \cong I_i \left| \frac{(1-2\xi_1)z^{-1}}{1+(1-4\xi_1)z^{-2}} \right|_{z = e^{j2\pi f_i T_s}} \tag{31}$$

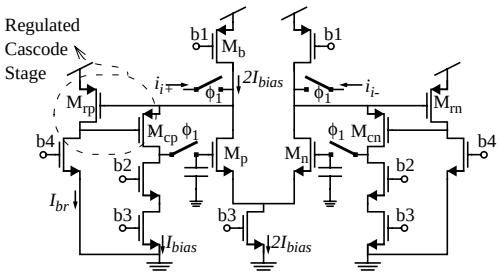

Fig. 7: Fully-differential regulated folded-cascode memory cell.

As for the case of the integrator, the output current of the resonator can be approximated by its fundamental harmonic, which can be generically expressed as

$$i_{o,n} \cong I_o \cos(\phi_n) \tag{32}$$

where $\phi_n = 2\pi f_i T_s n + \Phi(f_i, \xi_1)$ and $\Phi(f_i, \xi_1)$ is the phase delay caused by the resonator.

Substituting (32) in (30), and performing a Fourier series expansion, it can be shown that the third-order harmonic is

$$i_{3f_i,n} \cong \frac{-\xi_3 I_o^3}{1-2\xi_1}\left[\left(\frac{1}{2} + 6\pi f_i' T_s\right)\cos(3\phi_n) + \right. \\ \left. + (3\pi f_i' T_s)\sin(3\phi_n)\right] \tag{33}$$

where $f_i' = f_i - f_s/4$, and $f_i' T_s \ll 1$ has been assumed.

From (33) it can be derived that the amplitude of the third-order harmonic at the resonator input is

$$A_{H,3} \equiv \left|i_{3f_i,n}\right| \cong \frac{\xi_3 I_o^3}{2(1-2\xi_1)}(1 + 12\pi f_i' T_s) \tag{34}$$

Following the same procedure as in Section 3, the third-order harmonic distortion at the resonator output can be found by multiplying (34) by the resonator gain and dividing this result by I_o. This gives

$$HD_3 \cong \frac{\xi_3 I_i^2}{384(1-2\xi_1)(\pi f_i' T_s)^3(1+\chi^2)\sqrt{1+\frac{\chi^2}{9}}} \tag{35}$$

where $\chi = \xi_1/(\pi f_i' T_s)$.

As an application of the previous analysis, let assume that the resonator in Fig.6 is formed by fully-differential regulated-folded cascode memory cells like that shown in Fig.7. Because of the input feedback loop (which increases the input conductance), this memory cell exhibits a third-order dynamics. It can be shown that the current source named I_{br} (see Fig.7) has to be taken as large as possible in order to obtain an overdamped settling response. However, large values of I_{br} may force some transistors to leave the saturation region, thus causing a non-linear dependence of the input voltage on the input signal. This behavior can be modeled as

$$V_{id} = r_1 I_D + r_3 I_D^3 \tag{36}$$

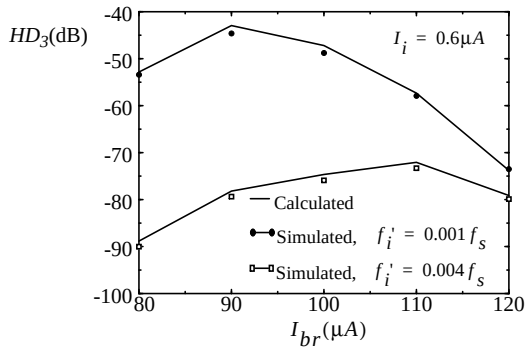

Fig. 8: Harmonic distortion at the output of a SI resonator caused by the non-linear input impedance of regulated folded cascode memory cells.

where V_{id} and I_D are respectively the differential input voltage and the differential drain current of each memory cell. Coefficients r_1 and r_3, which are function of I_{br}, were extracted from DC nominal HSPICE simulations. It can be shown that

$$\xi_1 \cong -2 g_{out} r_1 \qquad \xi_3 \cong -2 g_{out} r_3 \tag{37}$$

where g_{out} is the output conductance of the memory cell. Thus, the harmonic distortion of the resonator can be calculated by simply substituting (37) in (35).

Fig.8 compares theoretical results with simulations by plotting HD_3 as a function of I_{br} for different values of f_i'. Note that, as a consequence of changing both the linear and the non-linear error, the harmonic distortion does not increase with I_{br}. This is well predicted by the model. Because of the resonator open loop gain is too high, the input amplitude was chosen to be small ($I_i = 0.6\mu A$) in order to keep memory transistors in the saturation region.

B. Harmonic distortion in SI 4th-order bandpass ΣΔ modulators

Fig.9 shows the block diagram of a fourth-order bandpass ΣΔ modulator (4thBPΣΔM) based on LDI loop resonators like that shown in Fig.6. Modelling the quantizer as an additive white noise source $E(z)$ and considering that the integrators are ideal, the *z*-domain equations that describe the behavior of the modulator are:

$$\begin{aligned} Y(z) &= z^{-2}X(z) + (1+z^{-2})^2 E(z) \\ I_1(z) &= X(z) - z^{-2}Y(z) - 2I_o(z) \\ I_2(z) &= \frac{-z^{-1/2}}{(1-z^{-1})} I_1(z) \\ I_o &= \frac{z^{-1}}{1+z^{-2}}(X(z) - z^{-2}Y(z)) \end{aligned} \tag{38}$$

where $X(z)$ and $Y(z)$ represents respectively the input and the output of the modulator; $I_1(z)$ and $I_2(z)$ are the input and the output of the first integrator; $I_i(z)$ and $I_o(z)$ are the input and the output of the first resonator.

Only the contribution of the first resonator will be

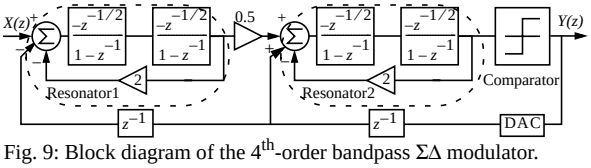

Fig. 9: Block diagram of the 4th-order bandpass ΣΔ modulator.

considered for the analysis of the distortion. This is because the contribution of the second resonator is attenuated by the gain of the first resonator in the signal band.

From (38), the amplitude of the resonator output can be written as

$$I_o = A\left|1 - z^{-2}\right|\Big|_{z = e^{j2\pi f_i T_s}} \qquad (39)$$

where A is the amplitude of the modulator input. Taking into account the effect of the linear gain error ξ_1 on the integrators, it can be shown that the above expression is modified as follows:

$$I_o \cong A(1 - 6\xi_1)\left|1 - z^{-2}\right|\Big|_{z = e^{j2\pi f_i T_s}} \qquad (40)$$

Substituting (40) in (34) and dividing by A the third-order harmonic distortion at the modulator output is approximately given by

$$HD_3 \cong 4\xi_3 A^2(1 - 16\xi_1)(1 + 12\pi f_i' T_s) \qquad (41)$$

In bandpass signal processing, the third-order intermodulation distortion, IM_3 is more appropriate for measuring distortion than HD_3. Let assume that the modulator input consists of two sinusoidal signals of the same amplitude and different frequencies f_1 and f_2. If the memory cells which form the modulator are degraded by non-linear errors, the modulator output spectrum presents intermodulation harmonics of the input signals. Among them, the most significant is IM_3, which is defined as the amplitude of the output at $2f_2 - f_1$ and $2f_1 - f_2$ related to the linear output amplitudes at f_2, f_1. It can be shown that IM_3 is related to HD_3 as

$$IM_3 = 3HD_3 \qquad (42)$$

For illustration, Fig.10(a) compares simulation results to theoretical data by plotting IM_3 against I_{br} for different values of the DAC reference current I_{DAC}. Fig.10(b) shows the output spectrum of the modulator for $I_{br} = 110\mu A$ and $I_{DAC} = 50\mu A$. The predicted value for IM_3 is -53dB which agrees with the simulated value (-51dB).

Conclusions

The impact of main SI errors on the harmonic distortion in both lowpass and bandpass ΣΔ modulators has been analysed. Closed form equations for the third-order harmonic distortion and the third-order intermodulation distortion of their main blocks are also provided. General expressions are derived which can be particularized for each SI error. All results are validated by time-domain behavioral simulations [11].

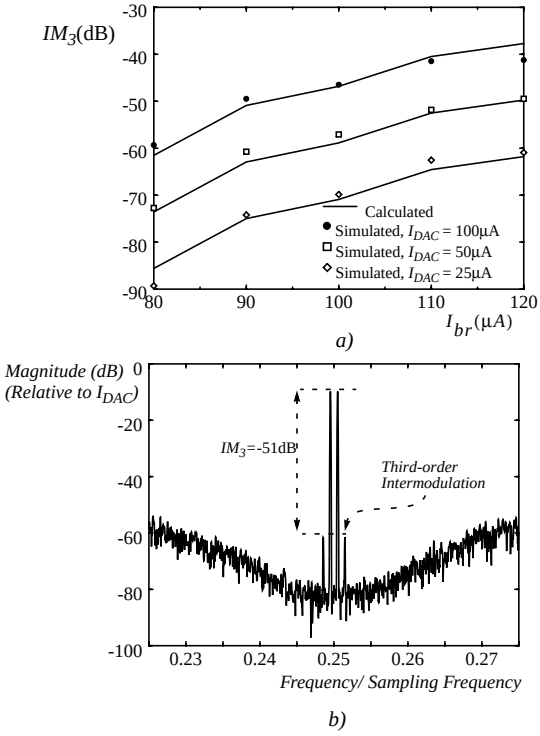

Fig. 10: IM_3 at the output of a 4th order bandpass ΣΔ modulator due to the non-linear input impedance of regulated folded-cascode memory cells. a) IM_3 vs. I_{br}. b) Output spectrum corresponding to $I_{br} = 110\mu A$, and $I_{DAC} = 50\mu A$. (Amplitude of each input tone equal to $(1/2\sqrt{2})I_{DAC}$).

References

[1] C.Toumazou, J.B.Hughes, and N.C. Battersby, *Switched-Currents: An Analogue Technique for digital technology*, London, Peter Peregrinus Ltd.,1993.

[2] J.B. Hughes, K.W. Moulding, J. Richardson, J. Bennet, W. Redman-White, Mark Bracey and R. Singh Soin, "Automated Design of Switched-Current Filters", *IEEE J. Solid-State Circuits*, pp. 898-907, July 1996.

[3] B.E. Jonsson and H. Tenhunen, "Low-Voltage, 10bit Switched-Current ADC with 20MHz Input Bandwidth", *Electron. Lett.*,pp. 1904-1905,October 1998.

[4] N.Tan, *Switched-Current Design and Implementation of Oversampling A/D Converters*, Kluwer Academic Publishers, 1997.

[5] N. Moeneclaey and A. Kaiser, "Design Techniques for High-Resolution Current-Mode Sigma-Delta Modulators", *IEEE Journal of Solid-State Circuits*, pp. 953-958, July 1997.

[6] J.M. de la Rosa, B. Pérez-Verdú, F. Medeiro and A. Rodríguez-Vázquez, "A 2.5MHz 55dB Switched-Current BandPass ΣΔ Modulator for AM Signal Conversion", *Proc. of the 1997 European Solid-State Cicuits Conference*, pp. 156-159, 1997.

[7] F. Medeiro, B. Pérez-Verdú and A. Rodríguez-Vázquez, *Top-Down Design of High-Performance Sigma-Delta Modulators*, Kluwer Academic Publishers, 1999.

[8] T.S. Fiez, G. Liang, and D.J. Allstot, "Switched-Current Circuit Design Issues", *IEEE J. Solid-State Circuits*, pp. 192-202, March 1991.

[9] J.M. Martins and V. F. Dias, "Harmonic Distortion in Switched-Current Audio Memory Cells", *IEEE Transactions on Circuits and Systems- Part II*,Vol. 46, pp. 326-334, March 1999.

[10] J.M. Martins, V.F. Dias, "Harmonic Distortion in Switched-Current Sigma-Delta Modulators due to Clock Feedthrough", *Proc. 1998 IEEE Int. Symp. Circuits and System*, 1998.

[11] J.M. de la Rosa, A. Kaiser and B. Pérez-Verdú, "Interactive Verification of Switched-Current Sigma- Delta Modulators", *Proc. of 1998 IEEE International Conference on Electronics, Circuits and Systems*, pp. 2.157-2.160, 1998.

[12] S.R. Norsworthy, R. Schreier, G.C. Temes: *Delta-Sigma Converters. Theory, Design and Simulation.* New York, IEEE Press, 1997.