XVII IMEKO World Congress
Metrology in the 3rd Millennium
June 22–27, 2003, Dubrovnik, Croatia

A FIRST ORDER INCREMENTAL ANALOG TO DIGITAL CONVERTER BASED ON CONTINUOUS TIME CIRCUITS

Ricardo Doldan, Alberto Yufera and Adoracion Rueda

Instituto de Microelectronica de Sevilla (IMSE), Sevilla, Spain

Abstract - In this paper, an incremental Analog-to-Digital Converter (ADC) designed as part of the signal-conditioning circuitry for tissue impedance measurement system is presented. Continuous-time design techniques has been used and a modified implementation of the conversion algorithm, with respect to its discrete-time counterpart, has been developed. To reduce the influence of the no-idealities, analog and digital corrections have been also implemented. A prototype in *0.8*μm *CMOS* technology has been fabricated and tested. Experimental results are reported.

Keywords Analog to Digital Conversion.

1. INTRODUCTION

In this work, we present the design and implementation of a first order Incremental Analog-to-Digital Converter (*ADC*) using the continuous-time approach. In particular, the *OTA-C* technique is applied to design the main analog signal processing functions, such as integrator and adders, as an alternative to Switched Capacitor (SC) approach for low voltage conditions. This work is part of a project aimed at establishing a design procedure for tissue impedance measurement with application in measure of biological parameter [1]. The proposed measurement system is shown in Fig. 1. It is based on a four-electrodes configuration (Z_{E1} to Z_{E4}), in which two of them (Z_{E1}, Z_{E4}) are employed to stimulate the tissue sample (*SUT)* of unknown impedance Z_x, and the other two (Z_{E2}, Z_{E3}) take the *SUT* response. After amplification and processing steps, two digital signals are obtained for real and imaginary parts of the tissue complex impedance, Z_x. Both are digitally codified for parallel transmission. Incremental converters based on sigma-delta modulation, double-ramp principle, or multivibrator are normally used in these applications [2-4], providing high accuracy, good linearity, and reduced offset levels. In our case, a first order incremental converter with a *bit parallel* digital output has been considered.

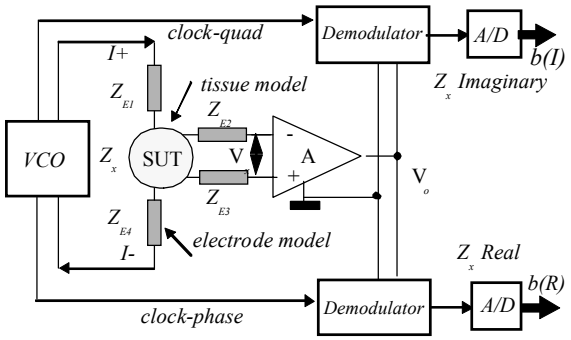

Fig. 1. Blocks envolved in the real and imaginary impedance measurement system

The paper is organized as follows. The conversion algorithm is briefly described in Section 2. The design of the basic building blocks for continuous time analog to digital conversion is presented in Section 3. Section 4 shows experimental results. Finally, some conclusions are given in Section 5.

2. THE ANALOG TO DIGITAL ALGORITHM

The operation principle of an incremental *ADC* relies on changing voltage-resolution for time-resolution, performing the integration of the analog input to obtain a *bit-stream* output [2]. This output is easily transformed into a digital word by basic digital circuits. The block diagram of the *ADC* is illustrated in Fig. 2. This incremental converter works as a sigma-delta modulator with a reset signal at the beginning of each conversion. Its main blocks are the integrator and the comparator. Other blocks are the input signal multiplexer, the control block to reset and invert the integrator output voltage, and the digital output signal processing, basically a counter. The basic algorithm works as follows: a differential signal ($V_{in} = V_{inp}$-V_{inn}) is continuously integrated. The integrator output (V_{op}) is then compared with zero. For positive values, a -V_{Ref} value will be added at the integrator input, V_{in}; For negatives, V_{Ref} will be. Every T seconds V_{op} is compared with zero, being the output, $N_{con,}$ a *n-bit* digital word proportional to the times that V_{Ref} has been added and subtracted at the input. This reference represents the half of converter *Full Scale*, so that the *LSB* is given by $V_{Ref} / 2^{n-1}$ for a converter of n bits. The decision to add/subtract depends on the comparator output. The

conversion time is fixed by the number of bits. A discrete-time realization of the converter requires three basic operation modes: reset, sample and positive conversion. A description of these follows.

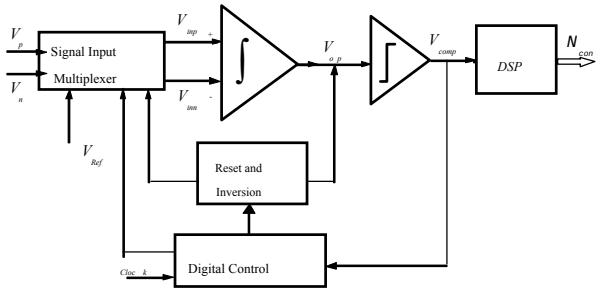

Fig. 2. Conceptual schematic o fan incremental ADC

In the first clock period, *Reset Mode*, the integrator is autozeroed. Next, in *Sample Mode*, the analog input signal is connected to the integrator positive input, giving $V_{op}=V_{in}^*$. The *Positive Conversion Mode* (*PCM*) interval is 2^{nT} (where T is the clock period), during which the comparator performs 2^n discriminations. Initially, depending on the positive or negative sign of V_{in}^*, V_{Ref} is subtracted from or added to V_{in}^*, respectively. Adding or subtracting means to put the V_{Ref} signal into the integrator positive or negative input terminal respectively, thus avoiding the need of two voltage reference V_{Ref} and $-V_{Ref}$. Adding and subtracting V_{Ref} also moves the counter state up and down. With N_{u1} and N_{d1} representing the number of up and down counts, respectively, the integrator output after 2^n clock periods will be:

$$V_{op}(2^n) = (N_{d1}-N_{u1})V_{Ref}+(N_{u1}+N_{d1})V_{in}^* \tag{1}$$

and,

$$N = N_{u1}-N_{d1} = 2^n\left(\frac{V_{in}^*}{V_{Ref}}\right)-\frac{V_{op}(2^n)}{V_{Ref}} \tag{2}$$

The analog-to-digital conversion is thus realized, and N represents the state of the output counter obtained as the difference between the up and down counts. The accuracy of the digital representation of V_{in}^* is ^{n} bits. One extra bit can be obtained by detecting the sign of $V_{op}(2^n)$. Due to the high number of integration steps, this type of conversion can be critical to the integrator input equivalent offset. A digital correction technique, as proposed in [3], can be used. In this case, two additional operation modes are necessary: inversion and negative conversion modes.

After the first 2^{n-1} positive conversion cycles, the signal at the integrator output is inverted. The integrator output in the next clock period will be $-V_{op1}$, where $V_{op1} = V_{op}(2^{n-1})$ is given by (1) using $n-1$ instead of n. This is the *Inversion Mode*. During the following 2^{n-1} clock cycles the *Negative Conversion Mode* (*NCM*) operates similarly to *PCM*, but now the $-V_{in}^*$ input signal is sampled and compared to zero. Up and down counts are decided inversely as in *PCM*. At the end, the signal accumulated at the integrator output is,

$$V_{op}(2^n) = -V_{op1}-2^{n-1}V_{in}^*+(N_{u2}-N_{d2})V_{Ref} \tag{3}$$

and,

$$V_{op}(2^n) = -2^nV_{in}^*+2NV_{Ref} \tag{4}$$

where $2N=(N_{u2}-N_{d1}+N_{u1}-N_{d2})$ is an *n-bit* digital word. In this case, the extra sign bit (d) will be *"1"* if $V_{op}(2^{n+1}) < 0$ and *"0"* otherwise. The final digital word, $N_{con,}$ will be obtained as $2N+d$.

The described *ADC* has the advantage that its resolution does not depend on the integrator gain errors, and furthermore, the integrator non-signal dependent offset is cancelled. An important property that must be preserved is the use of an unique V_{Ref}. The reason for this is that mismatching between V_{Ref} and - V_{Ref} generates output errors which increase with the number of bits. The same considerations apply to the input signals.

3. CONTINUOUS TIME IMPLEMENTATION

In the continuous time version of the ADC, the basic idea has been to divide each integration period, T, into two intervals, in such a form that the input signal, V_{in}, and the reference signal, V_{Ref}, will be integrated in different times: the input in $(0,T/2)$, and the reference in $(T/2,T)$, respectively. This is illustrated in Fig. 3. In this algorithm, a comparison by cycle is carried out at $T/2$. Analysing the final result the output digital code is obtained as,

$$N_{con} = \left\lceil \frac{V_{in}^*}{V_{LSB}} \right\rceil \tag{5}$$

that represents the integer part operator of this ratio. This modified algorithm solves some problems derived from continuous time implementations, in particular due to the integrator, since errors in linear integration will be high due to the influence of the finite transconductor output resistance [6]. When the input signal V_{in}^* approach to the FS limits, the effective period of integration increases since V_{op} changes its sign only a very few times. In these situations, the integrator output resistance will degrade the quality of the integration process.

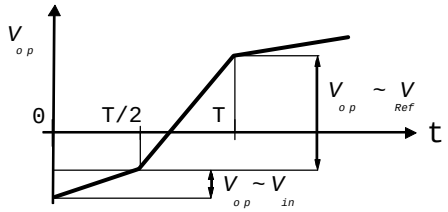

Fig. 3. Integrator output evolution in the proponed algorithm

The specifications for the targeted *ADC* are: *12* bits, a *50kHz* clock, a voltage supply below *3V*, and an input range of *0.5V* in bipolar conditions. The circuits required for that are both analog and digital.

The block diagram of the analog part is shown in Fig. 4. It includes a controlled two-input integrator and a comparator. The functionality of each block is briefly explained in the following. The input *mux* block is controlled by the S_{vin} digital signal, which selects when the integrator has to process the ADC input or a zero input. The *INV* block applies for signal inversions. Both blocks are implemented with *CMOS* analog switches, whose on-resistance must be optimized when they are in the signal path. The *RES* block discharges the capacitor when the conversion ends. For the reference signal integration the same *OTA* than for the input is used, whose operation is now controlled by the S_{vref} digital signal, sourcing/sinking (*b* for sourcing, and *b* for sinking, being *b* the comparator output signal) current at the integrating capacitor *C*. The more challenging analog block is the *OTA*. Its input voltage range must be *0.5V* bipolar, so a linearized architecture has to be chosen. We have employed the circuit reported in [5] which allows to increase the input linear range by properly designing *M2* and *M22* transistors. Its schematic including the common-mode feedback circuit is shown in Fig. 5. In order to guaranty the linearity of the *OTA-C* integrator, the selection of the transconductance value is realized taken into account the integrator capacitor value, the *OTA* output resistance, and the integration time. In the proposed algorithm, the input voltage at the integrator will be a step signal from zero to the present input sample value. So, considering an ideal integrator as illustrated in Fig. 6, transient time evolution of the capacitor voltage can be described as,

$$V_o = \frac{g_m V_{in}}{C} \cdot t \qquad (6)$$

The maximum value for V_{in} should be $V_{Ref,}$ that integrated in a *T/2* period of time will give us the maximum output range. For a *C=15pF*, we have chose g_m*=0.338*□*S*. The corresponding transistor sizes are in Table 1. The linearized *OTA* response is illustrated in Fig. 7, where an $1V_{pp}$ input range can be appreciated for a g_m linearity error below *0.9%*. For a real, the time constant given by $R_{out}C$ must be dimensioned to preserve the output linearity range. Since we have a *T/2 = 10*□*s,* and a *7.5ms* time constant value has been considered enough to work always in the linear region. This leads to a R_{out} *= 500M*Ω for a *C=15pF*.

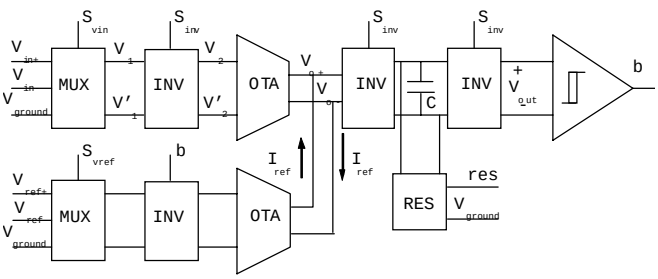

Fig. 4. ADC analog blocks

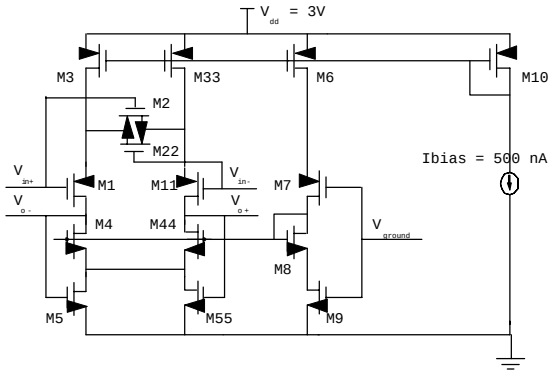

Fig. 5. Schematic of the OTA

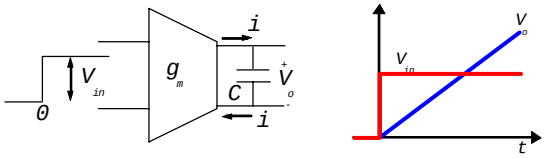

Fig. 6. Ideal step response of the linearized OTA-C integrator

Table 1: **Transistor sizes for the *OTA***

Transistor	[μm/μm]	Transistor	[μm/μm]
M1, M11	*4/20*	*M5,M55,M9*	*6/2*
M2, M22	*2/64*	*M6, M10*	*20/5*
M3, M33	*20/5*	*M7*	*4/20*
M4, M44	*1.5/13.8*	*M8*	*1.5/13.8*

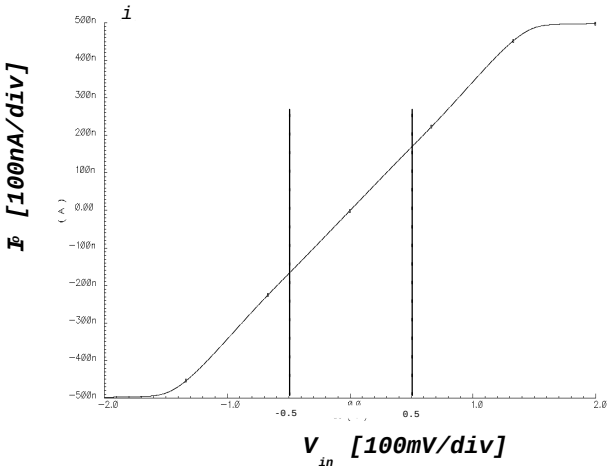

Fig. 7. I_o versus V_{in} linearized OTA characterictic

The general block descriptions for the digital control and processing parts comprises two *14bits* counters, and a more specific control block that will not be described now. The input for these blocks are: the clock (*clk*), an external reset (*res_ext*), the number of bits for the *ADC* (*n*) that has been parametrized in the range (*2,13*), and finally, the *bit-stream* (*b*) from the comparator output. The circuits has been implemented using standard cell from a *VHDL* whole function description.

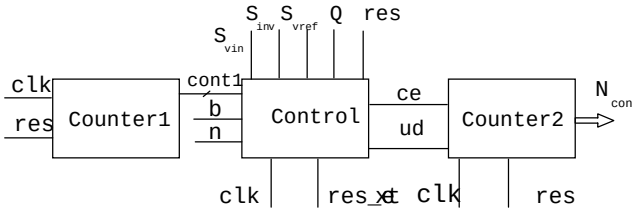

Fig. 8. Digital blocks involved in the ADC

4. EXPERIMENTAL RESULTS

A *0.8□m CMOS* prototype has been integrated and tested. Its layout spends a silicom area of *2265µm x 2012µm*. There has been performed a static test for the experimental characterization of the *ADC*. The transfer function and *DNL* and *INL* graphics obtained for *12b* are shown in Figures 10 and 11 respectively for *n=12 bits*, for an input signal of absolute value in the range of *500mV*, with V_{Ref}= *500mV*, and working with a power supply of *3V*. An implicit advantage of continuous time implementations is the good frequency scaling behaviour since the clock drives the conversion time but not the *ADC* operation. This is illustrated in Fig. 12, where the performance of the same prototype tested at *2MHz* clock frequency is shown.

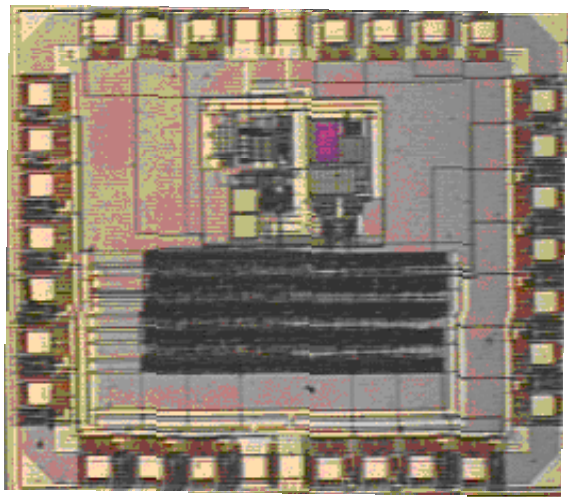

Fig. 9. Photograph of the ADC

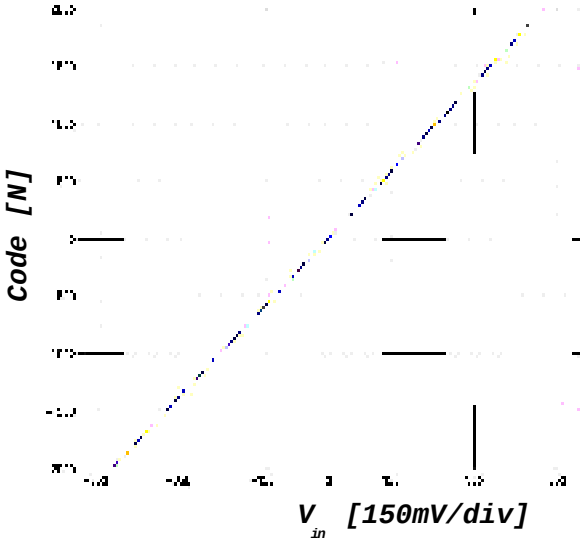

Fig. 10. Experimental transfer function for *n=12bits* and V_{Ref} = *500mV*.

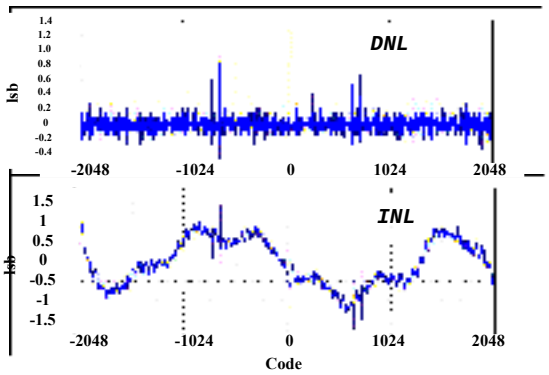

Fig. 11. DNL and INL for *n=12b*, V_{Ref}=*500mV* and f_c=*50kHz*.

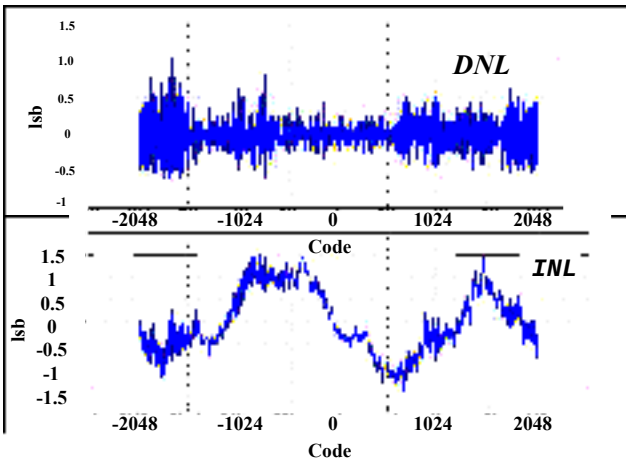

Fig. 12. DNL and INL for $n=12b$, $V_{Ref}=500mV$ and $f_c=2MHz$.

5. CONCLUSION

In this paper, the design of a first order Continuous Time Analog to Digital Converter has been presented. The proposed analog to digital conversion algorithm considers its continuous-time implementation, reducing the errors derived from the finite integrator output resistance. A silicon prototype has been integrated for a 12-bit resolution. Test results show a good agreement with the specified performance and an excellent frequency scaling performance.

REFERENCES

[1] A. Yúfera, G. Leger, E. O. Rodriguez-Villegas, J. M. Muñoz, A. Rueda, A. Ivorra, R. Gomez, N. Noguera and J. Aguiló: "An Integrated Circuit for Tissue Impedance Measured". *Proc. of IEEE EMBS*. USA, May 2002.

[2] J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy and P. Deval: "A 16-bit Low-Voltage CMOS A/D Converter". *IEEE J. of Solid-State Cir.*, vol SC-22, n□□, Apr., pp.157-163.1987.

[3] A. Yúfera and A. Rueda:"A S2I First Order Incremental A/D Converter". *Proc. of IEE Part-G: Circuits, devices and system*, vol. 145, nº2, pp. 78-84. 1998.

[4] A. Haberli, P. Malcovati, H. Baltes, and F. Maloberti: "An Incremental A/D Converter for Accurate Vector Probe Measurements". *Proc. of IEEE ISCAS*. pp. 541-544. 1995.

[5] F. Krummenacher and N. Joehl, "A 4-Mhz CMOS continuous- time filter with on-chip automatic tuning," *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 114-1121, Dec. 1985.

[6] R. Doldan, A. Yúfera and A. Rueda: " A Continuous-Time Incremental Analog to Digital Converter". *Proc. of the 15th Symposium on Integrated Circuits and Systems Design*. pp: 62-67. Porto Alegre, Brazil. Sep. 2002..

Author: Ricardo Doldan, Alberto Yúfera and Adoración Rueda. Instituto de Microelectrónica de Sevilla (IMSE-CNM). Ed. CICA. Av. Reina Mercedes s/n. 41012. Sevilla. SPAIN. Phone: +34-955056666.Fax:+34-955056686. emails:{rdoldan,yufera,rueda}@imse.cnm.es.