sciendo

Journal of ELECTRICAL ENGINEERING, VOL 69 (2018), NO3, 250–254

Methodology to improve the model of series inductance in CMOS integrated inductors

Eric F. Gutierrez-Frias*, Luis A. García-Lugo*, Edwin C. Becerra-Alvarez*, Juan J. Raygoza-Panduro*, José M. de la Rosa, Edgardo B. Ortega-Rosales*****

This paper presents a systematic optimization methodology to achieve an accurate estimation of series inductance of inductors implemented in standard CMOS technologies. Proposed method is based on an optimization procedure which aims to obtain adjustment factors associated to main physical inductor characteristics, allowing to estimate more accurate series inductance values that can be used in design stage. Experimental measurements of diverse square inductor geometries are shown and compared with previous approaches in order to demonstrate and validate presented approach.

K e y w o r d s: optimization, inductance, adjustment factors, integrated inductors

1 Introduction

Huge growth of mobile communications in last years demands more and more high-performance, low-cost and power-efficient on-chip Radio Frequency (RF) circuits and systems.

Continuous incorporation of new standards and services [1], together with the trend toward interconnection of billions of wireless devices in so-called Internet of Things (IoT), make the optimized design of RF transceivers one of pillars supporting this new technology wave [2]. Among others, integrated inductors are key circuit elements enabling implementation of efficient IoT devices [3], since they are essential parts used to build basic RF subcircuits, such as Low-Noise Amplifiers (LNAs), Power Amplifiers (PA), mixers and Voltage-Controlled Oscillators (VCOs) [4]. Inductors are employed for tasks such bias feeding and impedance matching of transistors. Reactively matched transistors enable significantly higher gain-DC power rations and better noise performance [5].

A problem in using on-chip inductors in design of integrated circuits is poor quality of inductors models in many available technologies. Using available inductor models in technology library may lead to a situation where parameters of manufactured systems do not match expected specifications [6]. An accurate and systematic design of integrated inductors requires taking into account most important physical effects associated to their implementation in CMOS technologies [7]. To this end, a physical model and an equivalent circuit, usually considered by RF circuit designers, is illustrated in Fig. 1(a) and pi-model Fig. 1(b) [8], which is a good approximation for the physical behavior of integrated inductors.

Physical model, Fig. 1(a), shows separation distance between spires s, spire width w, internal diameter d_{in} and outer diameter d_{out}. Equivalent circuit, Fig. 1(b), consists of main circuit-element parameters as series inductance L_s, series resistance R_s, overlap capacitance between segment and underpass C_s, and oxide capacitance between the silicon substrate C_{ox}. The substrate losses including parasitic capacitance C_{si} and its resistance R_{si}, are also considered in this model [9].

One of the most important characteristics in pi-model is L_s, which has been exhaustively analyzed by a number of authors in order to get compact and precise closed-form design expressions that relate the physical implementation with geometric dimensions of inductor structure [10,11,12,13]. Such design equations give an estimation of L_s, which can be used for design purposes. However, model value of L_s can be further improved by properly adjusting their main physical parameters through an optimization methodology.

2 Background of Series Inductance Modeling

As stated above, a number of closed-form expressions to estimate the series inductance have been reported.

Two of the simplest formulations were presented by Mohan *et al* in [10], where L_s is modeled by two series inductances: modified Wheeler's formula, and current-sheet approximation, denoted as L_{MW} and L_{MC}, respectively.

* University Center for Exact Sciences and Engineering, Universidad de Guadalajara, Av. Marcelino García Barragán and Calz. Olímpica 1421, Guadalajara, Jalisco, México, ** Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla, C/Américo Vespucio, 41092 Sevilla, Spain, *** Universidad Tecnológica de la Zona Metropolitana de Guadalajara, camino a San Isidro Mazatepec Km 4.7, Tlajomulco de Zuñiga, Jalisco, México eric.gutierrez@alumnos.udg.mx, luis.glugo@alumnos.udg.mx, edwin.becerra@cucei.udg.mx, juan.raygoza@cucei.udg.mx, jrosa@imse-cnm.csic.es, eortega@utzmg.edu.mx

DOI: 10.2478/jee-2018–0034, Print (till 2015) ISSN 1335-3632, On-line ISSN 1339-309X

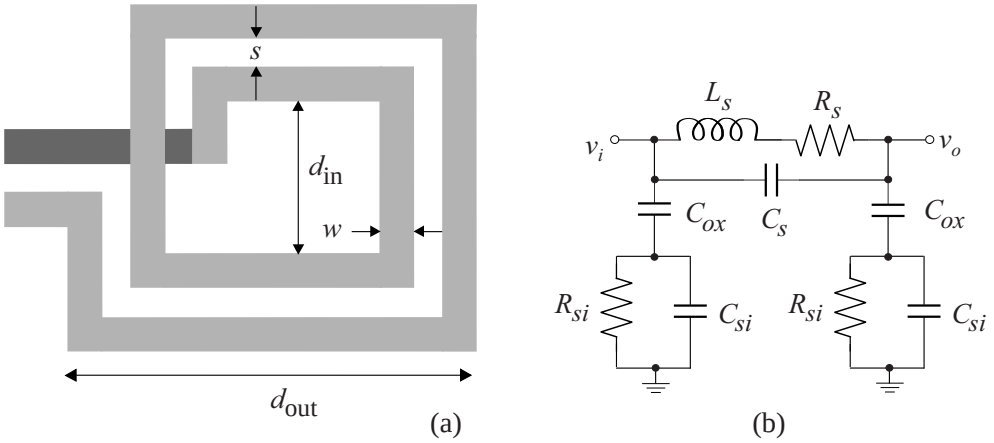


Fig. 1. Integrated inductor model: (a) – conceptual physical structure, (b) – equivalent circuit

These two series inductances can be approximated by the following expressions

$$L_{\text{MW}} = K_1 \frac{\mu_0\, n^2 d_{\text{avg}}}{1 + K_2 \rho} \tag{1}$$

$$L_{\text{MC}} = \frac{\mu_0\, n^2 d_{\text{avg}} c_1}{2} \left[\ln\left(\frac{c_2}{\rho}\right) + c_3 \rho + c_4 \rho^2 \right] \tag{2}$$

ρ and d_{avg} are respectively given by

$$\rho = \frac{d_{\text{out}} - d_{\text{in}}}{d_{\text{out}} + d_{\text{in}}} \quad d_{\text{avg}} = \frac{d_{\text{out}} + d_{\text{in}}}{2}$$

where μ_0 stands for the magnetic permeability in vacuum; d_{in} and d_{out} are respectively the inner and outer diameter shown in Fig. 1(a) as mentioned previously, n is the number of turns, with $K_1 = 2.34$, $K_2 = 2.75$, $c_1 = 1.27$, $c_2 = 2.07$, $c_3 = 0.18$, $c_4 = 0.13$ being some adjustment coefficients for square inductors [10].

Another approach to derive closed-form design expressions for L_s was proposed by Jenei *et al* [11] and Asgaran *et al* [12], which were in turn mainly inspired in Greenhouse's work [14]. Contrary to former approaches, Jenei's model expressions are based on an approximation of total length of the inductor, l_{tot}, rather than checking self-inductance and mutual inductance of every spire – as suggested by Greenhouse. This way, model proposed by Jenei *et al* can be formulated as

$$L_{\text{J}} = L_{0\text{J}} + M_{+\text{J}} - M_{-\text{J}} \tag{3}$$

where

$$L_{0\text{J}} = \frac{\mu_0}{2\pi} l_{\text{tot}} \left[\ln \frac{l_{\text{tot}}}{n(w+s)} - 0.2 \right]$$

$$M_{-\text{J}} = \frac{0.47 \mu_0 l_{\text{tot}} n}{2\pi}$$

$$M_{+\text{J}} = \frac{\mu_0}{2\pi}\, l_{\text{tot}} (n-1) \ln\left(\sqrt{1+x^2} + x\right) - \sqrt{1 + \frac{1}{x^2}} + \frac{1}{x}, \quad x = \left(\frac{l_{\text{tot}}}{4 n d^+}\right)$$

$$d^+ = (w+s) \frac{(3n - 2N_i - 1)(N_i + 1)}{3(2n - N_i - 1)}$$

with N_i being integer part of n, w is metal width and s is spacing between segments, as previously was mentioned. On the other hand, expressions obtained by Asgaran *et al* [12] are similar to that in (3), except that, instead of taking total length of the inductor, it considers the average diameter in the model, which is given by [12].

$$L_{\text{A}} = L_{0\text{A}} + M_{+\text{A}} - M_{-\text{A}} \tag{4}$$

where

$$L_{0\text{A}} = \frac{2\mu_0 n}{\pi} \left\{ d_{\text{avg}} \left[\frac{1}{2} + \ln\left(\frac{2 d_{\text{avg}}}{w}\right) \right] + 0.178 w \right\}$$

$$M_{-\text{A}} = \frac{2\mu_0}{\pi} 0.47 n^2 d_{\text{avg}}$$

$$M_{+\text{A}} = \frac{2\mu_0}{\pi} \{ N_i (2n - N_i - 1) d_s \left[\ln \frac{2 d_s}{w+s} - 1 \right] - 2 d_s \left[\ln P + (n - N_i) \ln N_i! \right] + (w+s) \times \times \frac{\sqrt{2} - \ln(1+\sqrt{2})}{3} N_i (N_i + 1)(3n - 2N_i - 1) \}$$

$$P = 1!, 2!, \ldots, (n-1)!, \quad d_s = d_{\text{avg}} + \frac{w}{2}.$$

3 Experimental implementation

Different square-shaped inductors were designed and fabricated in TSMC (Taiwan Semiconductor Manufacturing Company) $0.35\mu m$ CMOS technology process (the presented methodology can be extended to any standard CMOS process). These inductors were used to obtain the adjustment factors Δ_s, Δ_w, Δ_n and $\Delta_{d_{\text{out}}}$, which ones are about physical dimensions of inductors that have variations due manufacturing process, for instance Δ_s is about distance between segments, Δ_w is about segments width, etc. They were built with the top-metal layers,

Table 1. Integrated inductors sizing

Inductor	s (μm)	w (μm)	d_{out} (μm)	n (-)
1	3.0	15.0	145	3.25
2	5.0	5.0	160	2.5
3	5.0	5.0	190	6.5
4	3.0	10.0	200	3.0

Table 2. Inductance values in nH

Inductor	L_{MW}	L_{MC}	L_{J}	L_{A}	Measured
1	1.02	1.03	0.93	1.05	1.5
2	1.84	1.88	1.83	1.95	2.1
3	7.11	7.06	6.13	7.11	11.5
4	2.70	2.69	2.89	2.70	3.0

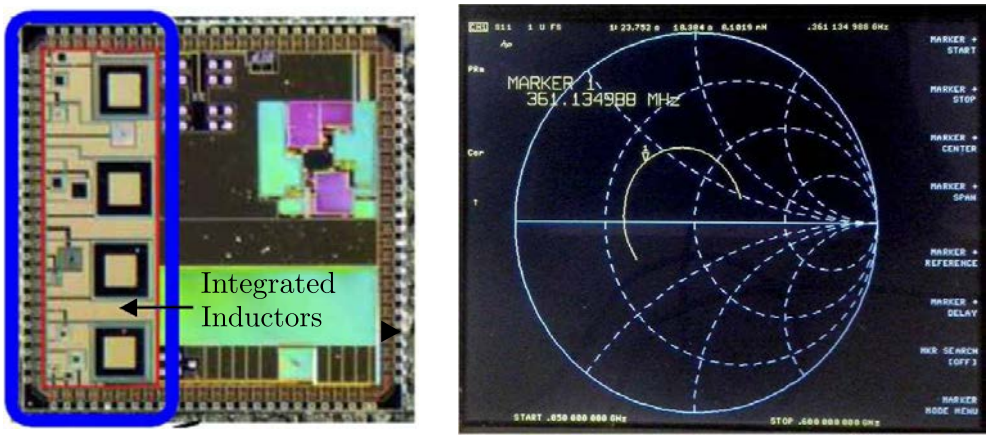
Table 3. Estimated,initial error in %

Inductor	MW	MC	J	A
1	31.49	31.25	37.68	29.74
2	12.03	10.16	12.73	6.96
3	38.11	38.58	46.64	38.14
4	9.78	10.1	3.41	9.71

Table 4. Error after the optimization in %

Inductor	MW	MC	J	A
1	0.00	0.00	0.00	0.00
2	0.00	2.15	0.00	1.03
3	6.06	0.00	0.00	0.00
4	4.38	2.79	5.96	0.00

MW, MC – Mohan, J – Jenei, A – Asgaran



(a) (b)

Fig. 2. Integrated inductors: (a) – microphotograph of the fabricated inductors in a multi-project chip, (b) – illustrating the inductors characterization in a network analyzer

Fig. 2(a) shows the microphotograph of the multi-project chip – which includes other subcircuits not related to this work – highlighting fabricated inductors, corresponding inductors sizes are shown in Tab. 1.

Experimental characterization was carried out by using a network analyzer HP8719D, a synthesized signal generator HP8664A and a MXA signal analyzer N9020A. As an illustration, Fig. 2(b) shows the Smith chart s_{12} parameter measured from network analyzer, while Tab. Tab. 2 shows the inductance values obtained for models given in (1) to (4) as well as their corresponding experimental measured values of fabricated inductors.

The difference between model and experimental measurements are computed as a percent error, defined as $(L_{se} - L_{sm})/L_{se}$, where L_{se} and L_{sm} are respectively the experimental and the model inductance values, as can be seen in Tab.2(a).

4 Error Reduction Procedure

Starting from the error values in Tab. 1 the proposed optimization algorithm depicted in Fig. 3 is applied to determine the corresponding adjustment factors in an iterative way. In order to determine the best values of them, the optimization algorithm proceeds iteratively, starting from Δ_s, Δ_w, Δ_n and $\Delta_{d_{\text{out}}}$, with an initial aleatory value. Afterwards, the error corresponding to the difference between the model estimation and the real experimental inductance value for each inductor is determined, a new aleatory value for adjustment factors is proposed, considering that every individual error must be reduced for all inductances at each iteration of the optimization procedure.

Process is repeated until a minimum error is achieved corresponding to a given tolerance . In order to optimize

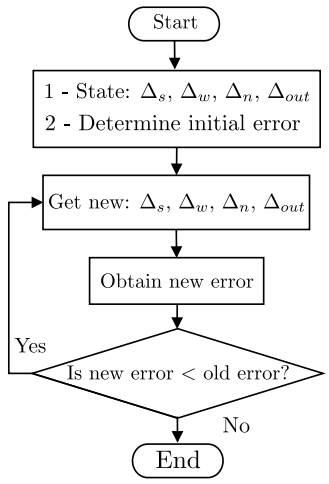


Fig. 3. Inductance error reduction algorithm

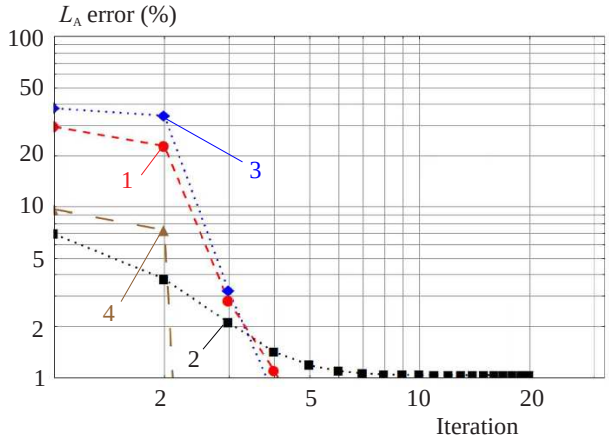


Fig. 4. Illustrating the error reduction process for L_A – Asgaran.

and to speed up the procedure, the so-called *gradient-based* method [15] is used in order to find out a local minimum with a low computational cost. Outcome of this optimization adjustment factors is shown in Tab. 5, where applying these factors to the models, the percent error associated to estimated series inductance is reduced in the most of the cases to 0%, being highest error the 6.06% as shown in Tab. 3. As an illustration of the optimization procedure, Fig. 4 shows the error reduction obtained by applying the algorithm to the L_A – Asgaran, series inductance. For this case, we have that in just five iterations the biggest percent error for the inductor No. 3 goes down from 38.14% to 0.0%. Optimization algorithm for the inductor No. 1, for all inductor models, gives a reduction error that goes from 32.5% as average to 0.0%.

Table 5. Optimized adjustment factors

Model	Δ_s	Δ_w	Δ_n	$\Delta_{d_{\text{out}}}$
Mohan W	1.2092	7.2173	0.0770	0.7609
Mohan C	0.3744	1.6050	0.2941	0.7445
Jenei	0.1097	0.4182	1.0815	0.7762
Asgaran	-1.2247	1.1708	0.5534	0.9646

Conclusions

An optimization-based methodology has been presented in order to find out a more accurate estimation of the series inductance in integrated inductors by means of adjustment factors that compensate fabrication variations of inductors, it is intended to be an useful tool during early design stages providing adjustment factors that are easily added to the well known inductance models, predicting more accurate inductance values. Experimental results are shown for a number of square integrated inductors with diverse sizes and geometry parameters, and used to obtain the mentioned adjustment factors, that allow an important error reduction as can see for Jenei model with a maximum of 46.64% to zero, thus validating the presented approach which can be extended to optimize the design of inductors in whatever RF CMOS circuit.

Acknowledgments

This work was partially supported by the National Council of Science and Technology of México (CONACYT) and by the Spanish Ministry of Economy and Competitiveness (with support from the European Regional Development Fund) under contract TEC2013-45638-C3-3-R, and by "Consejería de Economía, Innovación, Ciencia y Empleo de la Junta de Andalucía", under contract P12-TIC-1481.

References

[1] S. Onoe, "Evolution of 5G Mobile Technology Toward 2020 and Beyond IEEE International Solid-State Circuits Conference ISSCC, 2016, pp. 23-28 (DOI: 10.1109/ISSCC.2016.7417891).

[2] S. Vandebroek, "Three Pillars Enabling the Internet of Everything: Smart Everyday Objects, Information-Centric Networks, and Automated Real-Time Insights IEEE International Solid-State Circuits Conference ISSCC, 2016, pp. 14-20 (DOI: 10.1109/ISSCC.2016.7417889).

[3] A. M. Niknejad and R. G. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for Si RF ICs IEEE Journal of Solid-State Circuits vol. 33, no.10, pp. 1470-1481, 1998 (DOI: 10.1109/4.720393).

[4] S. Chakraborty, V. Ivanov, J. Einzinger, R. P. Aditham, D. LeDeaut, J. -F. Ren, H. -S. Kim, C. Kuch, G. Dietz, M. Goel and J. Graul, "An Ultralow power, Low-cost, Multi-standard Transceiver IEEE Wireless and Microwave Circuits and Systems Symposium WMCS, 2015, pp. 1-5 (DOI: 10.1109/WMCaS.2015.7233220).

[5] "[F. Ellinger Radio frequency integrated circuits and technologies, Springer Science & Business Media, 2008.

[6] D. Pietron, T. Borejko, K. Siwiec and W. A. Pleskacz, "Importance of on-chip inductor modeling radio frequency integrated circuits IEEE Mixed Design of Integrated Circuits and Systems International Conference, MIXDES-24th, 2017, pp. 398-403 (DOI: 10.23919/MIXDES.2017.8005240).

[7] E. Sano, K. Inafune and M. Akazawa, "RF CMOS inductor shielded by a high-impedance surface IEICE Electronics Express vol. 1, no.8, pp. 233-236, 2004 (DOI: 10.1587/elex.1.233).

[8] C. P. Yue, C. Ryu, J. Lau, T. H. Lee and S. S. Wong, "A physical model for planar spiral inductors on silicon IEEE International Electron Devices Meeting IEDM'96, 1996, pp. 155-158 (DOI: 10.1109/IEDM.1996.553144).

[9] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon IEEE Transactions on electron devices vol. 47, no.3, pp. 560-568, 2000 (DOI: 10.1109/16.824729).

[10] S. S. Mohan, M. del-Mar-Hershenson, S. P. Boyd and T. H. Lee, "Simple accurate expressions for planar spiral inductances IEEE Journal of solid-state circuits vol. 34, no.10, pp. 1419-1424, 1999 (DOI: 10.1109/4.792620).

[11] S. Jenei, B. K. Nauwelaers and S. Decoutere, "Physics-based closed-form inductance expression for compact modeling of integrated spiral inductors IEEE Journal of Solid-State Circuits vol. 37, no.1, pp. 77-80, 2002 (DOI: 10.1109/4.974547).

[12] S. Asgaran, "New accurate physics-based closed-form expressions for compact modeling and design of on-chip spiral inductors IEEE Microelectronics The 14th International Conference on 2002-ICM, no.1, pp. 247-250 (DOI: 10.1109/ICM-02.2002.1161540).

[13] M. B. Amor, M. Loulou, S. Quintanel and D. Pasquet, "An integrated 0. 35 ?m CMOS technology inductor for wideband LNA application IEEE Telecommunications International Conference, ICT'09, 2009, pp. 313-317 (DOI: 10.1109/ICTEL.2009. 5158665).

[14] H. [14] and Greenhouse, "Design of planar rectangular microelectronic inductors IEEE Transactions on parts hybrids, and packaging, vol. 10, no.2, pp. 101-109, 1974 (DOI: 10.1109/TPHP. 1974.1134841).

[15] J. Snyman, "Practical mathematical optimization: an introduction to basic optimization theory and classical and new gradient-based algorithms Springer Science & Business Media vol. 97, 2005.

Received 21 March 2018

Eric F. Gutierrez Frias received the BSc degree in Communications and Electronic Engineering and MSc degree in Electronic and Computer Engineering from University of Guadalajara, México in 2012 and 2015 respectively. Currently he is working toward the PhD degree in electronic and computer sciences at the University of Guadalajara. His current research interests include power amplifier and optimization of analog circuits.

Luis A. García Lugo received the BSc degree in Communications and Electronic Engineering from University of Guadalajara, México and MSc degree in Electrical Engineering in Semiconductors from the Center for Research and Advanced Studies of the National Polytechnic Institute, México in 1997 and 2001 respectively. He worked as quality, device and product engineer for Motorola, On Semiconductor, Siemens VDO and Hitachi GST, where he was involved in fabrication and testing of discrete semiconductor devices as power rectifiers, MOS and bipolar transistors as well as sliders for hard disk drives. He is a final year student of PhD studies in Electronic and Computing Sciences at the University of Guadalajara. The fields of his interest are low-noise amplifiers and sigma-delta modulators.

Edwin C. Becerra Alvarez received the BSc degree on Communications and Electronic Engineering from the University of Guadalajara, Mexico in 2004, the MSc degree on Electric Engineering from CINVESTAV, Mexico in 2006 and the PhD degree on Microelectronics from the University of Seville, Spain in 2010. Since 2010 he is working in the University of Guadalajara and his current research interests are on CMOS RF circuits.

Juan J. Raygoza Panduro received the BSc degree in Communications and Electronics from the University of Guadalajara, the MSc degree from the Center of Research and Advanced Studies of the IPN, Zacatenco, México. He received his PhD degree in Computer Science and Telecommunications from Autonomous University of Madrid, Spain. He worked for IBM and participated in the technological transfer of manufacturing hard disk heads, from San Jose, USA to Guadalajara, México. He specializes in the design of digital architecture based on FPGAs, Microprocessors, embedded system and bioelectronics. He is Professor at CUCEI; University of Guadalajara, his lines of research are: Electronic Systems Applied to Biomedicine, Neuroengineering, Microprocessor Design, Digital Control and Embedded system.

José M. de la Rosa received the MSc degree in Physics in 1993 and the PhD degree in Microelectronics in 2000, both from the University of Seville, Spain. Since 1993 he has been working at the Institute of Microelectronics of Seville (IMSE), which is its turn part of the Spanish Microelectronics Center (CNM) of the Spanish Council of Scientific Research (CSIC). He is presently the vicedirector of IMSE and he is also a Full Professor at the Dept. of Electronics and Electromagnetism of the University of Seville. His main research interests are in the field of analog and mixed-signal integrated circuits, especially high-performance data converters, including analysis, behavioral modeling, design and design automation of such circuits.

Edgardo B. Ortega Rosales received the BSc and MSc degrees in Electronics Engineering from the University of Guadalajara, México, in 1997 and 2004, respectively. He received the PhD degree in 2016 from the Centre of Research and Advanced Studies (CINVESTAV), México. He was a special student in 1998 at Gettysburg College while working as an assistant professor in Gettysburg, Pa, USA. He worked at the University of Guadalajara as a professor from 1999 to 2011. Currently, he is working at the Technological University of the Metropolitan Area of Guadalajara. He is interested in analog and RF circuit design areas for integrated communication systems.