

Mixed-Signal Map-Configurable IC Chaos Generator for Digital Communication Systems

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Abstract - In this paper, the methodological aspects for the design of mixed-signal map-configurable chaos generators are presented. Such techniques have been applied in the integration, embedded in a complete FM-DCSK modem, of a chaos generator which achieves 10 bits resolution at a maximum clock frequency of 20Mhz, from a 3.3V power supply.

I. INTRODUCTION

In the scenario of digital communications based on chaotic modulation, chaos generators play a prominent role as they provide the required sample functions to which information symbols are mapped to. In these systems, chaotic signals, instead of periodic waveforms, are used as *communication carriers* which, based on the wideband and noise-like spectral properties of chaos, can provide simultaneous *spreading* and *modulation* of the digital information. Since the processing gain, as a measure of the signal spreading, and the modulation process itself are severely constrained by the limited transmission bandwidth and the need for a low error rate performance, the *statistical properties* of the chaotic carriers must be carefully considered.

Yet another important requirement which must be considered is, obviously, the *suitability* of the chaos generator for electronic implementation. This is particularly stressing in an integrated circuit context where system tunability is intrinsically reduced. Because of the limited accuracy of any analog circuit implementation, models for chaos generators must be *robust* enough so that the unavoidable parameter perturbations do not severely degrade the prescribed statistical features nor the whole modulator functionality. Moreover, even if robustness is guaranteed by design, high accuracy chaotic waveform generation can only be achieved through the application of calibration and/or error correction techniques.

All the above considerations, as well as some additional constraints, have been applied on the mixed-signal chaos generator described herein. Such generator has been integrated, embedded in a FM-DCSK modem (details of

this modulation scheme can be found in [1]), in a 0.35 μ m 2P-3M CMOS technology. The chaos generator is autonomous, uses Switched-Capacitor (SC) sampled-data techniques (for a strict timing control of the modem) and achieves 10 bits resolution at a maximum clock frequency of 20Mhz, from a power supply voltage of 3.3V. Additionally, it can be electrically configured to implement different elements of the family of 1-D *Piece-Wise Affine Markov* (PWAM) maps [2], in order to extend the versatility of the chip under different communication links.

The paper focuses on the methodological aspects of the designed chaos generator and is organized in two main parts. Sec.II gives details on the selection of the chaos generator attending to the specifications arranged for the overall FM-DCSK modem. Considerations on robustness and accuracy are also addressed. In Sec.III, a generic architecture for the implementation of 1-D PWAM maps is proposed and the general procedure for configurability is illustrated with the particular chaos generator used in the modem. Finally, Sec.IV gives some concluding remarks.

II. SELECTION AND CHARACTERIZATION

In the FM-DCSK scheme, special care must be devoted to two particular statistical properties of chaos namely, its probability density function (PDF) and the auto-correlation function (ACF). Since the communication carrier is chaotic, its PDF directly affects the power spectrum profile of the transmitted signal. On the other hand, because signal recovery is achieved by cross-correlating two delayed copies (with equal or opposite signs) of the same sample function, the ACF properties determine the variance of the detection signal which is used to estimate the transmitted data [1]. From this, it can be concluded (and demonstrated by behavioral simulation of the designed FM-DCSK modem) that the PDF of the chaotic signal should be flat in order to guarantee *uniform spreading* of the information and hence a balanced coverage of the transmission band. Also, the chaotic waveform should exhibit *exponentially decaying delta-like* ACF (equivalently, a white noise-like power spectral density, PSD) to improve the noise performance of the receiver. Indeed, for the targeted FM-DCSK implementation, it has been found that the flatness of the chaotic signal PSD can tolerate up to ± 0.5 dB of maximum deviation from DC to about half the sampling frequency. Other requisites which must be also considered are robustness and adequate interfacing to the other blocks of the modem.

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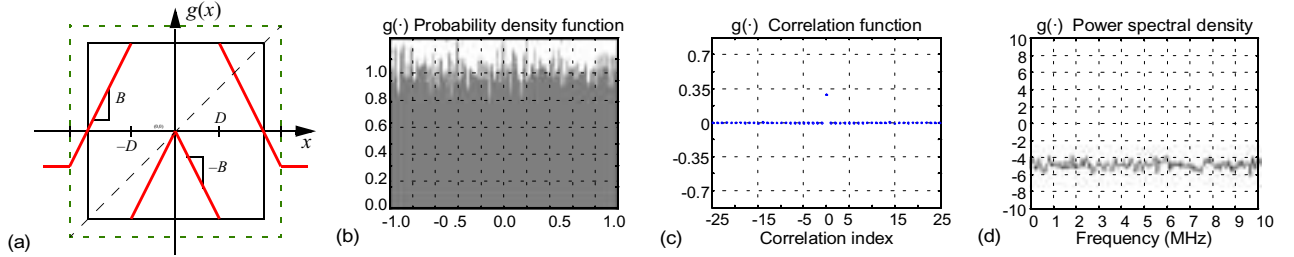


Fig. 1 (a) PWAM map suitable for FM-DCSK modulation; (b-d) Bifurcation diagram, short-term correlation function and power spectral density of the map.

Bearing all these selection criteria in mind, an exhaustive exploration within the family of PWAM maps with four uniformly partitioned non-overlapping intervals have been realized. Results were presented in [3] where a list of necessary conditions for a PWAM map to serve for chaos communication applications were given. Fig.1(a) shows an interesting solution found in this exploration. This map avoids the onset of parasitic stable equilibrium points and parasitic stable limit cycles, hence guaranteeing a correct system start-up and robust operation, as long as saturation levels can be re-injected into the invariant set of the map (solid box in Fig.1(a)) [3]. This can be done by properly setting parameter D which, otherwise, acts as a scaling factor of the output waveforms. Additionally, because all segments of the characteristics have the same slope in magnitude, B , and the partition of the interval is uniform, circuit implementation can be simplified using a block sharing strategy. Most important, for B around 2, the map exhibits a quasi-uniform PDF (Fig.1(b)), a delta-like ACF function (Fig.1(c)) and its PSD remains flat with deviations below ± 0.5 dB (Fig.1(d))^{†1}. Hence, the map in Fig.1(a) is a good candidate for the proposed FM-DCSK modem.

Unfortunately, as in any other chaos generator implementation, performance degrades (in particular, the PDF is the most affected statistical measure) as the map deviates from the ideal characteristics of Fig.1(a). To cope with this problem, high accuracy IC techniques should be used to keep partition mismatch, breakpoints misalignment and slope deviations below tolerable margins (see footnote 1). Further, it has been claimed [4] that maps in which a breakpoint inverting the slope of the characteristics is placed on the identity axis (as occurs in Fig.1(a)) may get lock at a parasitic trapping region, leading to a complete loss of ergodicity. Certainly, this may occur in the rather unlikely situation where there is no breakpoint misalignment or, referring to Fig.1(a), when the breakpoint at the origin remains continuous in spite of all the nonidealities, including noise, that appear in practice. From our view, the most

1. Simulations of Figs.1(b-d) correspond to a sample of a 100 run monte-carlo dynamic analysis of the map in Fig.1(a), where all the aforementioned non-ideal effects (assuming, respectively, 10 bits equivalent accuracy) and noise (with levels below half LSB) have been included. The remaining samples of the analysis do not reveal substantial differences with that shown in Figs.1(b-d).

serious drawback on the implementation of Fig.1(a) is the high accuracy demanding situation previously drawn (in correspondence to the severe specifications required by the application). This situation, however, is largely alleviated in the chaos generator architecture presented in Sec.III.

One final remark is related to the interface of the chaos generator with the remaining blocks in the FM-DCSK modulator. Because such interface is essentially digital, the chaos generator not only must internally operate in analog manner, but also must provide quantized versions of the iterates in the form of digital words. The length of the digital output words, i.e., the resolution of the chaos generator, is determined on the one hand, by the tolerances of its prescribed statistical features and, on the other, by the maximum allowable ripple on the transmission bandwidth. By behavioral simulations of the modem in an AWGN channel environment including major circuit non-idealities, it has been found that 10 bits resolution suffices to achieve the target performance of a BER below 10^{-3} with an E_b/N_0 less than 14dB. For similar reasons, it has been found that for a 500 kbps digital transmission, the chaos generator must operate at throughput rate of 10-20 Msamples/s.

III. GENERIC ARCHITECTURE

Fig.2 shows the conceptual block diagram of the proposed 1-D PWAM map realization. It consists of a discrete-time feedback architecture formed by a sample-and-hold amplifier, which implements the delay operation of the map, and a nonlinear circuitry, which obtains the next iterate of the sampled variable from its previous value. Assuming that the PWAM map consists of n segments, the circuit operation can be described as follows. The sampled and held signal V_{sh} is quantized by a flash-type sub-ADC to generate a coarse thermometer-coded digital output of $r = \lceil \log_2(n) \rceil$ equivalent bits resolution, which uniquely identifies each segment of the PWAM map. Decision levels of the sub-ADC correspond to the partition points of the PWAM characteristics. Following the flash sub-ADC section, a binary encoder circuitry converts the thermometer format to a 1-of- n code and suppresses the effects of possible metastable errors. Then, a DAC transforms the quantized digital information back to analog domain using the 1-of- n code to select the restoring configuration. This code is simultaneously used to define the gain A of a pro-

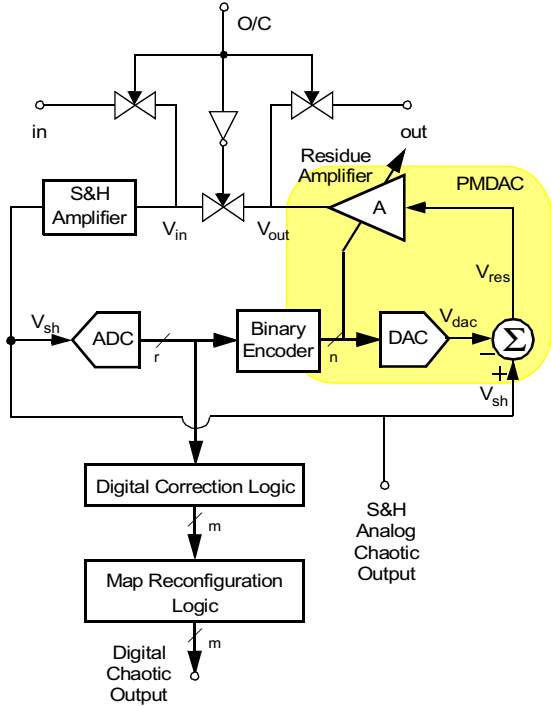


Fig. 2 Generic block diagram of a 1-D PWAM map realization.

programmable amplifier, which amplifies the residue signal V_{res} resulting from subtracting the output DAC value V_{dac} from the original input signal V_{sh} . In this way, the output signal of the nonlinear circuitry V_{out} takes the affine form

$$V_{out} = A(V_{sh} - V_{dac}) \quad (1)$$

where both A and V_{dac} depend on the segment indicated by the 1-of- n code. The different settings for A and V_{dac} can be digitally stored in dedicated RAMs, or calculated using proper combinatorial logic. The internal DAC and the programmable amplifier are commonly implemented in a single circuit, referred to as Programmable Multiplying DAC (PMDAC). Obviously, the higher the symmetry of the map, the lower the complexity of the PMDAC.

Accuracy requirements of the aforementioned building blocks are determined by the resolution of the chaos generator. Obviously, the maximum achievable resolution imposes an upper limit on the number of segments of the PWAM characteristics, and a lower limit on the length of the partition intervals. This clarifies the concept of suitability for electronic implementation and justifies the apparently short scope exploration of PWAM maps described in the previous section.

Interestingly enough, the thermometer codes obtained from the sub-ADC can be seen as a *symbolic dynamics* of the underlying map, as there is a one-to-one correspondence between such codes and the segments of the PWAM application. Hence, the architecture of Fig.2 not only provides the analog value of the iterations (it can be taken at the output of the sample-and-hold amplifier) but also a dig-

ital representation of the map dynamics. As shown below, this capability of digital code generation can be exploited to solve the interface between the chaos generator and the FM-DCSK modulator, precluding the need of an extra A/D conversion block.

Once in digital domain, the digital correction logic (DCL) block is used to construct representative digital outputs of the chaos generator; and the resulting output stream conveniently modified, at the map reconfiguration logic (MRL) block, to alter the statistical properties of the map.

The DCL block combines the most recent thermometer codes provided by the sub-ADC with those obtained in previous iterations to synthesize digital quantized versions of the analog iterations of the map. Because the DCL employs binary arithmetic, its implementation largely simplifies if the settings for A are multiple of 2, as it is the case of Fig.1(a). The number of codes which have to be combined depends on m , i.e., the resolution of the chaos generator, and the effective resolution of the sub-ADC, r_{eff} ^{†2}. The throughput rate of the DCL is thus one digital word per iteration with a latency of $\lceil m/r_{eff} \rceil$ cycles. The DCL block also incorporates a mechanism to generate correct digital outputs even if iterations eventually escape from the map attractor as a consequence of any offset-induced error in the flash ADC section (re-injection to the invariant set of the map must be guaranteed by design). The operation principle of the correction mechanism is beyond the scope of this paper, and can be found in many textbooks on A-to-D conversion (for instance, [5]).

On the other hand, the MRL block can be seen as a digital signal conditioning circuit which modifies the digital outputs from the correction block to accomplish any prescribed statistical feature. Its relevance and versatility mainly manifests if the application only exploits the digitized version of the map iterations for subsequent processing, as it is the case in the proposed FM-DCSK modulator. Even more important, the digital-domain configuration capability allows that the map implemented in the analog loop can be conveniently altered in order to relax the specifications of some of its building blocks. In other words, the analog loop in Fig.2 can be made as simple as possible, whenever it behaves as a robust source of chaos, because the more cumbersome, hardware-intensive tasks can be relied to the MRL block. This has been actually the approach followed in the implementation of Fig.1(a).

Assume that the analog building blocks of Fig.2 are configured to implement the nonlinear characteristic of Fig.3(a) with B around 2 and parameter D chosen so that

2. A sub-ADC with r bits resolution is able to index up to 2^r segments. Hence, if the number of segments of the characteristics is even, all the thermometer codes of the sub-ADC are used to codify corresponding segments and, we have $r_{eff} = r$. On the other hand, if the number of segments is odd, one of the bits of the sub-ADC is redundant because only $2^r - 1$ codes from the 2^r available are used to codify the segments of the PWAM map. In this case, we have $r_{eff} = r - 1$.

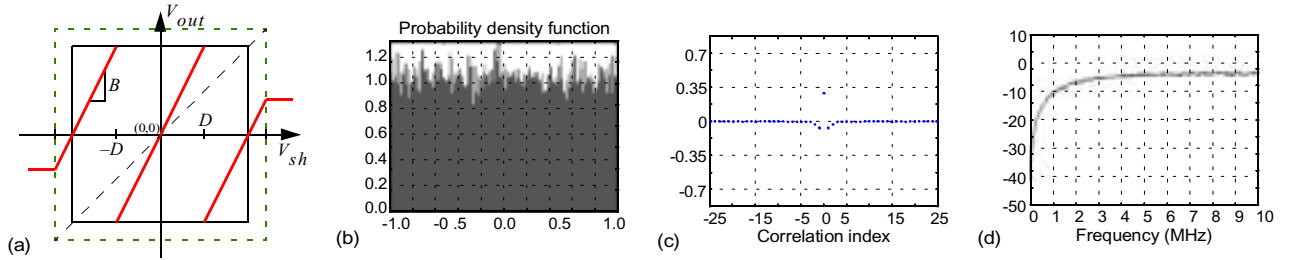


Fig. 3 (a) Rotated Bernoulli shift map; (b-d) Probability density function, short-term correlation function and power spectral density of the map.

the invariant interval of the map remains confined within the saturation levels of the circuit. It can be seen as a rotated version of the well-known *Bernoulli-shift* map, with three segments of identical slopes. This map clearly leads to a simpler implementation as compared to Fig.1(a) because there is no need for a reverse polarity device in the programmable amplifier of Fig.2, and the number of segments is reduced by one (a simpler sub-ADC is required).

The statistical properties of the map in Fig.3(a), though it shows a reasonably flat PDF (see Fig.3(b)), clearly deviate from the specifications of delta-like ACF and maximally-flat PSD (see Figs.3(c-d))^{†3}. However, using an appropriate MRL block, the statistics of the map in Fig.1(a) can be easily recovered (within the resolution of the chaos generator). Concretely, if d_k and c_k are, respectively, the input and output words of the MRL block at the k -th iteration; its operation is described as

$$c_k = \begin{cases} d_k & d_{k-1} < 0 \\ -d_k & d_{k-1} > 0 \end{cases} \quad (2)$$

Fig.4 shows the short-term correlation function (Fig.4(a)) and the power spectral density (Fig.4(b)) of the signal obtained by digitally configuring the output digital codes generated by the rotated Bernoulli-shift map of Fig.3(a). As can be seen, no substantial difference exists with respect to equivalent measures of Fig.1.

Another interesting property of the nonlinearity of Fig.3(a) is that it can be seen as the residue transfer function of a single stage in a 1.5 bit/stage pipeline ADC. This means that the structure of Fig.2 can be transformed into an A/D converter with an adequate timing scheme. Actually, the switch arrangement between the residue and sample-and-hold amplifiers in Fig.2 has the purpose of selectively

3. Simulations of Figs.3(b-d) correspond to a sample of a 100 run monte-carlo dynamic analysis of the map in Fig.3(a) after the digital correction logic process. Referring to Fig.2, the programmable gain and the sample-and-hold amplifiers have been assumed to achieve 11 bits equivalent accuracy, whereas the accuracy of the sub-ADC and the internal DAC is of only 6 bits (the correction mechanism is able to exactly correct the partition mismatch and the breakpoints misalignment). The remaining samples of the analysis confirm the features shown in Figs.3(b-d).

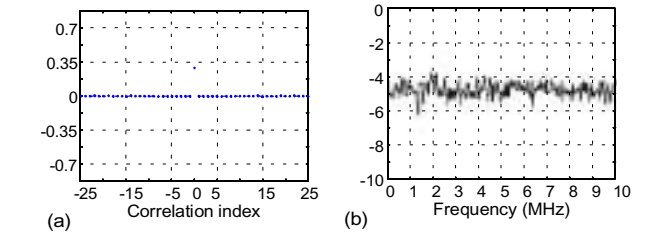


Fig. 4 Digitally configured PWAM map obtained from the Bernoulli-shift map of Fig.3. (a) Short-term correlation function and (b) power spectral density of the map.

open or close the analog loop of the circuit, so that it can correspondingly operate as an A/D converter or an autonomous chaos generator. This increases the testability of the generator, and allows that any other off-chip chaotic source can drive the modem FM-DCSK.

IV. CONCLUDING REMARKS

In this paper, the methodological aspects for the design of fast and accurate mixed-signal map-configurable IC chaos generators, with emphasis on digital communication applications, are presented. Techniques are extensible to other applications and solve the lack of robustness found in other PWAM maps integrated realizations.

V. REFERENCES

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