The EKV/ACM compact models for mismatch modeling down to 90nm and for new emergent non-CMOS nanotechnology FETs

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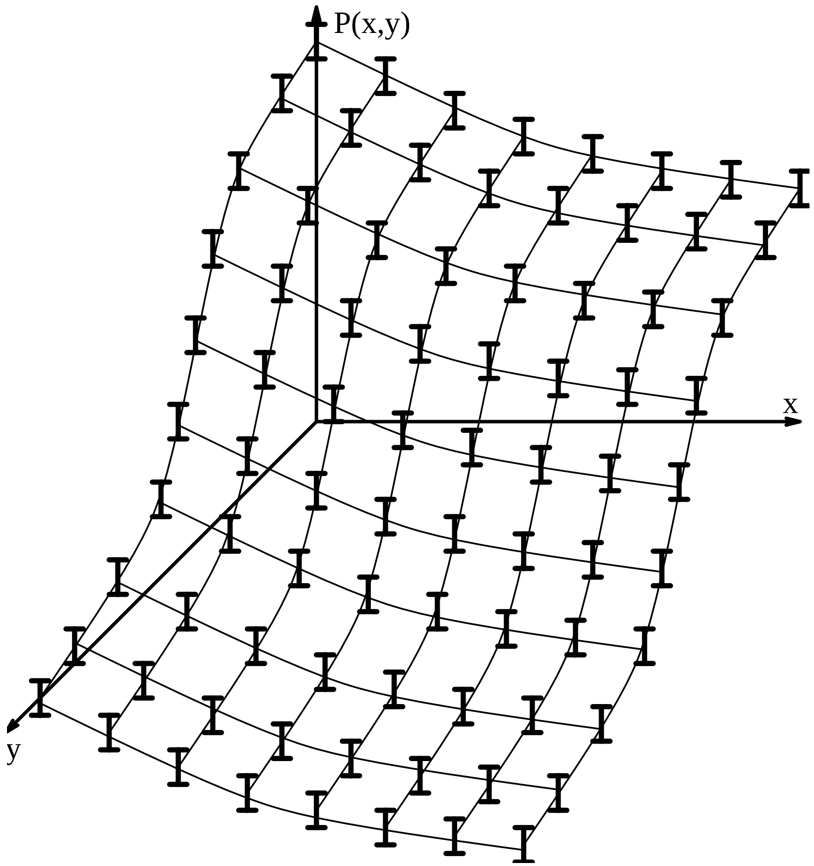
Outline

- Continuous Weak-to-Strong inversion models for mismatch
- Mismatch characterization chip
- Results for 0.35um CMOS
- Results for 90nm CMOS
- Simulating in Cadence-Spectre
- Modelling Pelgrom’s Distance Term Efficiently
- Extension of continuous CMOS models to new coming nano-FETs

The Mismatch Behavior



$$\sigma^2(\Delta P) = f_A(W, L) + f_D(D)$$

- $f_A(W, L)$ Small random, transistor size dependent component, 'true' mismatch component
- $f_D(D)$ Gradient surface, transistor distance dependent component, can be eliminated with layout techniques

Historical Perspective. Mismatch Models in Strong Inversion

$$\sigma^2(\Delta P) = f(W, L) + S_P^2 D^2$$

	$\sigma^2_{(\Delta\beta/\beta)}$	$\sigma^2_{(\Delta V_{T0})}$	$\sigma^2_{(\Delta\theta)}$		$\sigma^2_{(\Delta\gamma)}$
			$\sigma^2_{(\Delta\theta_o)}$	$\sigma^2_{(\Delta\theta_e)}$	
Pelgrom89	✓	✓	–		✓
Bastos98	✓	✓	✓		✓
Serrano99	✓	✓	✓	✓	✓

$$\Delta\theta = \Delta\theta_o + \frac{V_{DS}\big|_{sat}}{V_{GS} - V_T}\Delta\theta_e$$

$$\theta_o = \theta + 2\frac{\mu C_{ox} l_d R_{\square}}{L} \qquad \theta_e = \frac{\mu}{L}\left(\frac{1}{2v_s} - C_{ox} l_d R_{\square}\right)$$

A Continuous Transistor Model from Weak to Strong Inversion. The ACM Model

$$I_{DS} = I_s(i_f(V_P - V_S) - i_r(V_P - V_D))$$

$$V_P - V_{S(D)} = \phi_t(\sqrt{1 + i_{f(r)}} - 2 + \ln(\sqrt{1 + i_{f(r)}} - 1))$$

$$V_P = \frac{V_G - V_{TO}}{n}$$

$$n = 1 + \frac{\gamma}{2\left(\sqrt{V_G - V_{TO} + 2\phi_F + \gamma\sqrt{2\phi_F} + 1/4\gamma^2} - 1/2\gamma\right)}$$

$$I_S = I_S'n = \mu n C'_{ox}(W/L)\left(\phi_t^2/2\right)$$

- Continuous for all transistor operation regions
- Based on a reduced set of physically meaningful parameters $\{I_S, V_{TO}, \gamma, \phi_F\}$
- Drain/Source symmetric

Introducing Continuosly Second Order Effects

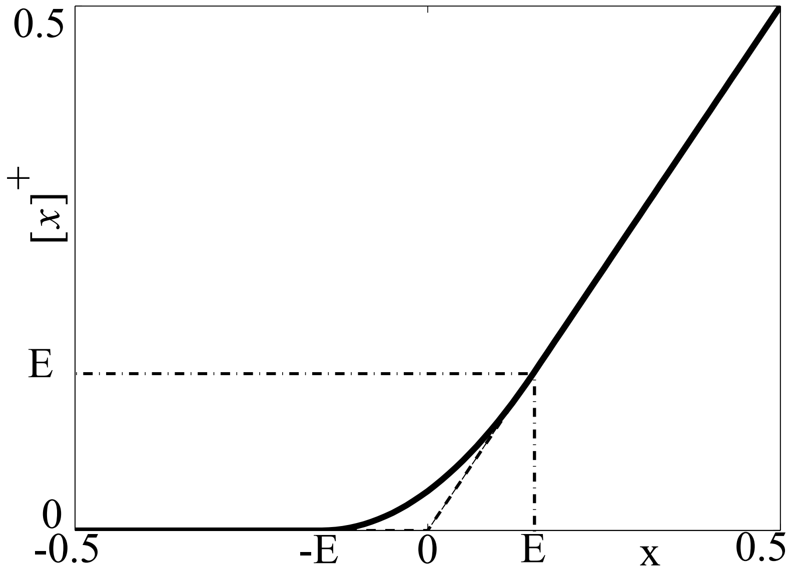
$$I_{DS} = \frac{I_S(i_f - i_r)(1 + \lambda(V_D - V_S))}{\left(1 + \theta_o [V_P - V_S]^+\right)\left(1 + \theta_e V_{DS_{eff}}\right)} \quad ,$$

traditionally,

$V_{DS_{eff}} = V_{DS}$ in ohmic region;

$V_{DS_{eff}} = V_P - V_S$ in saturation.

define smoothed rectification $[\ ]^+$



$$[x]^+ = \begin{cases} 0 \text{ if } x < -E \\ \dfrac{(x+E)^2}{4E} \text{ if } -E < x < E \\ x \text{ if } x > E \end{cases}$$

redefine

$$V_{DS_{eff}} = \left| [V_P - V_S]^+ - [V_P - V_D]^+ \right|$$

with $E = 0{,}3\, V_{DS}$

A Continuous Mismatch Model Valid from Weak to Strong Inversion

$$I_{DS} = \frac{I_S(i_f - i_r)(1 + \lambda(V_D - V_S))}{\left(1 + \theta_o[V_P - V_S]^+\right)\left(1 + \theta_e V_{DS_{eff}}\right)}$$

$$\Downarrow$$

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta I_S}{I_S} + \frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_P}\frac{\partial V_P}{\partial V_{T0}}\Delta V_{T0} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_P}\frac{\partial V_P}{\partial n} + \frac{1}{n}\right)\frac{\partial n}{\partial \gamma}\Delta\gamma + \frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta_o}\Delta\theta_o + \frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta_e}\Delta\theta_e$$

$$\Downarrow$$

$$\left\{\frac{\Delta I_S}{I_S}, \Delta V_{T0}, \Delta\gamma,\ \Delta\theta_o, \Delta\theta_e\right\}$$

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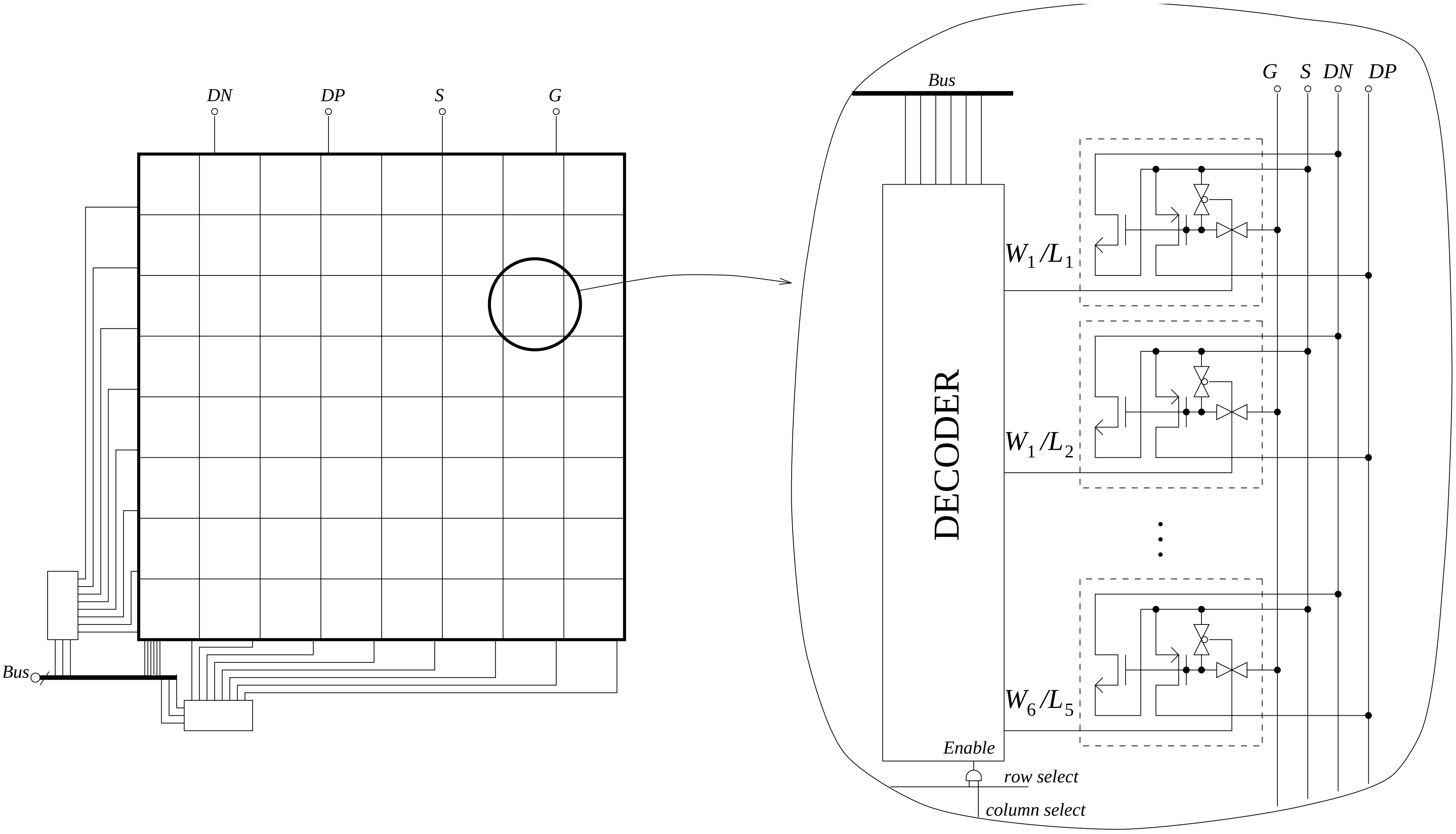
Mismatch Characterization Chip



Measuring Curves: 7 Measured Curves

- $V_{DS} = 1{,}65V$

  Curve 1: $I_{DS}(V_{GS})$, $V_{SB} = 0V$, $V_{GS} \in [0, 3{,}3]$

  Curve 2: $I_{DS}(V_{GS})$, $V_{SB} = 1V$, $V_{GS} \in [0, 3{,}3]$

- $V_{DS} = 0{,}1V$

  Curve 3: $I_{DS}(V_{GS})$, $V_{SB} = 0V$, $V_{GS} \in [0, 3{,}3]$

  Curve 4: $I_{DS}(V_{GS})$, $V_{SB} = 1V$, $V_{GS} \in [0, 3{,}3]$

- $V_G = 1{,}25V_S + \alpha$

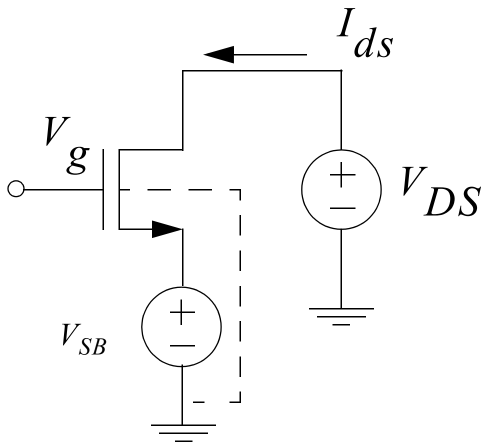
  Curve 5: $I_{DS}(V_S), \alpha = \alpha_1, V_S \in [0, 3{,}3]$

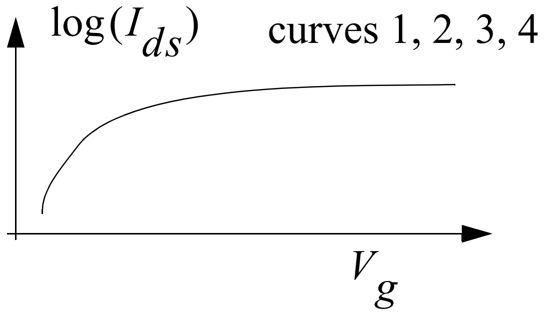
  Curve 6: $I_{DS}(V_S), \alpha = \alpha_2, V_S \in [0, 3{,}3]$

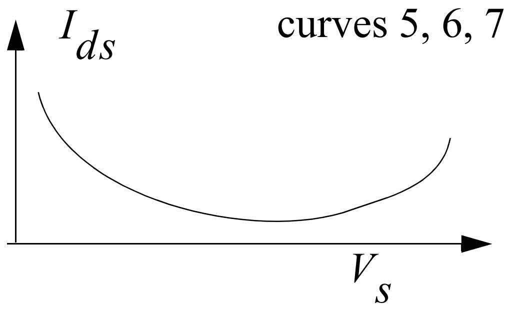
  Curve 7: $I_{DS}(V_S), \alpha = \alpha_3, V_S \in [0, 3{,}3]$

where:

α_1, α_2 and α_3 are values of V_G from curve 1 so that we are in weak, moderate and strong inversion respectively.







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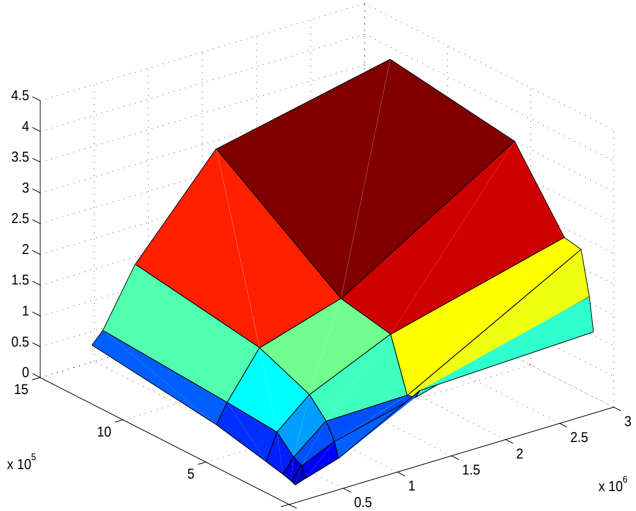
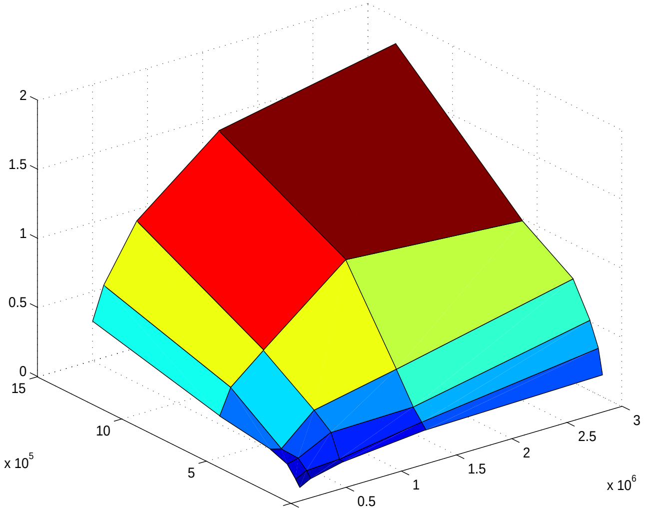
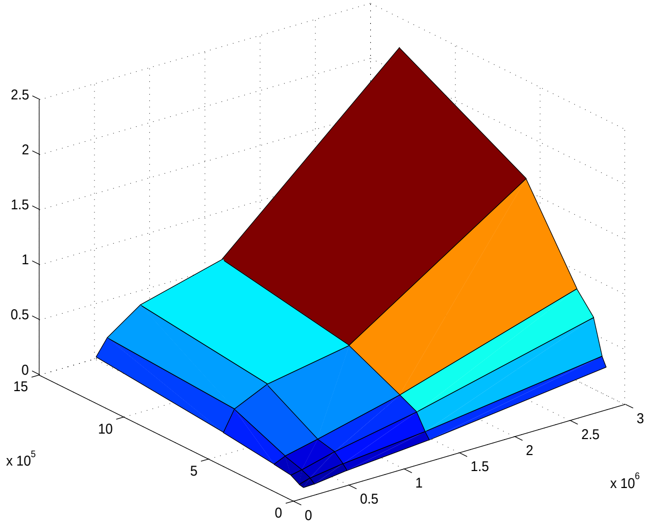
Computing Statistics



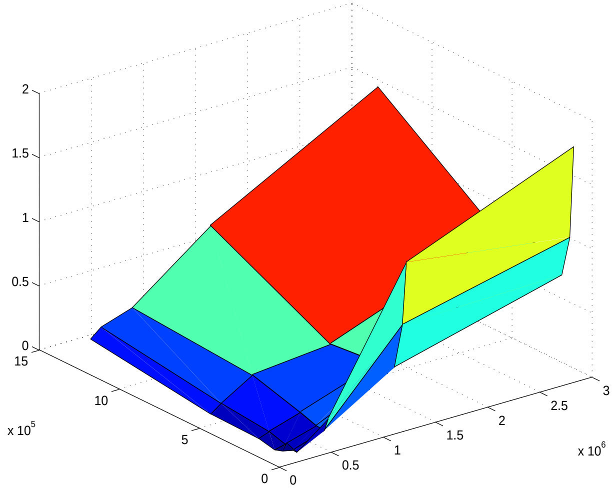
$\sigma(\Delta I_S/I_S)$



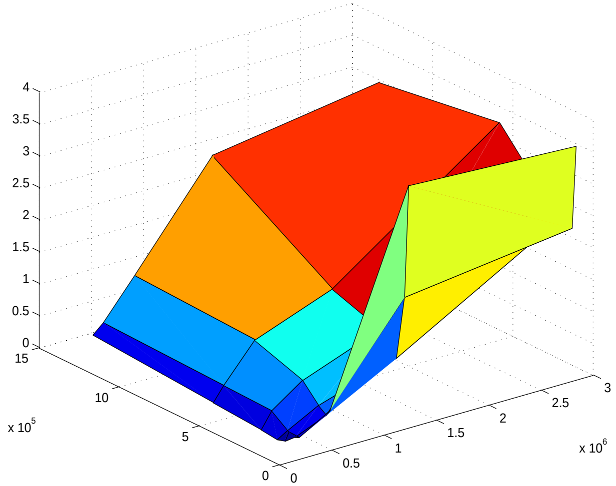
$\sigma(\Delta\gamma)$



$\sigma(\Delta V_{T0})$

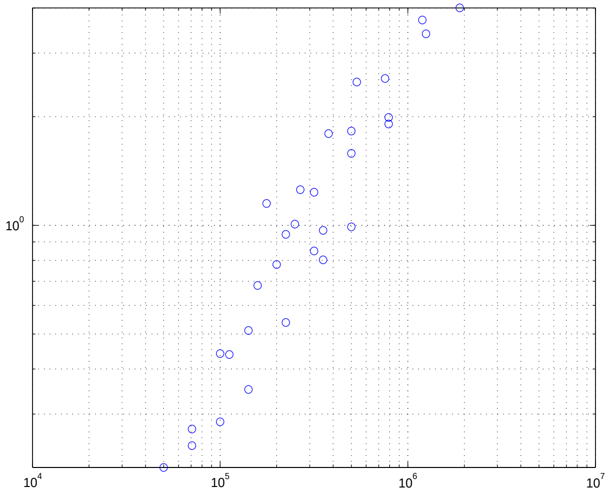


$\sigma(\Delta\theta_e)$

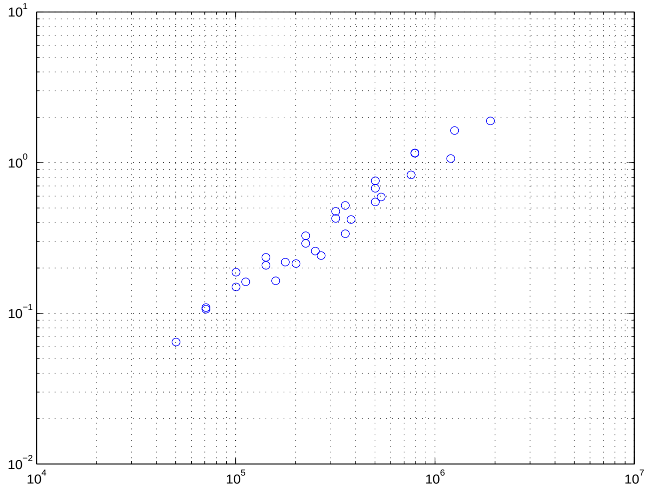


$\sigma(\Delta\theta_o)$

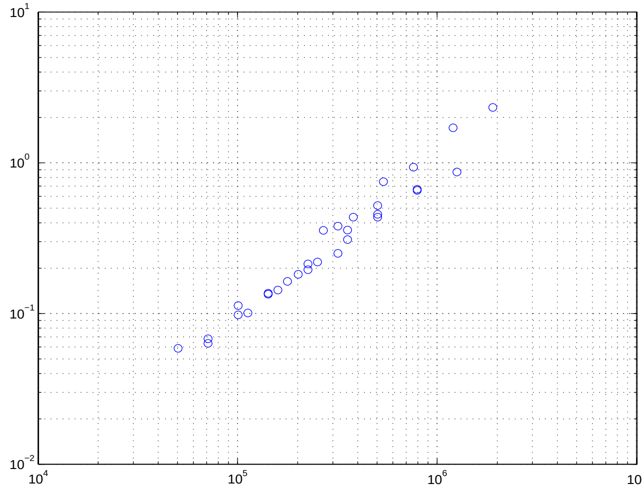
Computing Statistics



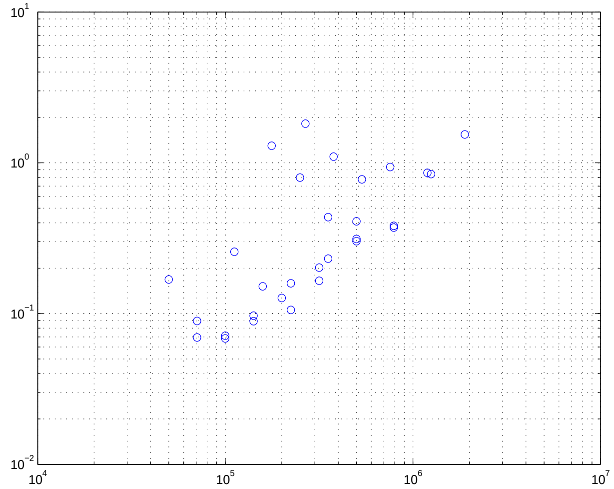
$\sigma(\Delta I_S/I_S)$



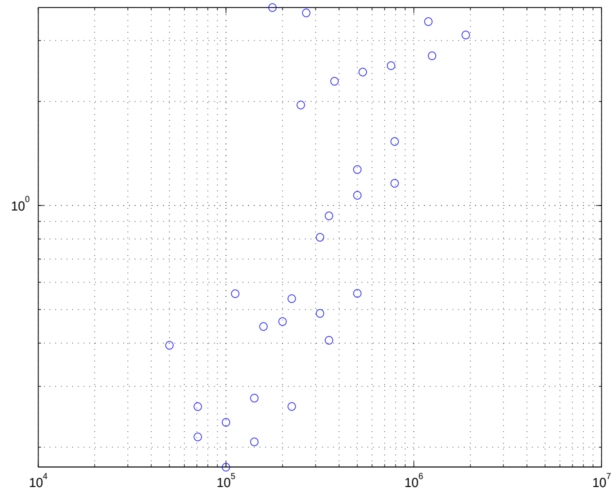
$\sigma(\Delta\gamma)$



$\sigma(\Delta V_{T0})$



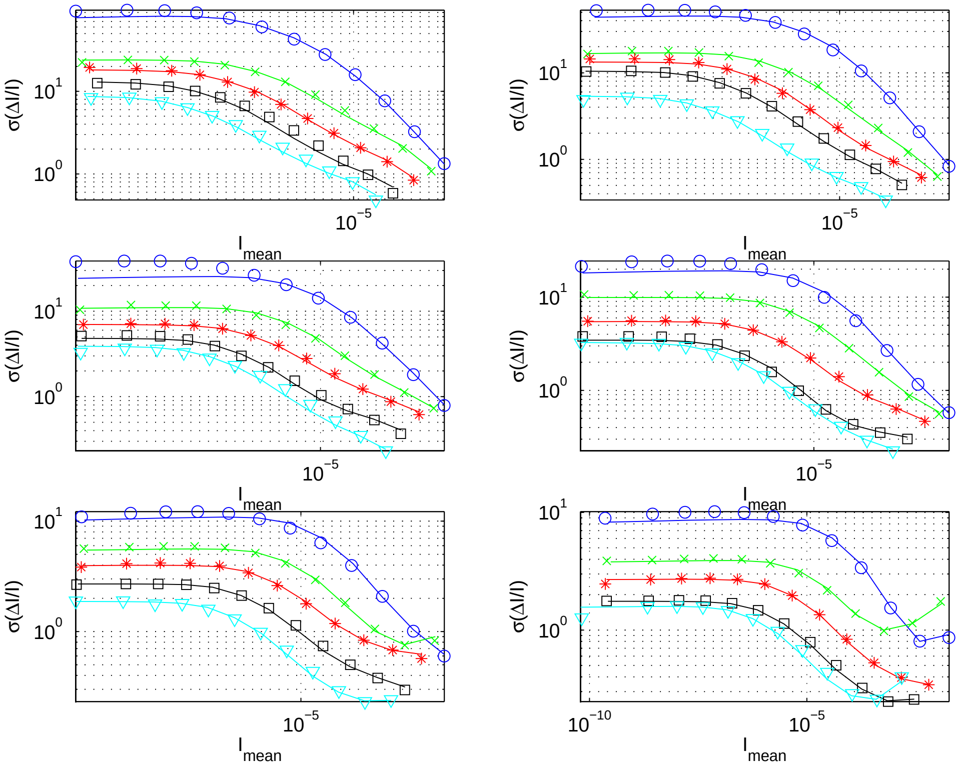
$\sigma(\Delta\theta_e)$

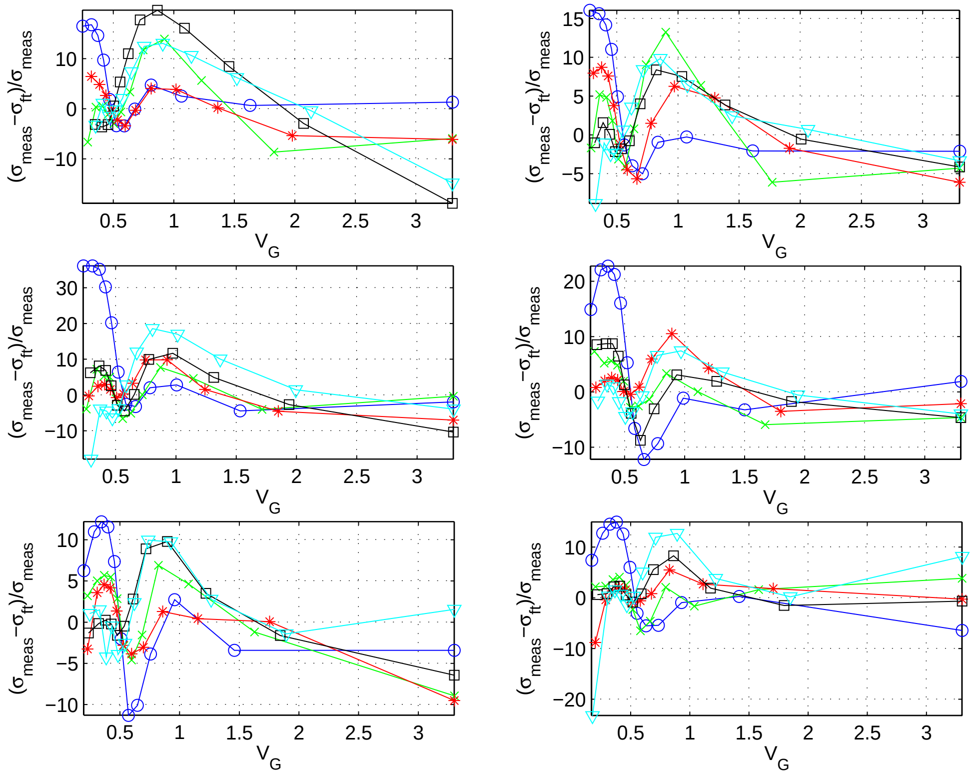


$\sigma(\Delta\theta_o)$

Predicting $\sigma(\Delta I/I)$ of measured curves and errors $(\sigma(\Delta I/I)_{meas} - \sigma(\Delta I/I)_{pred})/\sigma(\Delta I/I)_{meas}$

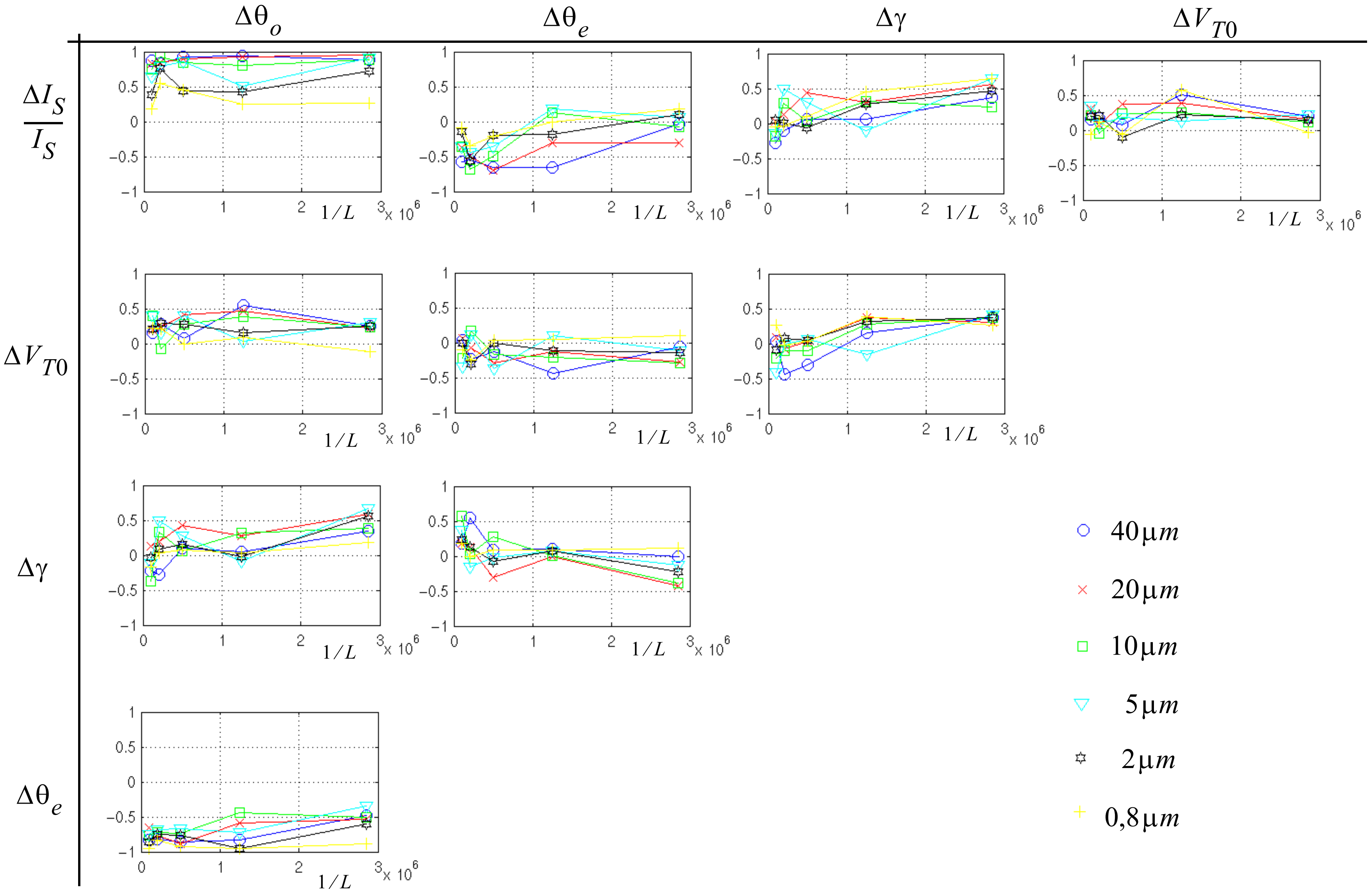
$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2_{I_S} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_{TO}}\right)^2 \sigma^2_{V_{T0}} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \gamma}\right)^2 \sigma^2_{\gamma} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta_o}\right)^2 \sigma^2_{\theta_o} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial \theta_e}\right)^2 \sigma^2_{\theta_e} + \text{correlation}$$





Curve 1. $V_{DS} = 1{,}65V \quad V_S = 0V$

Correlations



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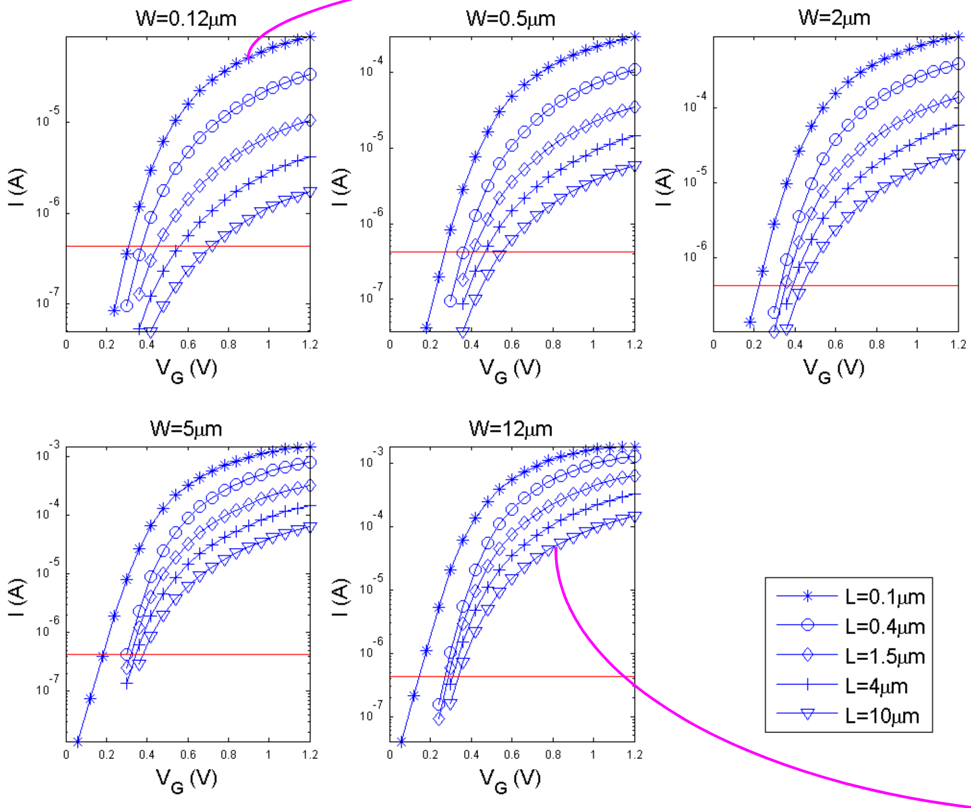
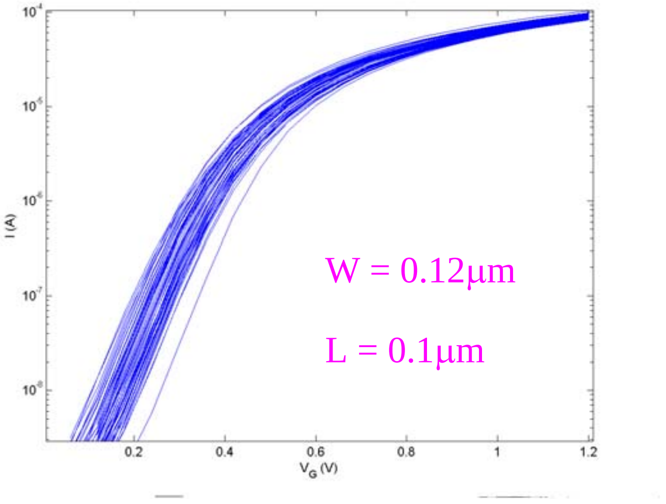
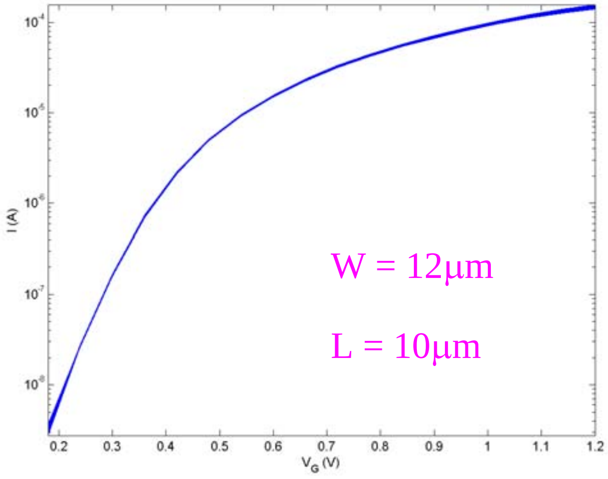
Mismatch Measurements

Nominal Measured Curves







CMOS Transistors

90nm process

25 different sizes

64 devices each size

Measured Curves with Mismatch

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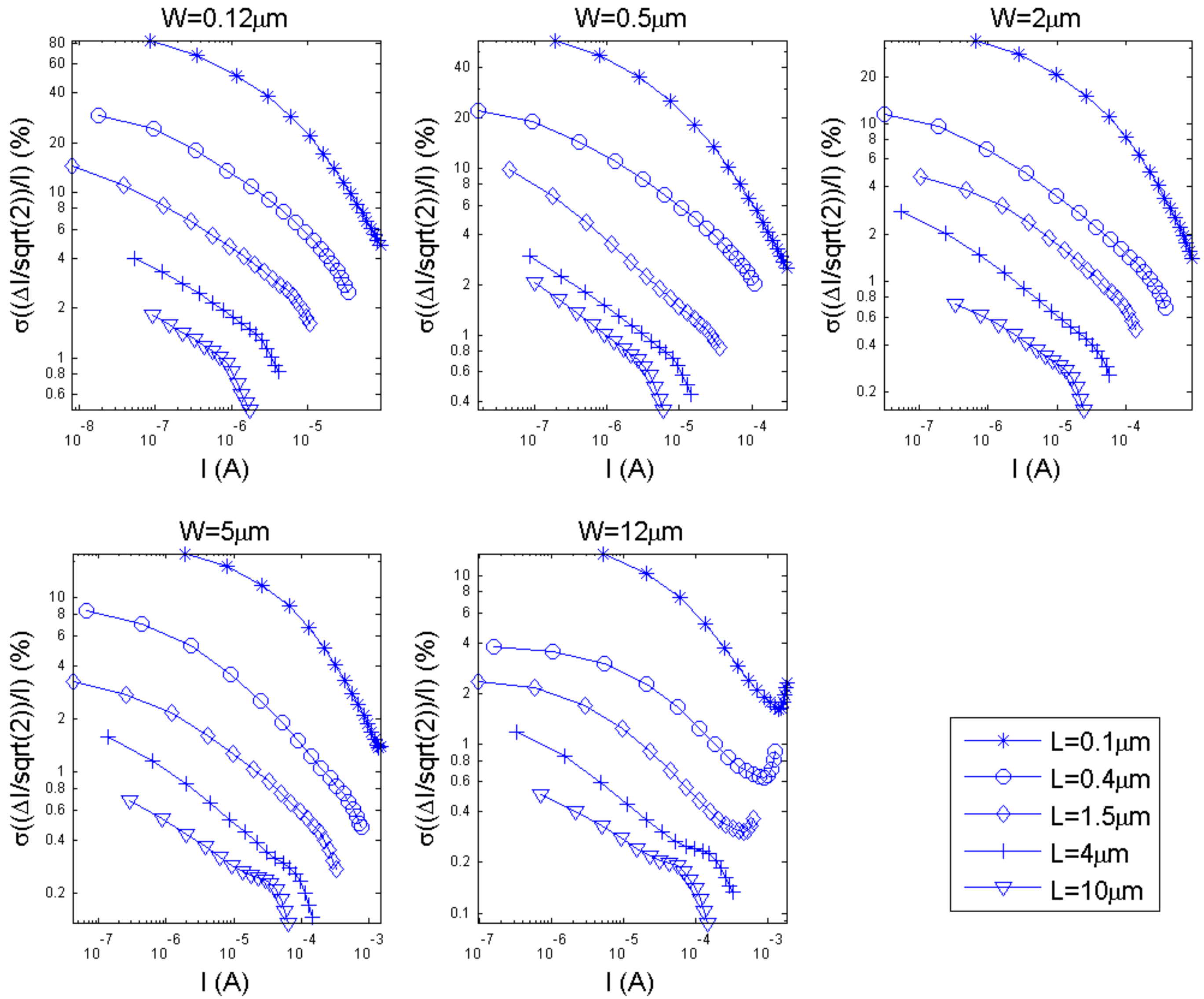
41092 Sevilla, SPAIN

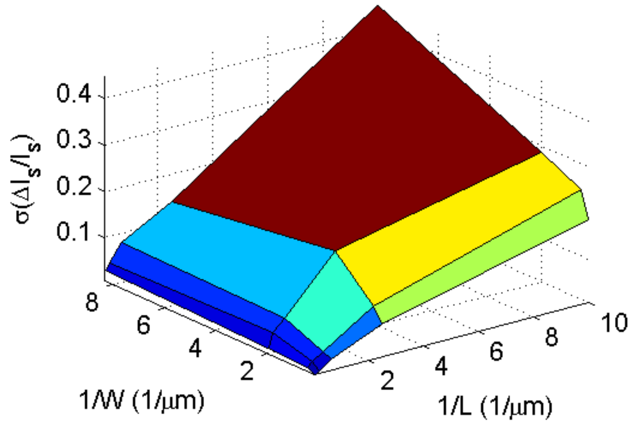
Phone: 34-95-4466666
Fax: 34-95-4466600
E-mail: terese@imse-cnm.csic.es

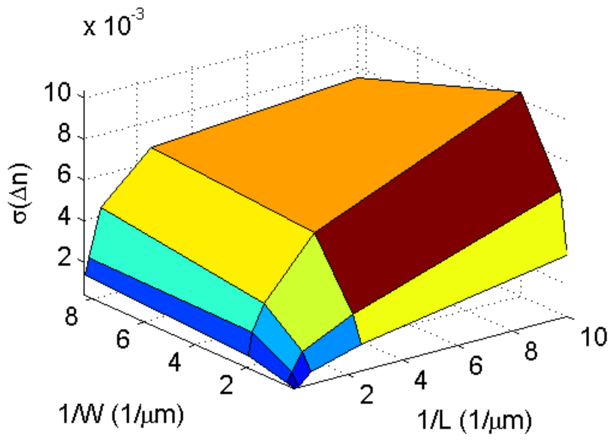
Mismatch Measurements

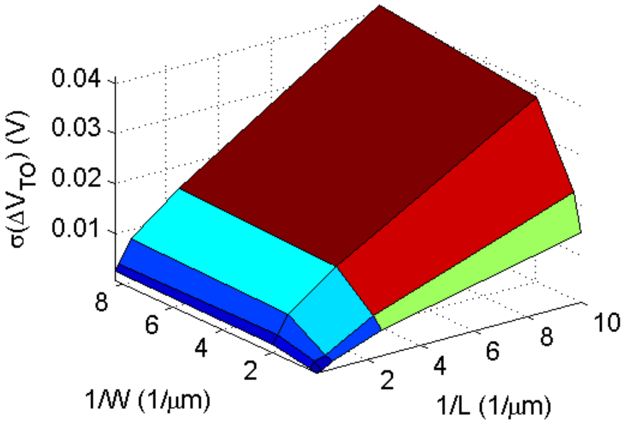


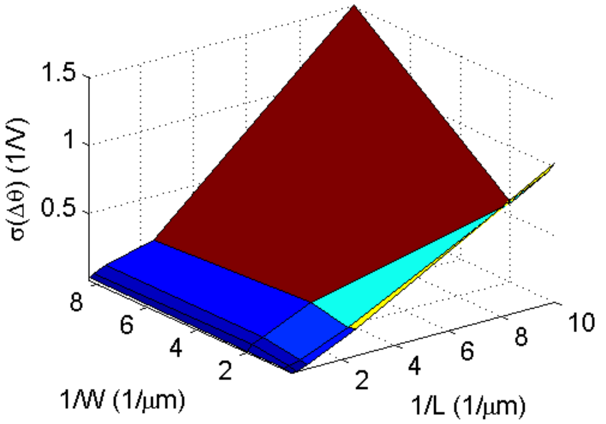
Extracted Mismatch Parameters

Standard NMOS transistors 90nm process



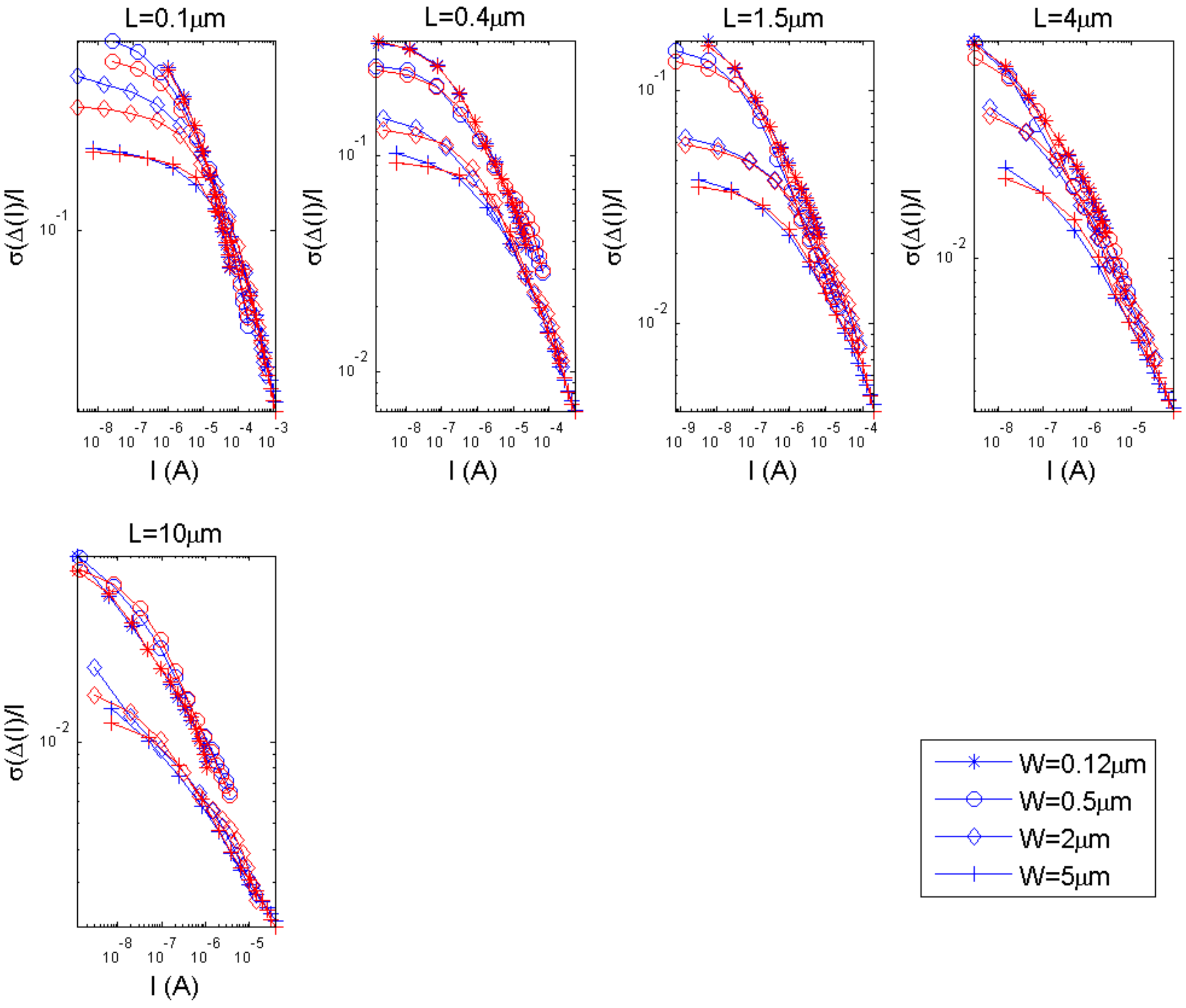






Measured vs. Predicted Current Mismatch

Standard NMOS transistors 90nm process

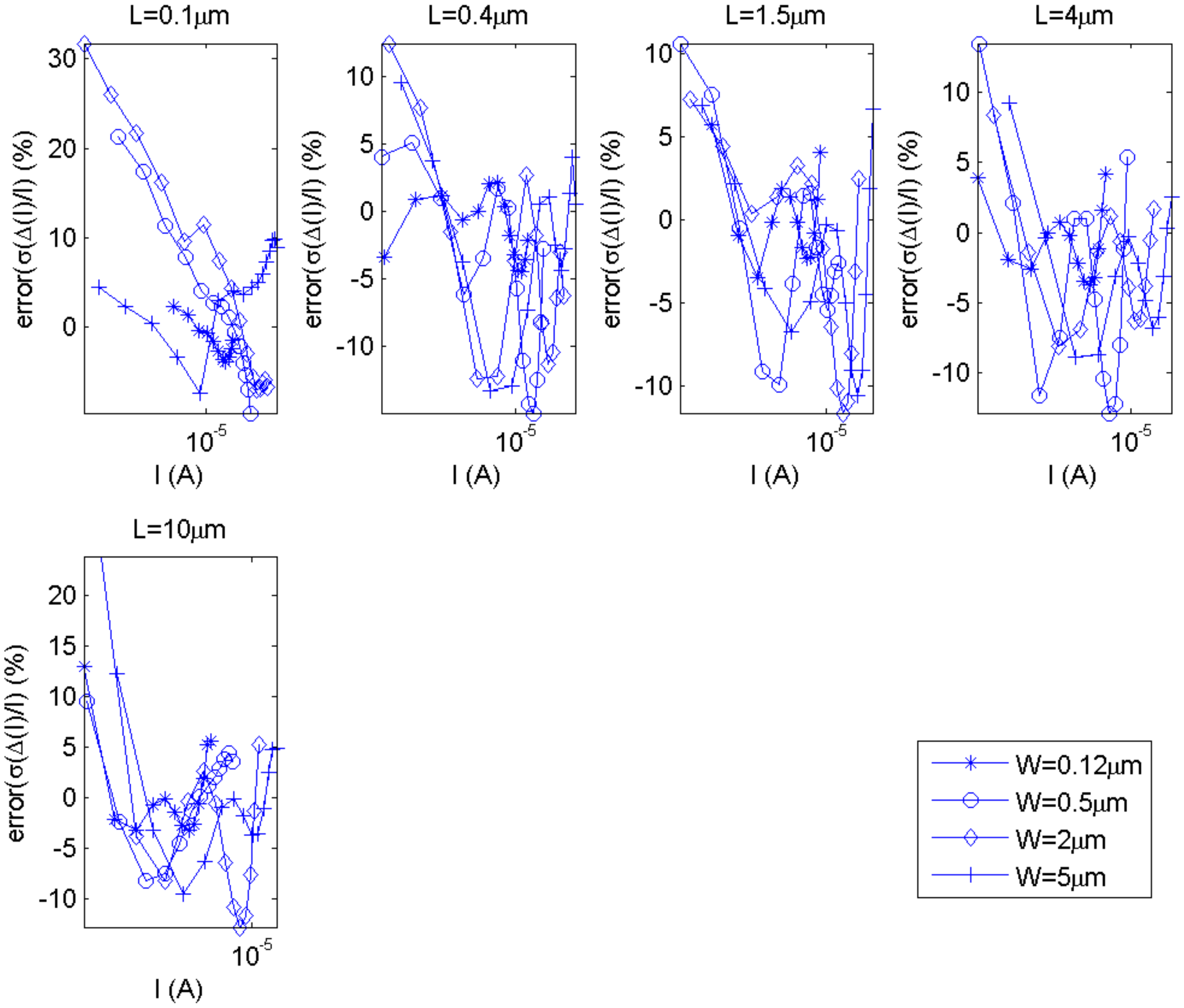


measured

predicted

Error in Current Mismatch Prediction

Standard NMOS transistors 90nm process



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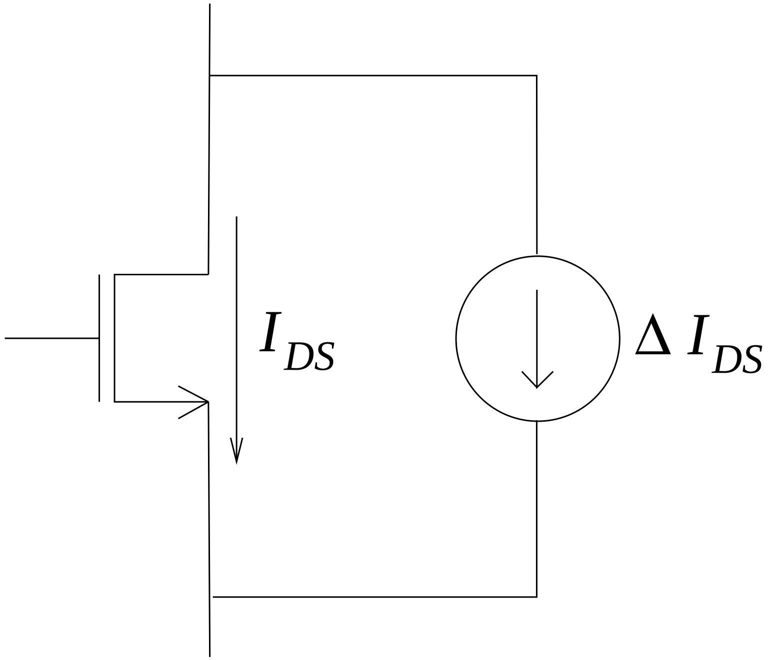
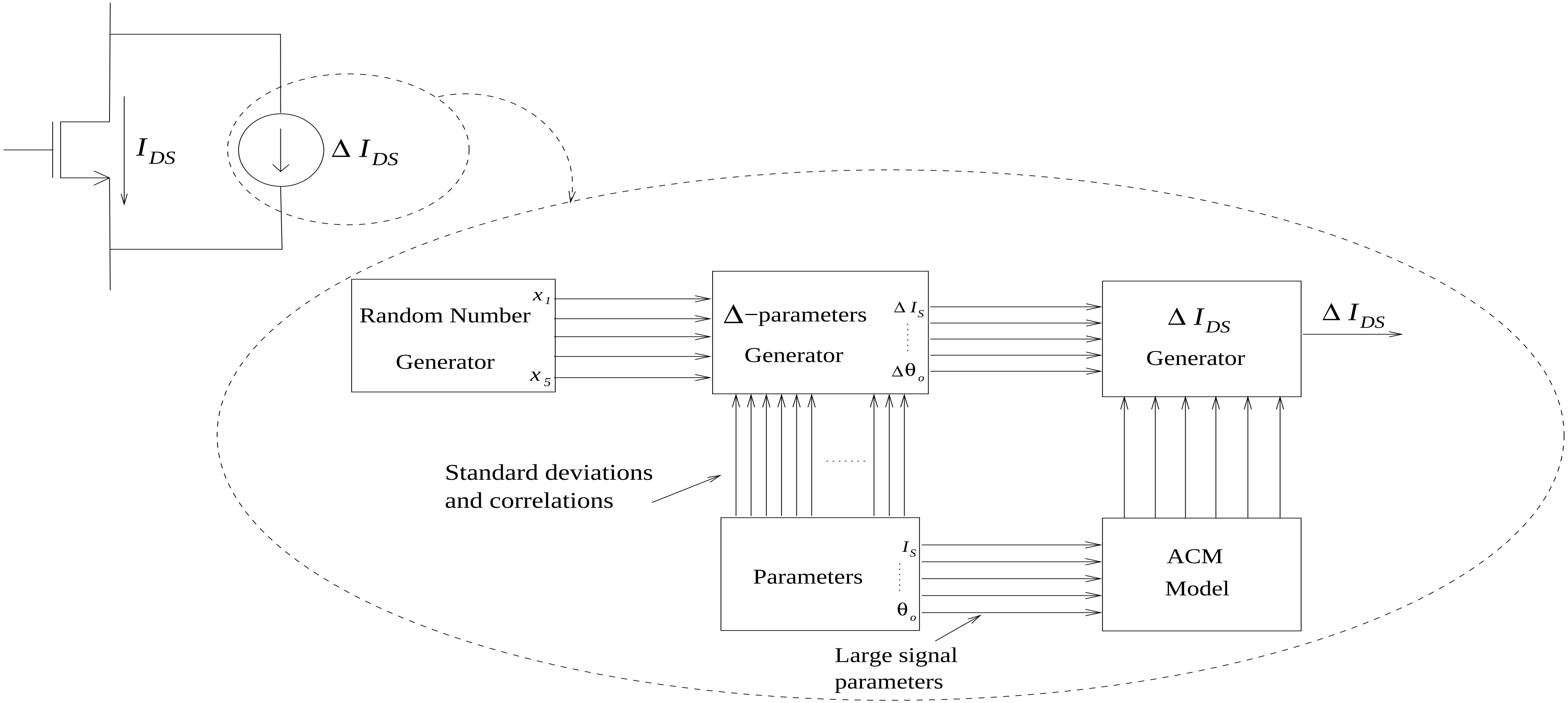
Spectre Mismatch Model Implementation

- Our intention is to create a model of a MOS transistor that fits with the results of the model.
- This model has been implemented in AHDL (Analog Hardware Description Language) and can be used in Simulator Spectre
- The model implementation is based on a current in parallel with a spectre library transistor that emulates the mismatch behavour.



Spectre Mismatch Model Implementation



I_{DS}

ΔI_{DS}

Random Number Generator

x_1

x_5

Δ−parameters Generator

ΔI_S

$\Delta\theta_o$

ΔI_{DS} Generator

ΔI_{DS}

Standard deviations and correlations

Parameters

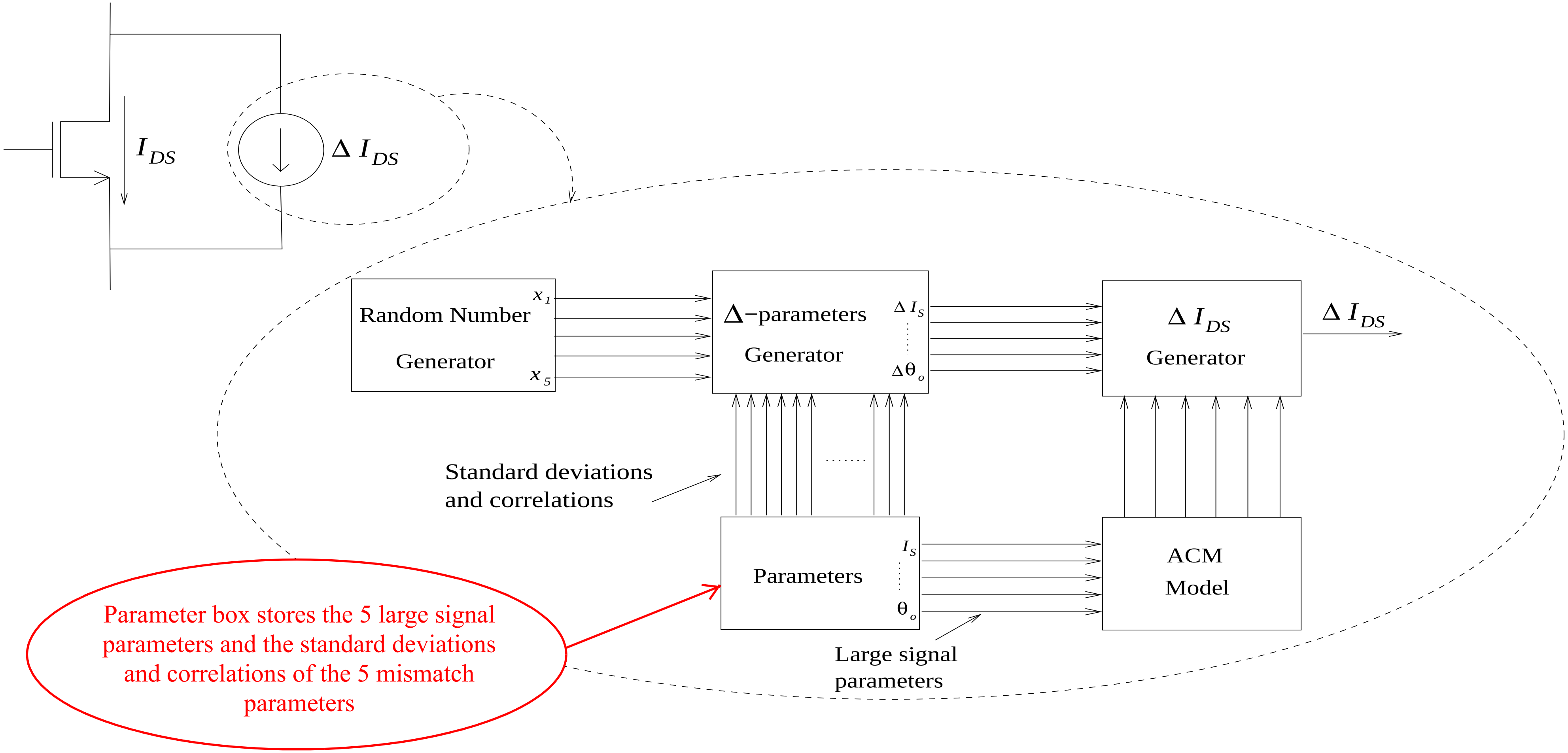
I_S

θ_o

ACM Model

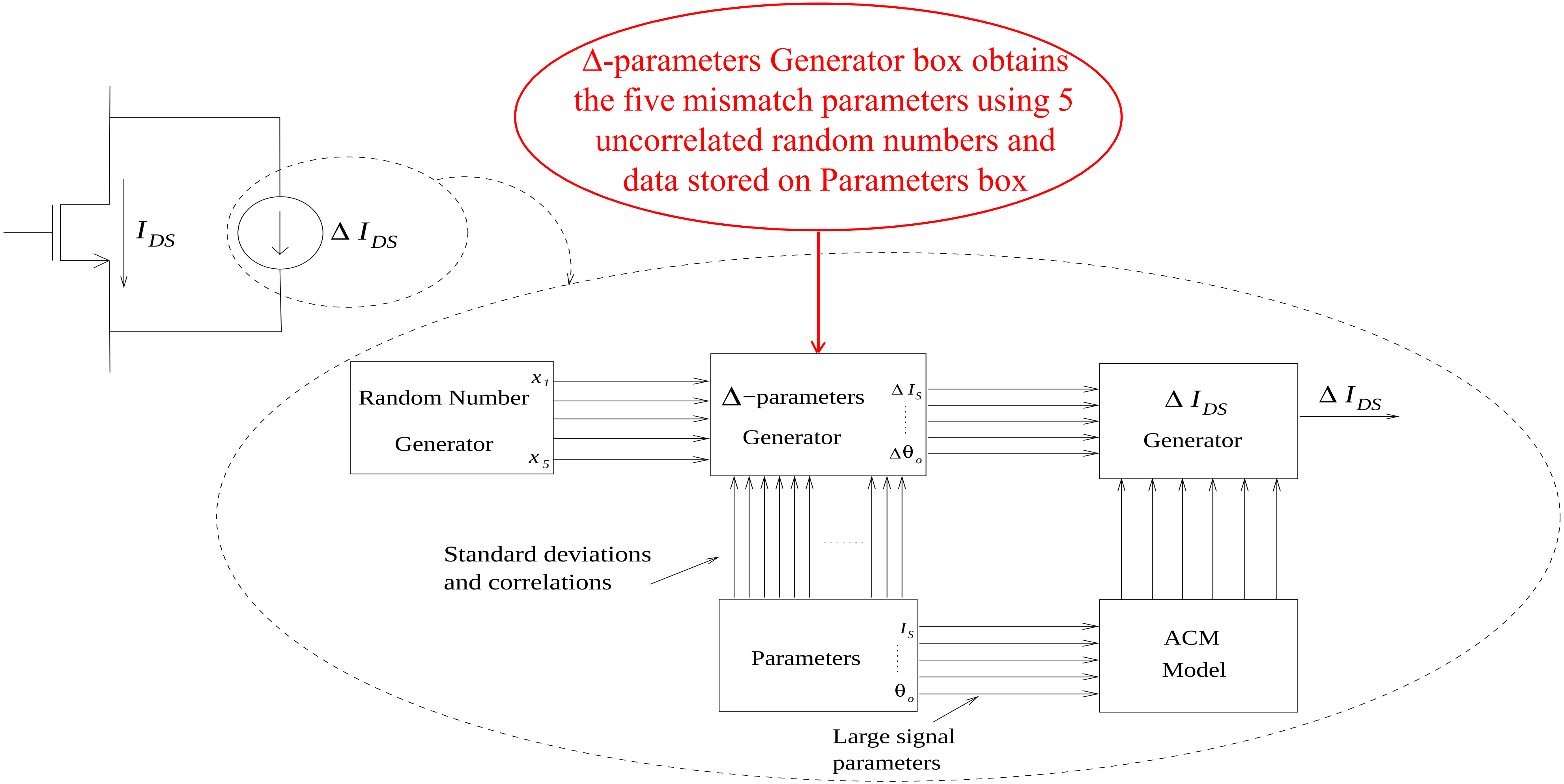
Large signal parameters

Spectre Mismatch Model Implementation



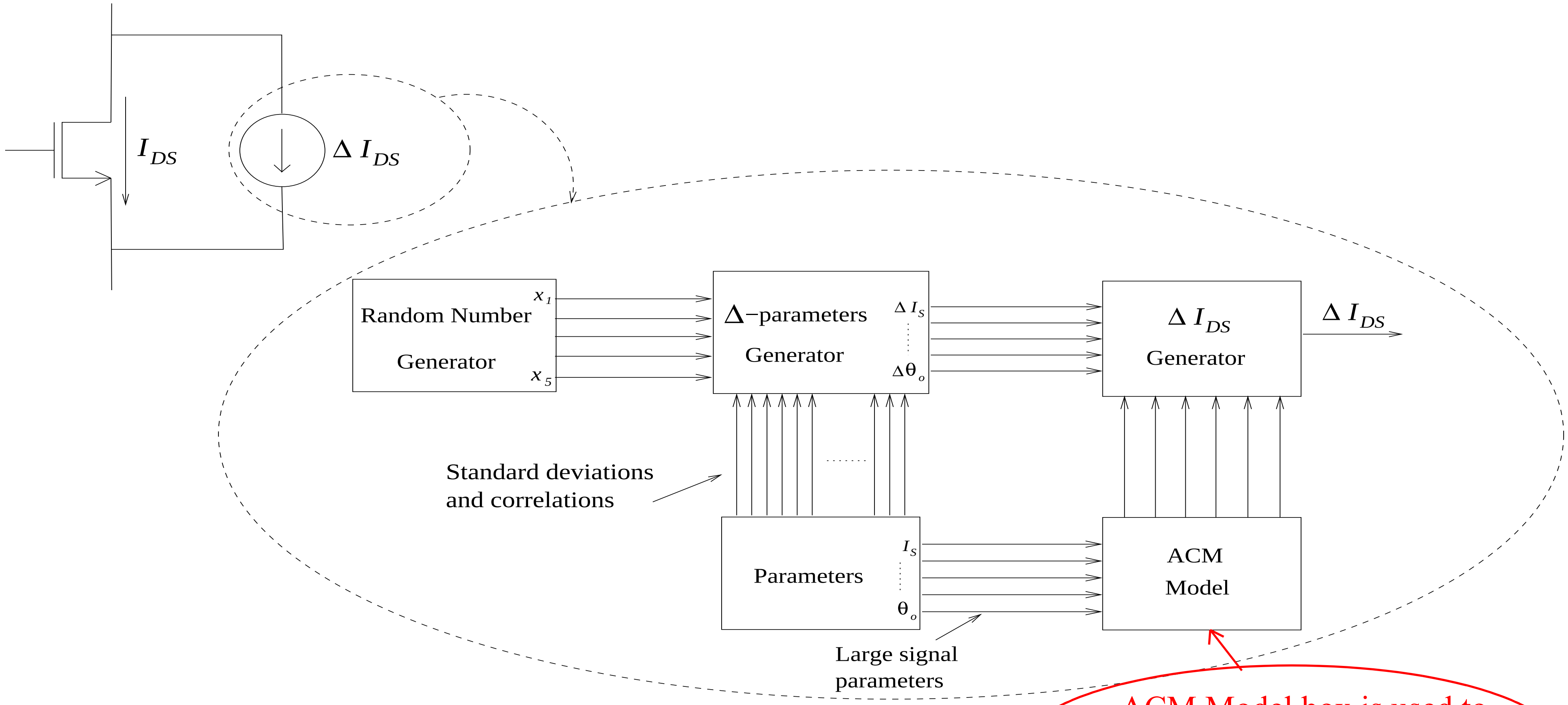
Parameter box stores the 5 large signal parameters and the standard deviations and correlations of the 5 mismatch parameters

Spectre Mismatch Model Implementation



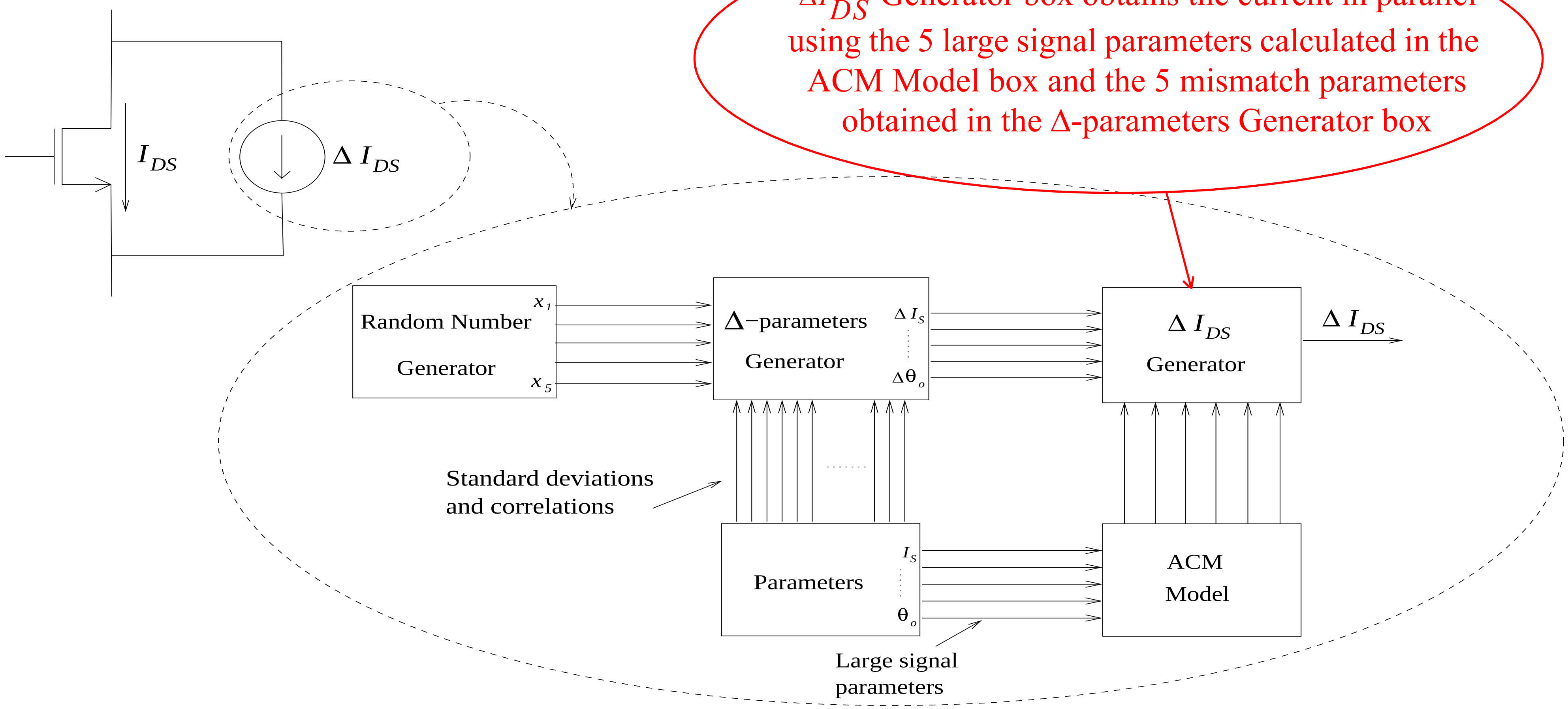
Δ-parameters Generator box obtains the five mismatch parameters using 5 uncorrelated random numbers and data stored on Parameters box

Spectre Mismatch Model Implementation



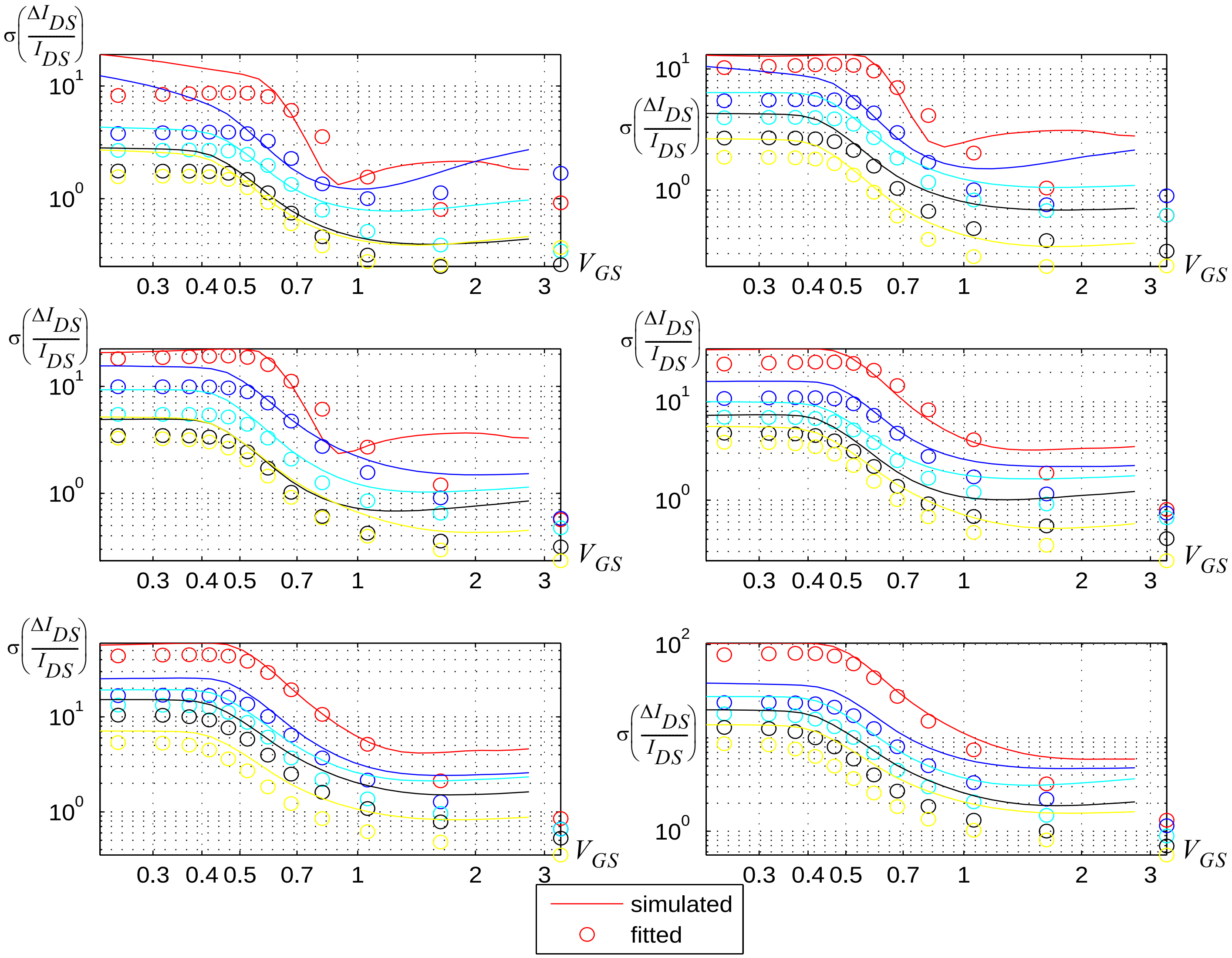
ACM Model box is used to obtain the large signal current using the 5 large signal

Spectre Mismatch Model Implementation



ΔI_{DS} Generator box obtains the current in parallel using the 5 large signal parameters calculated in the ACM Model box and the 5 mismatch parameters obtained in the Δ-parameters Generator box

Spectre Mismatch Model Implementation



Comparisson between simulated and fitted data for curve 1 and all transistor sizes

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Pelgrom JSSC-89

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2$$

size dependent term
distance independent

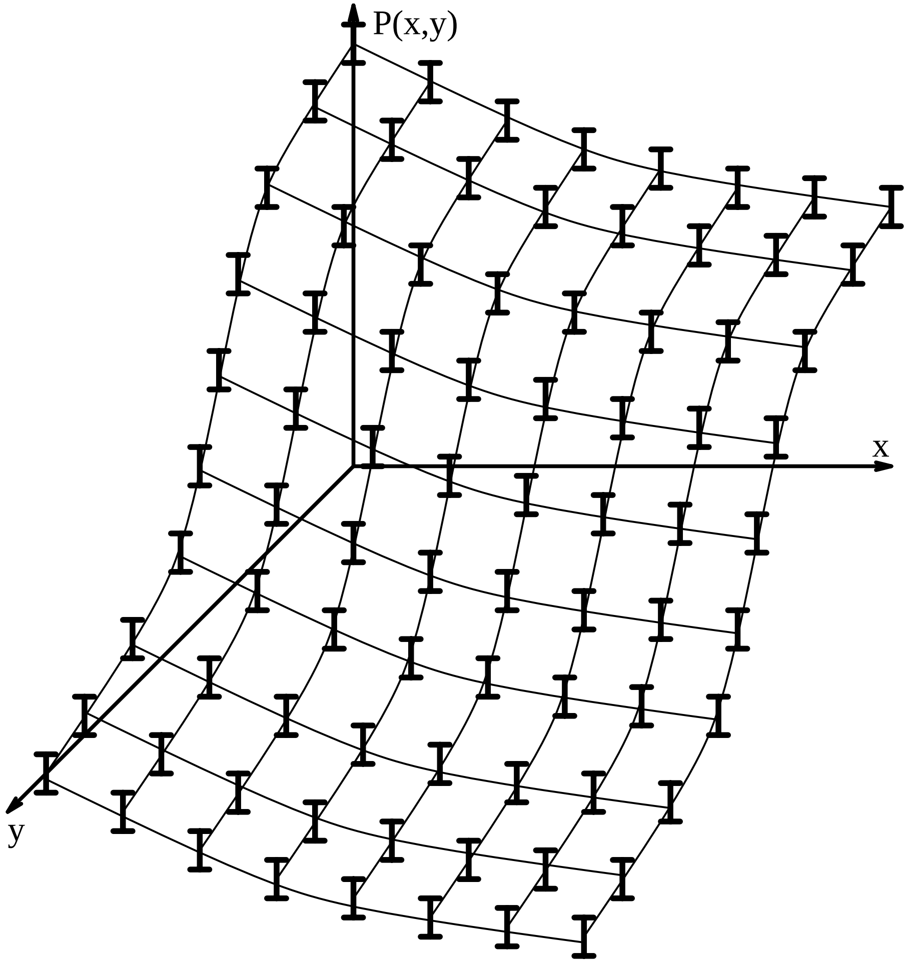
(lot of literature)

distance dependent term
size independent

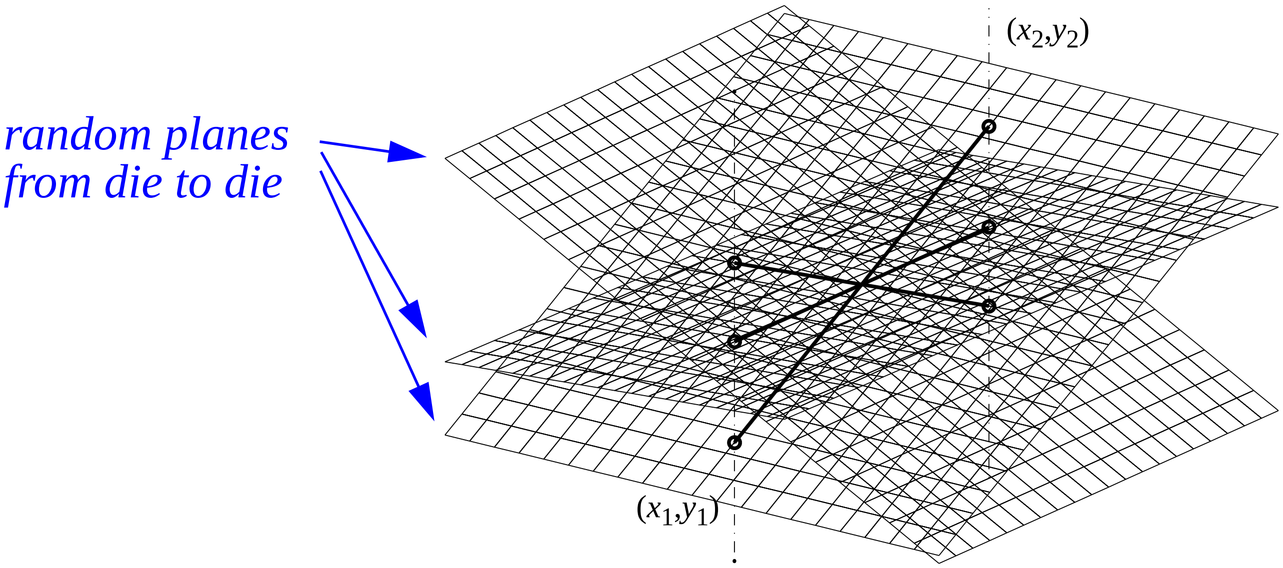
(little literature)

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2$$

By analyzing the mathematical derivation



Gradient Component



random planes
from die to die

$$P(x, y) = Ax + By + C$$

random numbers

die average

Generate random numbers A and B

$$P(x, y) = Ax + By + C$$

Generate random numbers A and B

$$P(x, y) = Ax + By + C$$

$$\downarrow$$

Gradient-induced mismatch

$$\Delta P_{grad\_ij} = A(x_i - x_j) + B(y_i - y_j)$$

Generate random numbers A and B

$$P(x, y) = Ax + By + C$$

Gradient-induced mismatch

$$\Delta P_{grad\_ij} = A(x_i - x_j) + B(y_i - y_j)$$

Statistics over many planes

$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)(x_i - x_j)^2 + \sigma^2(B)(y_i - y_j)^2$$

Generate random numbers A and B

$$P(x, y) = Ax + By + C$$

$$\downarrow$$

Gradient-induced mismatch

$$\Delta P_{grad\_ij} = A(x_i - x_j) + B(y_i - y_j)$$

$$\downarrow$$

Statistics over many planes

$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)(x_i - x_j)^2 + \sigma^2(B)(y_i - y_j)^2$$

$$\downarrow$$

no preferred directions: $\sigma(A) = \sigma(B)$

$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)[(x_i - x_j)^2 + (y_i - y_j)^2] = \sigma^2(A)D_{ij}^2$$

Generate random numbers A and B

$$P(x, y) = Ax + By + C$$

$$\downarrow$$

Gradient-induced mismatch

$$\Delta P_{grad\_ij} = A(x_i - x_j) + B(y_i - y_j)$$

$$\downarrow$$

Statistics over many planes

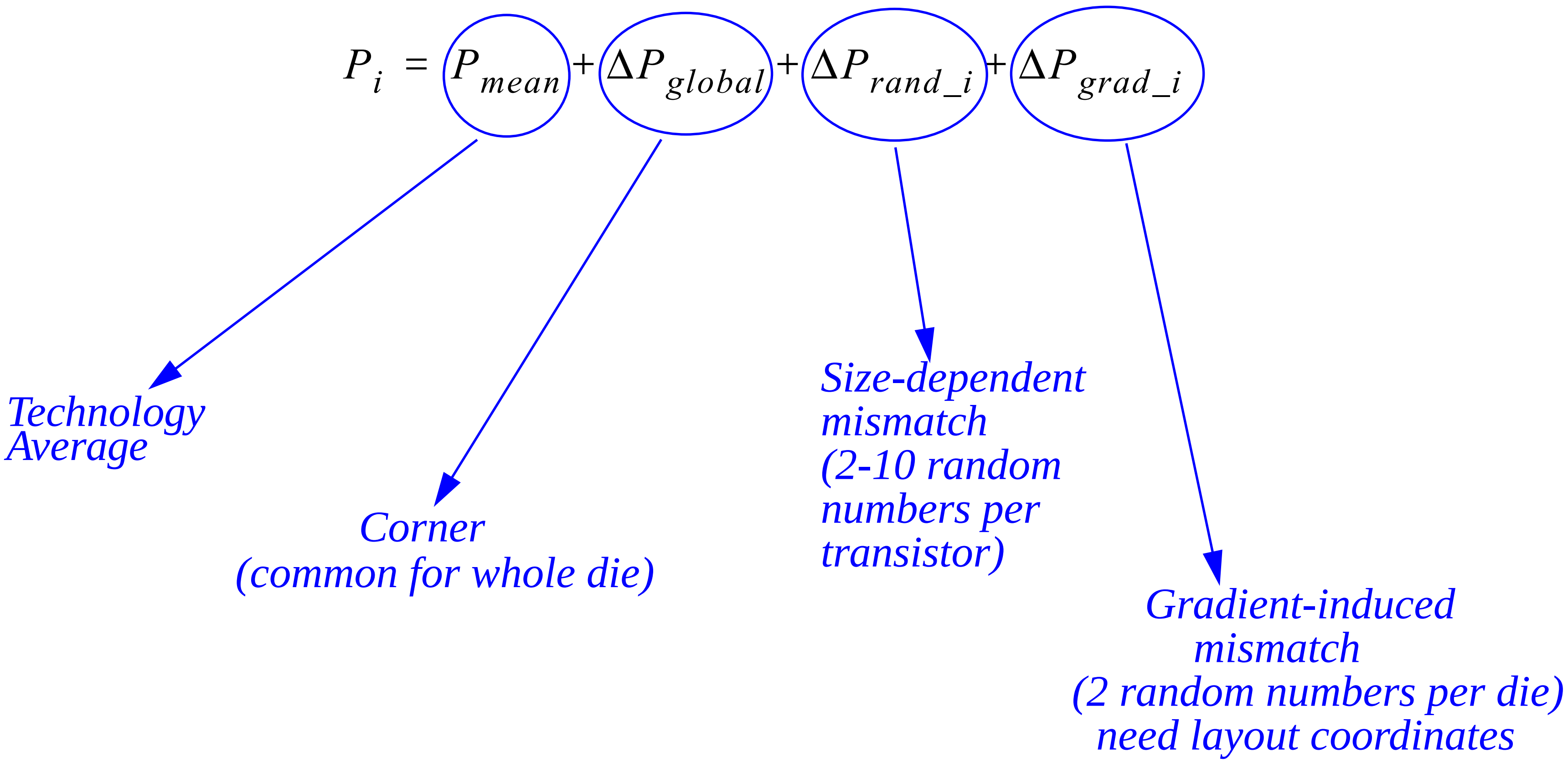
$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)(x_i - x_j)^2 + \sigma^2(B)(y_i - y_j)^2$$

$$\Big\downarrow \text{ no preferred directions: } \sigma(A) = \sigma(B)$$

$$\sigma^2(\Delta P_{grad\_ij}) = \sigma^2(A)[(x_i - x_j)^2 + (y_i - y_j)^2] = \boxed{\sigma^2(A)D_{ij}^2}$$

$$\sigma^2(\Delta P_{ij}) = \frac{A_P^2}{WL} + \boxed{S_P^2 D_{ij}^2} \longrightarrow S_P = \sigma(A) = \sigma(B)$$

Mismatch Modelling in a CAD Tool



$$P_i = P_{mean} + \Delta P_{global} + \Delta P_{rand\_i} + \Delta P_{grad\_i}$$

Technology Average

Corner
(common for whole die)

Size-dependent mismatch
(2-10 random numbers per transistor)

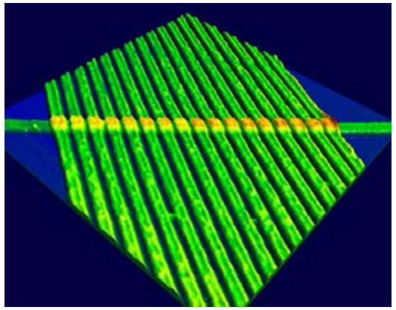
Gradient-induced mismatch
(2 random numbers per die)
need layout coordinates

Outline

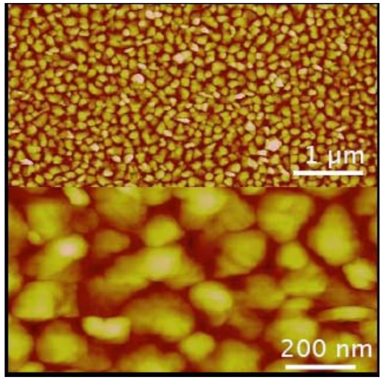
- Continuous Weak-to-Strong inversion models for mismatch
- Mismatch characterization chip
- Results for 0.35um CMOS
- Results for 90nm CMOS
- Simulating in Cadence-Spectre
- Modelling Pelgrom's Distance Term Efficiently
- Extension of continuous CMOS models to new coming nano-FETs

Motivations: Why?

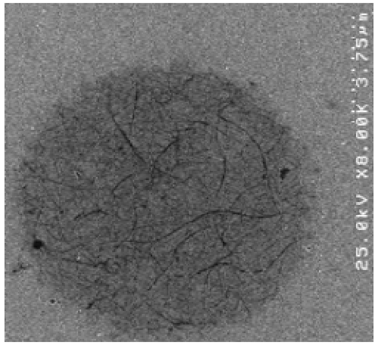
- New nano devices are rapidly appearing offering new functionality and memory capabilities



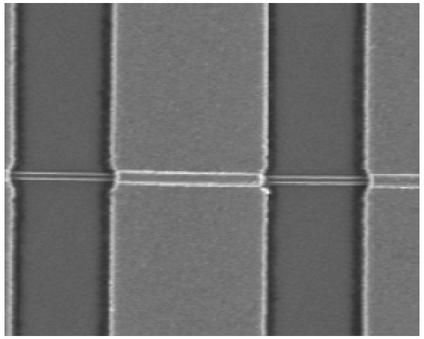
17 memristors in a row. The wires in this image are 50nm about 150 atoms, wide. J. J. Yang, HP Labs



NOMFET



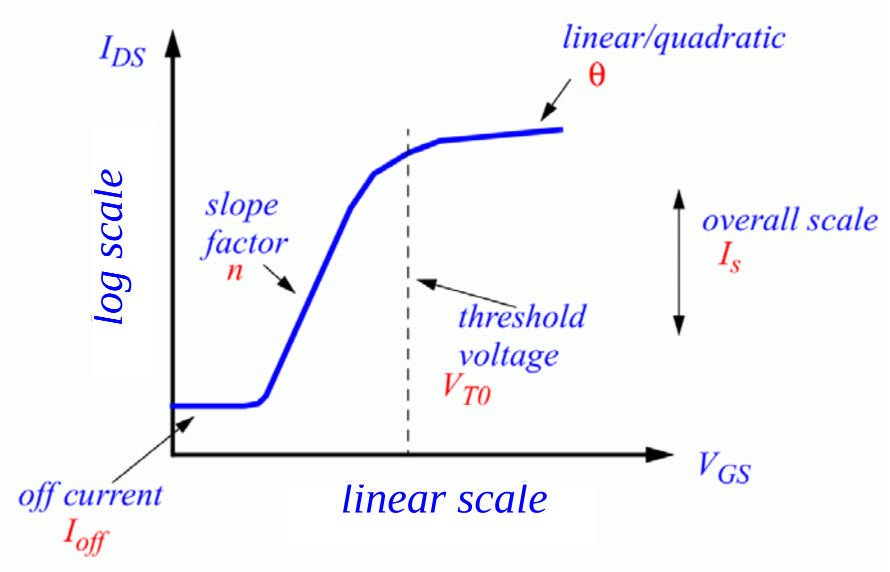
OG-CNFET

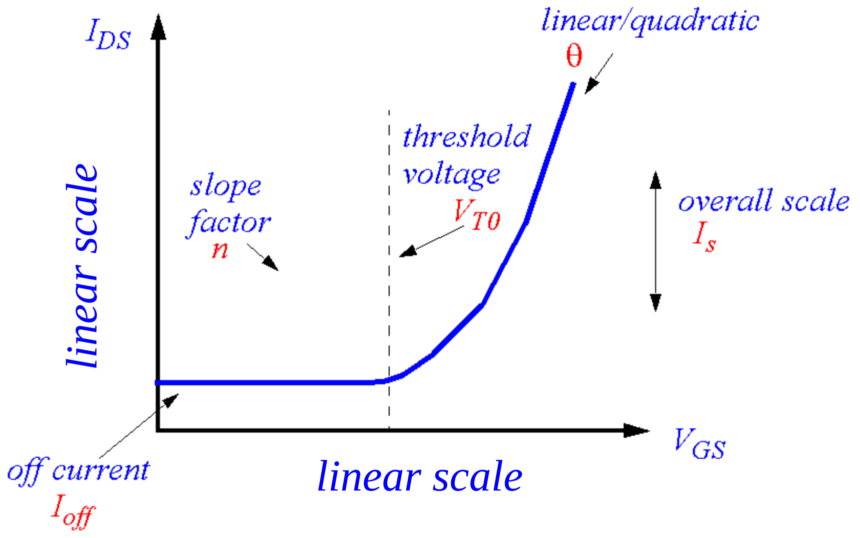


ZnO-MemoryFET

- Parallely, new circuits and architectures should be devised exploiting new capabilities
- Models are needed to simulate architectures and circuits
- Physical modelling is a slow, complex and sophisticated process
- Fitting new devices to a compact CMOS model has the advantage that circuit simulators are available allowing quick design and simulation of new architectures
- Hybrid nano-CMOS arquitectures can be easily simulated

EKV Compact Model [Enz et al. 1995]





I_{DS}	$\frac{I_F - I_R}{1 + \theta(V_P - min(V_D, V_S))} + I_{off}$
I_F	$I_s i_f(V_P, V_S)$
I_R	$I_s i_r(V_P, V_D)$
V_P	$\frac{V_G - V_{TO}}{n}$
$i_{f(r)}$	$\left[\ln\left(1 + \exp\left[\frac{V_P - V_{S(D)}}{2U_t}\right]\right)\right]^2$

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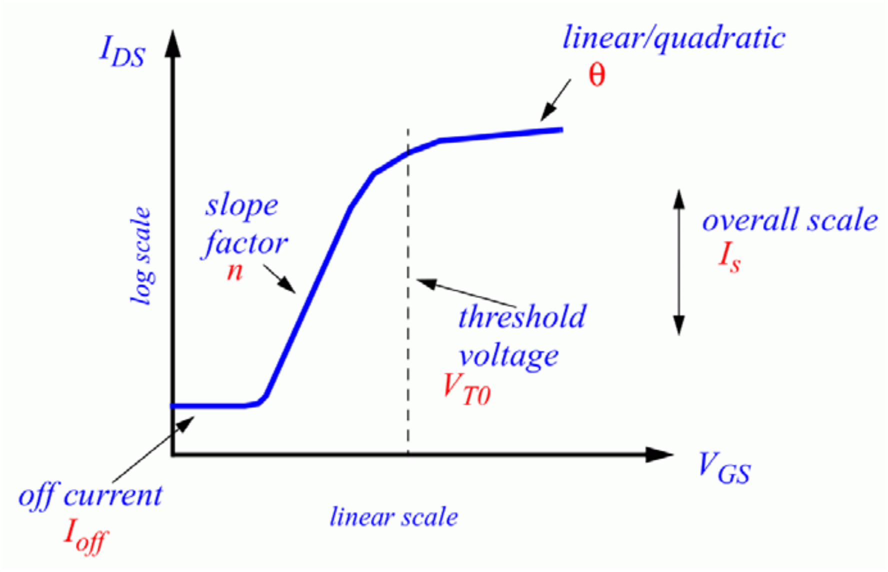
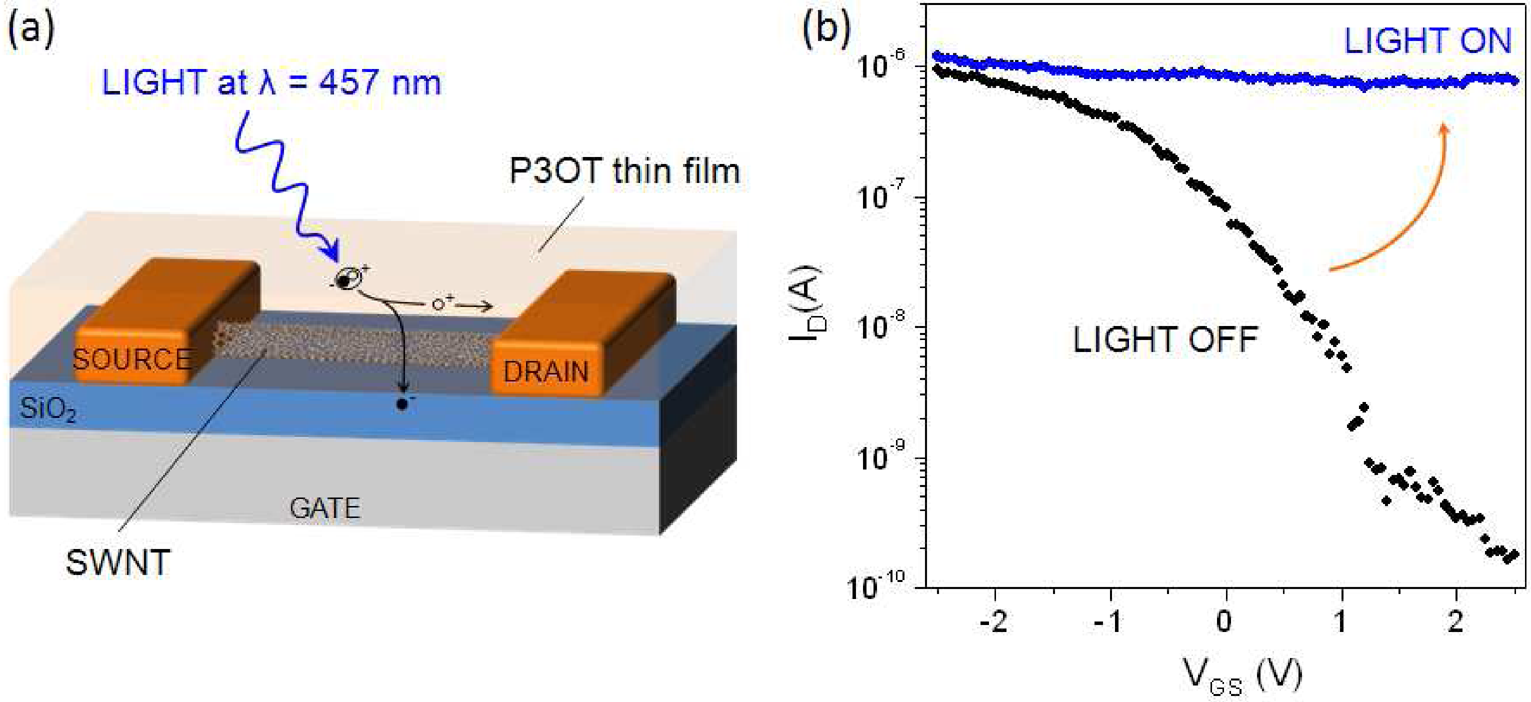
ACM Compact Model [Cunha et al., 1995]



I_{DS}	$\frac{I_F - I_R}{1 + \theta(V_P - min(V_D, V_S))} + I_{off}$
I_F	$I_s i_f(V_P, V_S)$
I_R	$I_s i_r(V_P, V_D)$
V_P	$\frac{V_G - V_{TO}}{n}$
$i_{f(r)}$	$q'^2_{is(d)} + 2q'_{is(d)}$
$V_P - V_{S(D)}$	$\phi_t((q'_{is(d)} - 1) + \ln q'_{is(d)})$

Other compact models could have been used [Iñiguez et al., 1995]

NABAB Nano Devices: OG-CNFET



- OG-CNFET: Optically Gated Carbon Nanotube FET
- P-type Carbon nanotubes single/network coated with photosensitive polymers act as memory devices
- Change in conductance four orders of magnitude upon illumination
- Response to light robust and reversible

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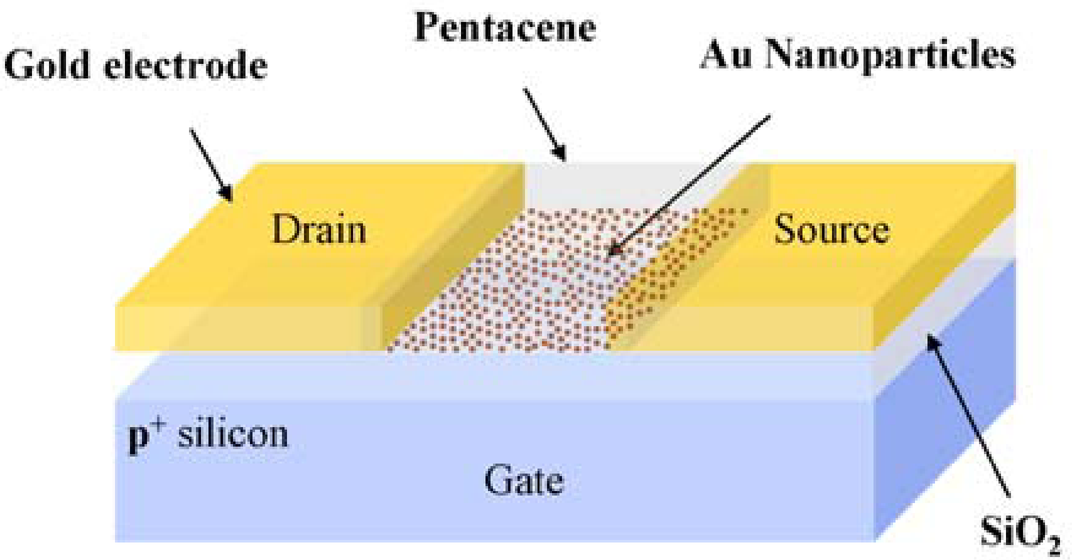
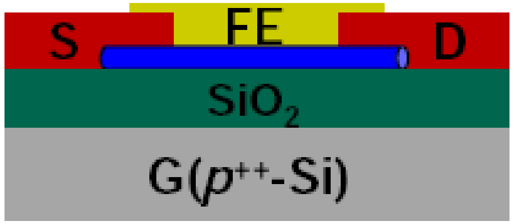
NABAB Nano Devices: NOMFET



- NOMFET: Nano Particle Organic Memory FET Transistor
- Three terminal device
- p^+ common gate/200nm $Si0_2$/gold source-drain electrodes/interelectrode gap 0.2-20µm
- Au nanoparticles deposed on the inter-electrode gap before pentacene deposition
- NPs are afterwards inmobilized using surface chemistry
- Pentacene (organic p-type semiconductor) deposited on top

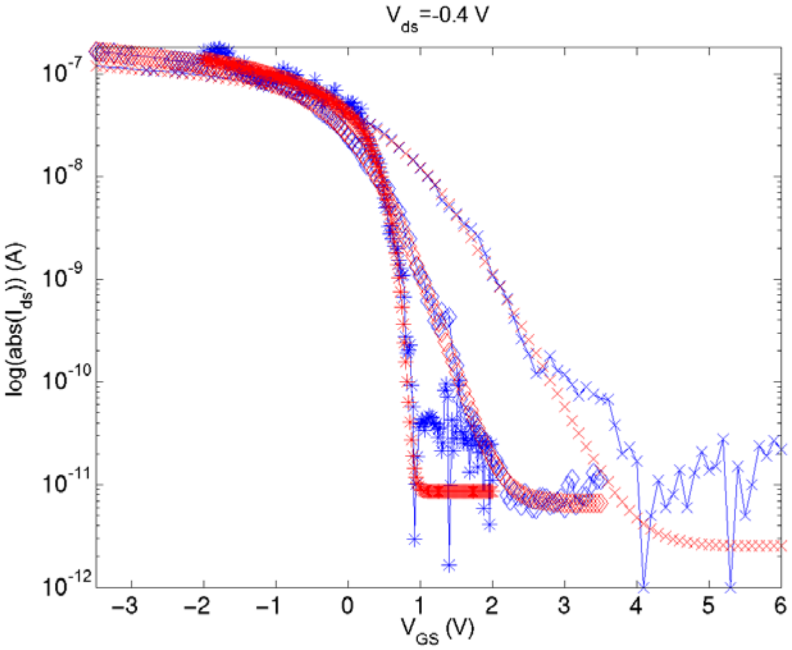
NABAB Nano Devices: ZnO NW memory FETs



- ZnO nanowires dispersed on a $Si0_2$-coated Si substrate

  100nm thick $Si0_2$
- Drain/source metal electrodes grown by photolitography
- Coated with layer of ferroelectric nanoparticles shifts threshold voltage positively or negatively depending on polarization
- Top gate made easy to change the orientation of polarization completely
- Long retention times
- Reversible

Fitting OG-CNFET to the EKV model. Experimental Results



Different type of channel

Different oxide thickness

Different size

* *Device L_g=200nm, t_{ox}=2nm, single tube:*

I_S=0.4nA n=1.22 V_{TO}=0.7895V θ=1.7530V^{-1} I_{off}=8.7pA

♦ *Device L_g=8000nm, t_{ox}=10nm, network of nanotubes:*

I_S=17.0nA n=7.78 V_{TO}=0.5396V θ=2.2085V^{-1} I_{off}=6.6pA

✕ *Device L_g=8000nm, t_{ox}=20nm, network of nanotubes:*

I_S=28.6nA n=11.82 V_{TO}=1.1904V θ=1.6013V^{-1} I_{off}=2.5pA

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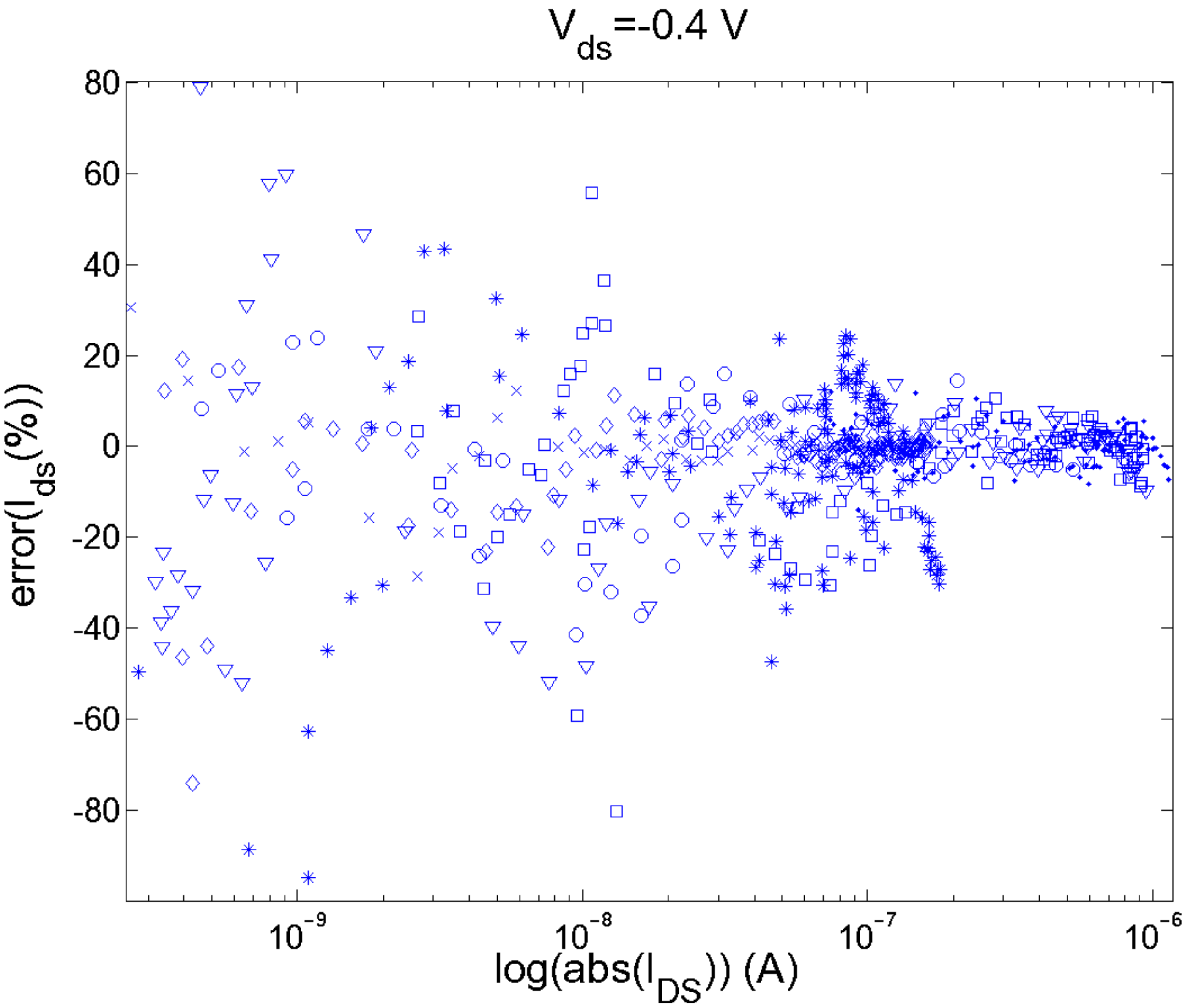
Fitting OG-CNFET to the EKV model. Experimental Results



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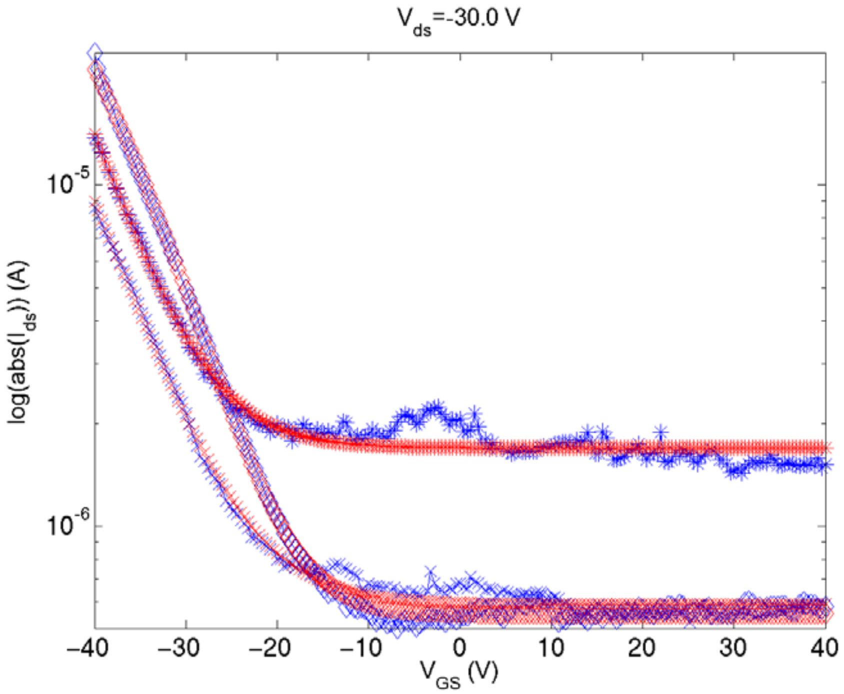
Fitting NOMFET to the EKV model. Experimental Results



Same device

Different programming conditions.

Writing

V_{GS}=-50V for 30 seconds

Erasing

V_{GS}=50V for 30 seconds

* *Device W=1000μm, L=1μm,* t_{ox}*=200nm, initial:*

$I_S=58.6\mu A$ $n=177$ $V_{TO}=-44.95V$ $\theta=0V^{-1}$ $I_{off}=1.7\mu A$

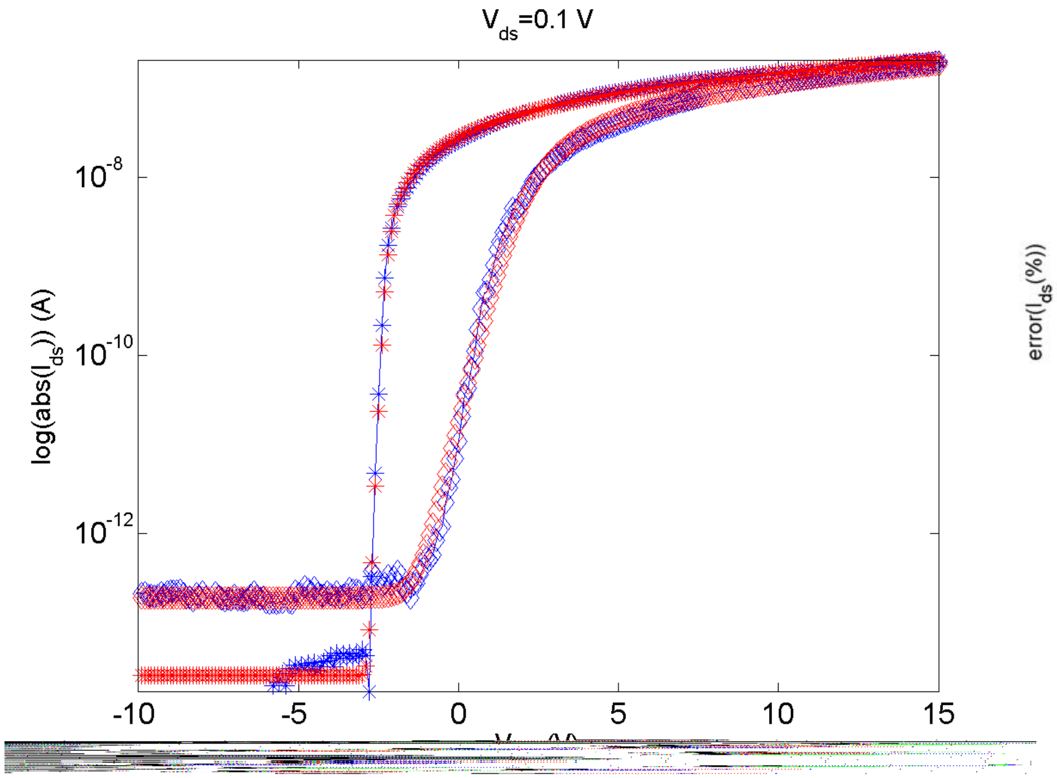
✕ *Device W=1000μm, L=1μm,* t_{ox}*=200nm, after writing:*

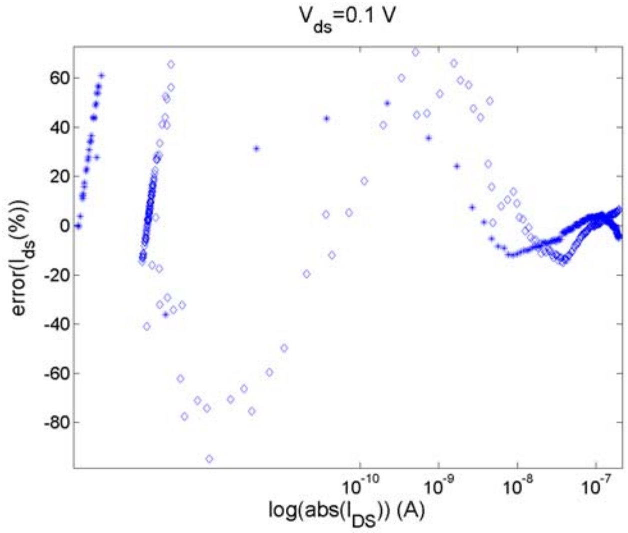
$I_S=65.4\mu A$ $n=199$ $V_{TO}=-48.74V$ $\theta=0V^{-1}$ $I_{off}=0.6\mu A$

♦ *Device W=1000μm, L=1μm,* t_{ox}*=200nm, after erasing:*

$I_S=6.7\mu A$ $n=140$ $V_{TO}=-28.44V$ $\theta=0V^{-1}$ $I_{off}=0.6\mu A$

Fitting ZnO Memory FET to the EKV Model. Experimental Results





✕ *Device bottom gated ZnO nanowire,* $L=3\mu m$, $t_{ox}=100nm$, V_{GS} *swept -10V to 15V:*

$I_S=0.5521nA$ $n=1.84$ $V_{TO}=-2.3675V$ $\theta=0.0006V^{-1}$ $I_{off}=0.0259pA$

♦ *Device bottom gated ZnO nanowire,* $L=3\mu m$, $t_{ox}=100nm$, V_{GS} *swept 15V to -10V:*

$I_S=6.7\mu A$ $n=10.88$ $V_{TO}=1.6554V$ $\theta=0V^{-1}$ $I_{off}=0.1926pA$

Conclusions

- We have shown how to extend in a compact manner the continuous EKV/ACM model to model mismatch including 2nd order effects relevant for mismatch.
- The model has been tested on 0.35um and 90nm CMOS technologies.
- We have indicated how one can simulate the model in a conventional circuit simulator.
- We have indicated how to include Pelgrom's Distance Term efficently in a CAD layout-aware mismatch simulator.
- We have shown the potential of the EKV/ACM continuous model to model some of new nano-FET devices.

References

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