Fourth-Order Cascade SC $\Sigma\Delta$ Modulators: A Comparative Study

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***Abstract*—Fourth-order cascade $\Sigma\Delta$ modulators are very well suited for IC implementation using analog sampled-data circuits because of their robust, stable operation and their capability to achieve high resolution and wide bandwidth with moderate power consumption. However, their optimum realization requires careful consideration of their performance degradations due to the hardware nonidealities. This paper presents a comparative study of the influence of finite op-amp gain and capacitor mismatch on the performance of fourth-order cascade $\Sigma\Delta$ modulators realized by means of switched-capacitor circuits. It considers single-bit and multibit quantizers and draws a number of comparative remarks validated by time-domain behavioral simulations.**

***Index Terms*— Analog–digital, conversion, sigma–delta modulators, switched capacitor circuits.**

I. Introduction

SIGMA–DELTA modulators $\Sigma\Delta$M use *oversampling* to reduce the in-band power of quantization noise, and filtering to *shape* this noise and push it out of the band. Assume the signal band is fixed. One strategy to increase the resolution of $\Sigma\Delta$M-based converters is to reduce the density of quantization noise in the signal band, which can be achieved by either increasing the sampling frequency, equivalently the oversampling ratio (M), or by increasing the number of levels (N) of the internal quantizer. The other strategy is to improve the filtering; i.e., the order (L) of the modulator. For practical integrated circuit (IC) design, these three degrees of freedom (M, N, and L) have to be explored under the constraints imposed by the required resolution, bandwidth and the available power budget. For signal bands up to the audio frequency range, it is common practice to use low-order modulators ($L = 1$ or 2) with 1-bit quantizers ($N = 1$) and large oversampling ratios ($M = 256$ and more); in particular, the well-known second-order structure [1]–[3]. However, achieving high resolution at frequencies in the video range and beyond requires high-order modulators and/or multibit quantizers to keep the oversampling ratio low, and hence to achieve optimal exploitation of the operation speed of the circuitry.

Practical considerations impose also the demand for robust stable operation, which has resulted in the use of *cascade* structures as the preferred alternative to implement high-order noise shaping functions [4], [5]. Since these structures are unconditionally stable [6], designers can focus their efforts on the optimization of the circuit performance. On the contrary, single-loop and interpolative high-order modulators need to address stability issues during the design phase [6]. Actually, most of the reported high-order single-bit and multibit $\Sigma\Delta$M IC's have cascade structure. Particularly, several switched-capacitor (SC) CMOS prototypes have been developed in different technologies to obtain: an effective resolution of 16 bit at 320 kHz Nyquist band with $N = 1, M = 64$, and $L = 3$ [7]; 15 bit at 200 kHz with $N = 1, M = 16$, and $L = 6$ [8]; 15 bit at 160 kHz with $N = 1, M = 32$, and $L = 4$ [9]; 12 bit at 2.1 MHz with $N = 3, M = 24$, and $L = 3$ [10], 12 bit at 2.2 MHz with $N = 3, M = 16$, and $L = 4$ [11], respectively.

A drawback of cascade $\Sigma\Delta$M's is their larger sensitivity to circuit imperfections as compared to single-loop modulators. For SC implementation, large op-amp gain must be used to attenuate the effect of integrator leakage [12]; also, good capacitor matching is required to avoid uncancelled low-order quantization noise. Although the first problem is partially solvable by using SC integrators insensitive to the finite gain of the op-amps [13], [8], the second problem presents still a major limitation—the capacitor mismatch is difficult to control due to its dependence on the technological parameters and the fabrication process. Thus, deep knowledge of the practical limitations of cascade SC $\Sigma\Delta$M's, the ways to overcome their drawbacks, and the trade-offs among alternative architectures, is fundamental for optimum circuit design. Unfortunately, this knowledge is not readily available in literature.

This paper focuses on the comparative analysis of two widely used fourth-order architectures: a two-stage fourth-order modulator, or 2-2 cascade [14], [15], and a three-stage fourth-order modulator, or 2-1-1 cascade [16]. These fourth-order architectures constitute a good practical compromise between performance and power consumption for medium- to high-frequency operation, which renders them worth considering in detail. On the other hand, other fourth-order cascade architectures whose first stage is a first-order modulator are not considered here due to their already demonstrated disadvantages [6]. The paper is organized as follows. Both architectures are analyzed first from an ideal point of view in Section II. Afterward, Section III considers nonideal behavior including the effect of the finite op-amp gain and capacitor mismatching. The benefits of combining these cascade architectures and multibit quantization are examined in Section IV. Finally, the results from the comparative study are discussed in Section V.

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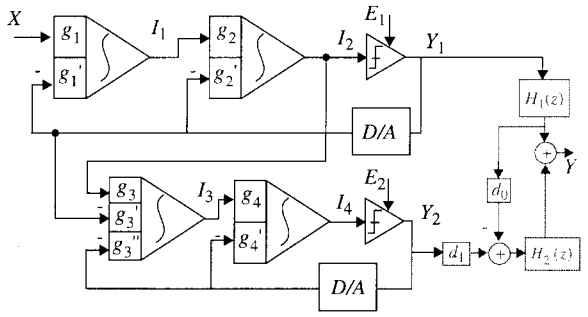

Fig. 1. Two-stage fourth-order cascade $\Sigma\Delta$ modulator (2-2).

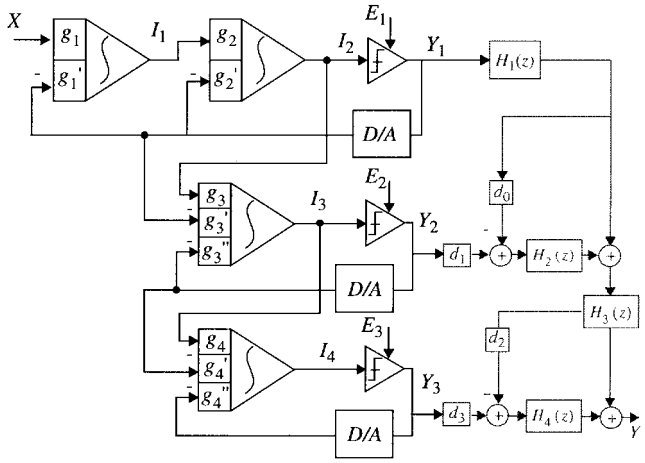

Fig. 2. Three-stage fourth-order cascade $\Sigma\Delta$ modulator (2-1-1).

II. Ideal Study

Figs. 1 and 2 show the architectures covered in this paper. Both operate according to the principles of cascade modulators: each stage in the cascade modulates the quantization noise of the previous; then, the quantization noise produced by all the stages but the last is digitally cancelled out [6]. Thus, the order of the noise shaping function is equal to the number of integrators in the chain. Although the need to conveniently scale the signals in the analog part yields a systematic loss of resolution, the use of unconditionally stable stages of order 1 and 2 renders cascade architectures very well suited for the practical implementation of high-order modulators up to video frequencies [7]–[11].

Fig. 1 realizes a fourth-order modulator by cascading two second-order stages (2-2), while Fig. 2 consists of a cascade of one second-stage and two first-order stages (2-1-1). These architectures are generalizations of those originally proposed in [14]–[16]. These works considered predetermined values of some integrator gains, for instance, $g_3 = 1$ and $g_3' = 0$ for the 2-2 in [15]. Here we assume that the integrator gains, g_i, are degrees of freedom. Then, the resolution limits of each topology may be reached through optimization of these coefficients and by taking into account constraints of the hardware implementation.

A. Digital Cancellation of the Quantization Noise

Let us focus first on the 2-2 modulator and assume that the quantization noise is additive, the modulator output after the cancellation logic can be expressed as

$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \tag{1}$$

where $X(z)$ and $Y(z)$ represent the input and output of the modulator, respectively; $E_1(z)$ and $E_2(z)$ are the respective quantization noises of the first and second quantizer; and $STF(z)$ and $NTF_i(z)$ $(i = 1,2)$ represent the transfer functions for the signal and the quantization noises. The following must be met to obtain the behavior of a fourth-order modulator:

$$|STF(z)| = 1 \quad NTF_1(z) = 0 \quad NTF_2(z) \sim (1 - z^{-1})^4. \tag{2}$$

That is, the input signal must be unaltered, the quantization noise in the first stage cancelled, and a shaping function of fourth-order must be provided for the quantization noise in the second stage. In the more general case, the exact expressions of these transfer functions, as well as the digital scaling coefficients d_0 to d_3, depend on the analog scaling coefficients and the transfer functions $H_i(z)$ of the digital filters that perform the noise cancellation. Considering the filters

$$H_1(z) = z^{-2} \quad H_2(z) = (1 - z^{-1})^2 \tag{3}$$

and imposing (2), yields the relationships among coefficients found in Table I. Thus, (1) becomes

$$Y|_{2-2}(z) = X(z)z^{-4} + d_1^2(1 - z^{-1})^4 E_2(z). \tag{4}$$

Similarly, for the 2-1-1 modulator of Fig. 2 using

$$\begin{aligned} H_1(z) &= z^{-1} \quad H_2(z) = (1 - z^{-1})^2 \\ H_3(z) &= z^{-1} \quad H_4(z) = (1 - z^{-1})^3 \end{aligned} \tag{5}$$

obtains the relations shown in Table II, and the following expression for the output:

$$Y|_{2-1-1}(z) = X(z)z^{-4} + d_3^2(1 - z^{-1})^4 E_3(z). \tag{6}$$

In principle, any combination of the integrator gains that meets the relations of Table I for the 2-2 architecture (alternatively, Table II for 2-1-1) and, hence, satisfies the conditions given by (2), leads to a *mathematically* correct modulator. However, to obtain a practical architecture, other constraints about the physical implementation must be imposed.

- The output range of the integrators, which depends on the input level and on the integrator gains, must be physically achievable for given supply voltage.

TABLE I
Relationships Between Analog and Digital Coefficients for the 2-2 Modulator

Digital/Analog	Analog
$d_0 = 1 - g_3'/(g_1 g_2 g_3)$	$g_1' = g_1$
$d_1 = g_3''/(g_1 g_2 g_3)$	$g_2' = 2g_1' g_2$
	$g_4' = 2g_3'' g_4$

TABLE II
RELATIONSHIPS BETWEEN ANALOG AND DIGITAL COEFFICIENTS FOR THE 2-2-1 MODULATOR

Digital/Analog	Analog
$d_0 = 1 - g_3'/(g_1g_2g_3)$	$g_1' = g_1$
$d_1 = g_3''/(g_1g_2g_3)$	$g_2' = 2g_1'g_2$
$d_2 = \left(1 - \frac{g_3'}{g_1g_2g_3}\right)\left(1 - \frac{g_4'}{g_3''g_4}\right) \equiv 0$	$g_4' = g_3''g_4$
$d_3 = g_4''/(g_1g_2g_3g_4)$	

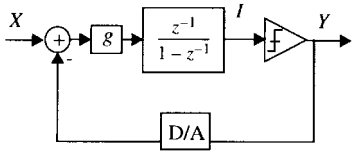

Fig. 3. First-order ΣΔ modulator.

- For each stage, the level of the signal transferred to the next one, which is a function of the integrator gains in the former, should not prematurely overload the latter.

Unfortunately, formulating both features as functions of the values of the integrator gains is not easy, and requires a detailed analysis of the time-domain operation of the low-order modulator stages, which shall be covered in the next section of the paper.

B. Time-Domain Behavior of Low-Order ΣΔ Modulators

Here we use a technique similar to that used in [17] to determine an upper bound for the integrator output signal of first- and second-order ΣΔM's driven by a dc input. Since the oversampling makes the input signal vary only slowly during the sampling period, this assumption does not constrain the validity of our results for ac input signals.

Let us first consider the first-order ΣΔM of Fig. 3. As shown in [1], by averaging the output sequence, one obtains the input, that is,

$$X = \frac{v_1 - v_{-1}}{v_1 + v_{-1}} \cdot V_r \tag{7}$$

where X is the input level of the modulator, V_r is the reference voltage (the output levels of the quantizer are $+V_r$ and $-V_r$), and v_1 and v_{-1} are the number of positive and negative pulses, respectively, observed at the modulator output in a sequence of length $v_1 + v_{-1}$. Equation (7) can be rewritten as

$$\frac{v_1}{v_{-1}} = \frac{V_r + X}{V_r - X}. \tag{8}$$

Thus, as expected, in a sequence of arbitrary length and for positive input, the number of positive pulses increases as the input level approaches the reference voltage. In fact, in a first-order ΣΔM, the number of consecutive positive pulses for inputs close to the reference levels is given by the integer larger than or equal to (8).

On the other hand, the finite-differences equation that governs the first-order modulator is

$$I_n = I_{n-1} + g(X - Y_{n-1}V_r) \tag{9}$$

which may be written as

$$\begin{aligned} I_n &= I_0 + \sum_{k=1}^{n} (I_k - I_{k-1}) = I_0 + g \sum_{k=1}^{n} (X - Y_{k-1}V_r) \\ &= I_0 + g\left(nX - V_r \sum_{k=0}^{n-1} Y_k\right). \end{aligned} \tag{10}$$

Let us suppose that the first pulse of a sequence of consecutive positive pulses is produced at $n = 0$. As stated, the last positive pulse of the sequence is produced for

$$n_l = \left\lfloor \frac{V_r + X}{V_r - X} \right\rfloor - 1 \tag{11}$$

where $\lfloor a \rfloor$ denotes the smaller integer larger than or equal to a. According to this, for $n = n_l + 1$ a negative pulse is obtained at the output, which implies that $I_{n_l+1} \leq 0$. Applying (10),

$$\begin{aligned} I_{n_l+1} &\cong I_0 - g(V_r - X)\,\frac{V_r + X}{V_r - X} \\ &= I_0 - g(V_r + X) \leq 0 \Rightarrow I_0 \leq g(V_r + X). \end{aligned} \tag{12}$$

Note that in previous calculations, the approximation $\lfloor a \rfloor \cong a$; for $a \gg 1$ was made, which, in our case, is more accurate the closer the input level is to the reference voltage. If the calculations are repeated assuming negative input, one reaches the conclusion

$$|I_0| \leq g(V_r + |X|). \tag{13}$$

Bearing in mind (10) and (13), one may state that for positive input levels near the reference voltage, the output signal of the integrator evolves following a sawtooth curve, where the minimum is slightly below zero and the maximum is $g(V_r + X)$. Alternatively, for negative input, the maximum will barely exceed zero while the minimum will be $-g(V_r - X)$. Thus, in the limit, as X tends toward V_r, the range of the integrator output swing (OS) will be

$$OS = \pm 2gV_r. \tag{14}$$

Consider now the second-order modulator of Fig. 4. Here, double integration implies greater difficulties to determine an equation similar to (13), mainly due to the fact that, even though (7) and (8) are still valid, the number of consecutive positive (or negative) pulses, even for input close to reference levels, does not coincide with the integer larger or equal to said expressions. In fact, for given input level, the output sequences contain subsequences of positive (or negative) pulses of varied length, in compliance with (7) and (8). In addition, the number of subsequences of different lengths strongly depends on the initial conditions of the integrators, as well as on the input level. Fig. 5 shows an example of this through time-domain behavioral simulation for an input of $0.725V_r$. Given this

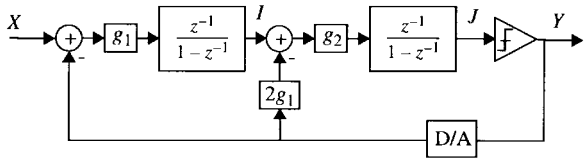

Fig. 4. Second order $\Sigma\Delta$ modulator.

difficulty, in what follows we use an iterative process of fast convergence to obtain the output ranges of the integrators.

Let us start with the discrete-time equations of the second-order $\Sigma\Delta$M

$$I_n = I_{n-1} + g_1(X - Y_{n-1}V_r)$$
$$J_n = J_{n-1} + g_2(I_{n-1} - 2g_1Y_{n-1}V_r) \tag{15}$$

which can also be written as

$$I_n = I_0 + \sum_{k=1}^{n}(I_k - I_{k-1}) = I_0 + g_1\left(nX - V_r\sum_{k=0}^{n-1}Y_k\right)$$
$$J_n = J_0 + \sum_{k=1}^{n}(J_k - J_{k-1})$$
$$= J_0 + g_2\left(\sum_{k=0}^{n-1}I_k - 2g_1V_r\sum_{k=0}^{n-1}Y_k\right). \tag{16}$$

From the first equality in (16),

$$\sum_{k=0}^{n-1}I_k = nI_0 + g_1\left(X\sum_{k=0}^{n-1}k - V_r\sum_{k=0}^{n-1}\sum_{l=0}^{k-1}Y_l\right)$$
$$= nI_0 + \frac{n(n-1)}{2}g_1X - g_1V_r\sum_{k=0}^{n-2}(n-k-1)Y_k$$
$$n \geq 2. \tag{17}$$

With that, the second equality in (16) is

$$J_n = J_0 + g_2nI_0 + g_1g_2\frac{n(n-1)}{2}X - 2g_1g_2V_rY_{n-1}$$
$$+ g_1g_2V_r\sum_{k=0}^{n-2}(n-k+1)Y_k. \tag{18}$$

Let X be a positive input close to the reference voltage. Starting from an arbitrary condition greater than zero at the output of both integrators, a sequence of consecutive positive pulses is generated until the output of the second integrator is less than or equal to zero, thus leading to a negative pulse. This will occur for the first value of n so that

$$J_0 + g_2nI_0 + g_1g_2\left(\frac{n(n-1)}{2}X - \frac{n(n+3)}{2}V_r\right) \leq 0 \tag{19}$$

condition which is obtained by making $Y_k = 1, k = 0, 1, \cdots, n-1$ in (18). Said value of n will be

$$n_0 = \lfloor r_0 \rfloor \tag{20}$$

where r_0 is the value (integer or not) for which the equality in (19) is met. The negative pulse generated at $n = n_0$ supposes increments in the output of both integrators that again become positive, thus starting another sequence of consecutive positive pulses. The duration of this sequence, which may differ from the previous one, obviously depends on the output values of the integrators at $n = n_0 + 1$ which play a role of new initial conditions in (18). In any case, these values are known

$$I_0 = I_{n_0} + g_1(X + V_r)$$
$$J_0 = J_{n_0} + g_2(I_{n_0} + 2g_1V_r). \tag{21}$$

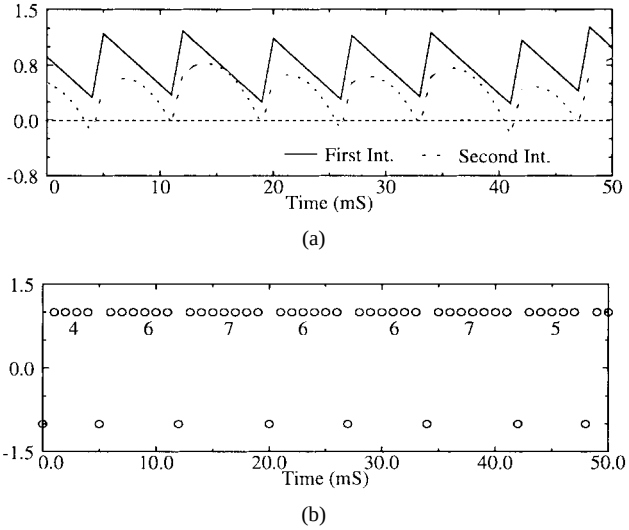

Fig. 5. (a) Output of both integrators and (b) sequences of consecutive positive pulses at the second-order modulator output.

Fig. 5(a) shows the evolution of the integrator outputs for $X = 0.725$ and $V_r = 1$. The corresponding output ranges are defined by the maximum of both curves which, as shown in the figure, coincide with the beginning $(n = 0)$ of a sequence of consecutive positive pulses for the first integrator and with an intermediate point in the corresponding sequence for the second integrator. In this last case, the maximum is reached when the derivative of (19) is nulled at

$$n_m = \frac{I_0}{g_1(V_r - X)} - \frac{3}{2}\frac{V_r + X}{V_r - X}. \tag{22}$$

Thus, the maximum output levels are given by

$$m_1 = I_0 = I_{n_0} + g_1(X + V_r)$$
$$m_2 = J_{n_m} = J_0 + g_2\frac{[g_1(3V_r + X) - 2I_0]^2}{8g_1(V_r - X)}. \tag{23}$$

The fact that the output levels of the integrators may be limited has not yet been considered. For a first-order modulator, if the output swing of the integrator is lower than the expression in (14), the modulator simply malfunctions (the average of the output does not equal the input). However, for the second-order modulator, for certain values of OS less than m_2 in (23), sequences of such a duration are produced that its maximum falls below said OS, maintaining correct operation of the modulator. This, which is clarified through the behavioral simulation of Fig. 6, is understood if one takes into account that, contrary to what occurs in first-order modulators, the sequence of consecutive positive (or negative) pulses in a second-order modulator is not unique for each input level.

We can now propose an iterative process to calculate the required output swing in the integrators given their gains and

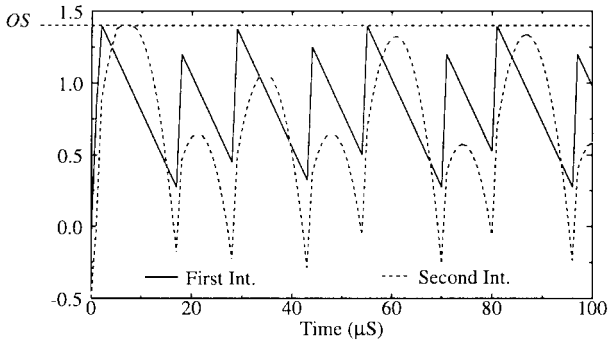

Fig. 6. Effect of the OS limitation on the integrator output.

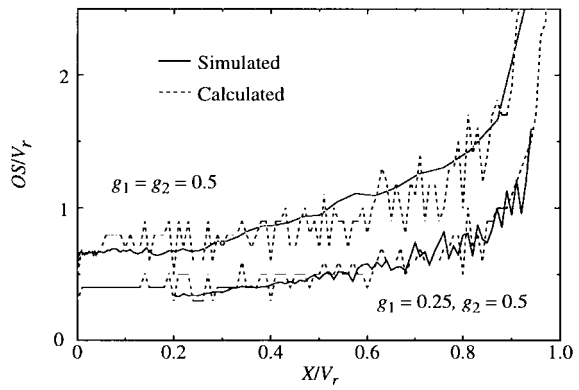

Fig. 7. Output range required in integrators.

input level. Said process, starting from an arbitrary OS value, will consecutively use (20)–(23), bearing in mind that the maximum output range is set. After checking that the new maximum reached (23) is larger than or equal to OS, the latter is increased and the process repeated until said maximum does not surpass OS.

Fig. 7 compares the results obtained by the algorithm to those obtained through behavioral simulation using dynamic input. A good fit is seen between both curves. Also, using the proposed procedure, the computation time is reduced at least 100 times. Note that for $g_1 = 0.25, g_2 = 0.5$, and X/V_r close to 0.9, OS must be slightly larger than V_r. However, for $g_1 = g_2 = 0.5$ OS must be, at least, equal to $2V_r$.

C. Optimization of the Coefficients

Optimization implies the determination of the analog scaling coefficients which, fulfilling the relationships of Tables I and II, lead to: 1) minimum quantization noise (this means that the digital coefficients in expressions (4) and (6) have to be as small as possible); 2) physically realizable output ranges of integrators; and 3) signal levels in the transition among stages that do not prematurely overload the next modulator. These levels are $\pm V_r$ for a first-order modulator and approximately $\pm 0.9V_r$ for a second-order modulator [18].

The optimization was performed using a statistical procedure [9], guided by the previous calculations,[1] to obtain the values in Table III, which result in the following digital

[1] Behavioral simulations show that the calculations of the upper bounds of the integrator outputs, which have been made assuming a DC or low-frequency input, remain valid for the second stage whose input contains the first stage quantization noise and therefore is not low-frequency.

TABLE III
OPTIMIZED ANALOG COEFFICIENTS

Coefficient	2-2	2-1-1
g_1	0.25	0.25
g_1'	0.25	0.25
g_2	0.5	0.5
g_2'	0.25	0.25
g_3	1	1
g_3'	0.375	0.375
g_3''	0.25	0.25
g_4	0.5	1
g_4'	0.25	0.25
g_4''	-	0.25

coefficients:

$$d_0 = -2 \quad d_1 = 2 \quad d_2 = 0 \quad d_3 = 2 \tag{24}$$

and the output range needed for the integrators is approximately equal to $\pm 1.2V_r$ for the 2-2 architecture and $\pm V_r$ for the 2-1-1.

Fig. 8(a) shows the SNR curves as a function of the input range referred to the reference voltage (0 dB $= V_r$) obtained through behavioral simulation with $M = 64$; similar results are obtained for other oversampling ratios (see Section V). Ideal elements, except the limited output ranges of integrators, were considered for simulation, and the gains of Table III were used. As shown in the figure, there are no important differences between the 2-2 and 2-1-1 topologies, except for input ranges close to the reference voltage; Fig. 8(b) shows this zone in detail. The difference is explained due to the fact that the second stage in the 2-2 topology is a second-order modulator whose maximum input level is approximately 10% lower than that of a first-order modulator, which coincides with V_r. Consequently, the overload of the 2-2 modulator is produced slightly before that of the 2-1-1 and, ideally, the SNR peak is higher by 5 dB in this latter case.

III. NONIDEAL EFFECTS

So far, modulators have been studied from an ideal point of view, with the exception of the limited OS of the integrators. This section covers a comparison of both architectures regarding their degree of sensitivity to the nonidealities of the electric implementation. These can be classified into two large categories.

- Nonidealities whose impact on modulator performance can be modeled as a source of noise at the first integrator input.[2] These include thermal noise, incomplete settling at the integrator output, nonlinear gain, etc. [9]. Since the extra noise power due to these phenomena depends on the integrators in the first stage, and both the 2-2 and the 2-1-1 have a second-order modulators at the first stage, there are no differences between them with regard to these

[2] The contributions of the remaining integrators in the chain to the total in-band noise is attenuated by the loop filtering.

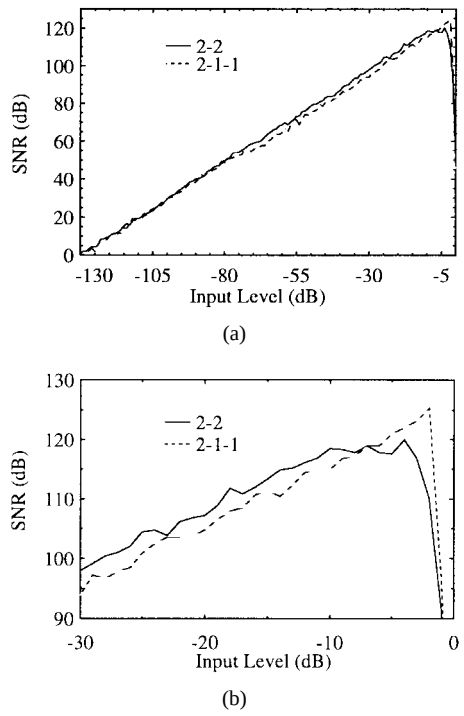

Fig. 8. (a) SNR as a function of the input level and (b) detail for large inputs.

nonidealities; consequently, their study is not necessary in this context.

- Nonidealities due to integrator leakage and mismatching between coefficients. These produce changes in the signal transfer function (STF) and the quantization noise transfer function (NTF) and, as shown later, introduce differences between the architectures studied.

A. Integrator Leakage

In the ideal analysis, the dc gain of the integrators of Figs. 1 and 2 has been assumed to be infinite—a feature which is impossible to achieve in practical realization due to circuit limitations. A consequence of the finite gain is that only a part of the signal at the integrator output node is added to the new input; that is, the transfer function in the Z-domain is,

$$H_I(z) = \frac{gz^{-1}}{1-(1-\mu)z^{-1}} \quad \mu = \frac{g}{A_{\rm dc}} \ll 1 \tag{25}$$

where $A_{\rm dc}$ represents the dc gain of the integrator (which coincides with that of the operational amplifier in an SC realization). Using (25) to hierarchically calculate the transfer functions of a first-order modulator (see Fig. 3) yields

$$\begin{aligned} STF(z,\mu) &= \frac{1}{1+\mu z^{-1}} \cong \frac{1}{1+\mu} \\ NTF(z,\mu) &= \frac{1-z^{-1}+\mu z^{-1}}{1+\mu z^{-1}}. \end{aligned} \tag{26}$$

Thus, the result is, first, an error in the modulator gain and, second, a change in NTF. This second result is much more explicit if we pass to the frequency domain

$$\begin{aligned} |NTF(f,\mu)|^2 &\cong \mu^2 + (1-\mu)|NTF(f,0)|^2 \\ &= \mu^2 + 4(1-\mu)\sin^2\left(\pi\,\frac{f}{f_S}\right) \end{aligned} \tag{27}$$

where f_S is the sampling frequency. The frequency-independent term in (27) is responsible for the increased power of quantization noise, which is calculated as

$$\begin{aligned} P_Q(\mu) &= \int_{-f_d/2}^{f_d/2} E(f)|NTF(f,\mu)|^2\,df \\ &\cong \frac{u^2}{12}\left(\frac{u^2}{M} + \frac{(1-\mu)\pi^2}{3M^3}\right) \end{aligned} \tag{28}$$

where it is assumed that the quantization noise presents a constant power spectral density equal to $u^2/(12f_S)$, where u is the separation between the levels of the comparator, $M = f_s/f_d \gg 1$; and f_d is the Nyquist frequency of the input signal.

Performing a similar analysis for the 2-2 and 2-1-1 modulators, after some simplifications, gives the following results for the quantization noise power:

$$\begin{aligned} P_{Q|2\text{-}2} &\cong \frac{u_1^2}{12}\left[\frac{4\pi^2\mu^2}{3M^3} + \frac{12\pi^6}{7M^7}\,d_0^2\mu^2\right] \\ &\quad + \frac{u_2^2}{12}\,d_1^2\left[\frac{4\pi^6\mu^2}{7M^7} + \frac{\pi^8}{9M^9}\,(1+2\mu)\right] \end{aligned} \tag{29}$$

$$\begin{aligned} P_{Q|2\text{-}1\text{-}1} &\cong \frac{u_1^2}{12}\left[\frac{4\pi^2\mu^2}{3M^3} + \frac{4\pi^6}{7M^7}\,d_0^2\mu^2\right] \\ &\quad + \frac{u_2^2}{12}\,d_1^2\,\frac{\pi^4\mu^2}{5M^5} \\ &\quad + \frac{u_3^2}{12}\,d_3^2\left[\frac{\pi^6\mu^2}{7M^7} + \frac{\pi^8}{9M^9}\,(1+2\mu)\right] \end{aligned} \tag{30}$$

which can be further simplified into

$$\begin{aligned} P_{Q|2\text{-}2} &\cong \frac{u^2}{12}\left[\frac{4\pi^2}{3M^3}\,\mu^2 + d_1^2\,\frac{\pi^8}{9M^9}\,(1+2\mu)\right] \\ P_{Q|2\text{-}1\text{-}1} &\cong \frac{u^2}{12}\left[\frac{4\pi^2}{3M^3}\,\mu^2 + d_1^2\,\frac{\pi^4\mu^2}{5M^5}\right. \\ &\qquad \left. + d_3^2\,\frac{\pi^8}{9M^9}\,(1+2\mu)\right] \end{aligned} \tag{31}$$

where we have assumed that the step between levels is identical for all the comparators ($u_1 = u_2 = u_3 \equiv u$) and that M is large enough—customary for $\Sigma\Delta$M IC design.

According to (31), the integrator leakage increases the quantization noise power as compared to the ideal case—calculated from (31) by making $\mu = 0$. This increase is caused by the incorrect cancellation of quantization noise in the first stages, and reflects in the onset of terms in M^{-3} and M^{-5}, besides the ideal one in M^{-9}. Among these error terms, the one in M^{-3} comes from the first-order filtering of the noise in the second-order modulator at the first stage. Generally, it can be shown that the output noise power of an Lth-order $\Sigma\Delta$M subjected to integrator leakage contains an error term in M^{-2L+1}. Thus, as indicated in (28), a first-order modulator causes the appearance of a noise term in M^{-1}, which is a consequence of the zero-order filtering. Since this term significantly degrades the modulator efficiency for given μ, those cascades starting with a first-order modulator (1-2-1, 1-1-1-1, and 1-1-2) are of little practical interest—which is why they are not covered here.

Equation (31) shows that the effect of the integrator leakage is larger in the 2-1-1 topology than in the 2-2. The onset of the

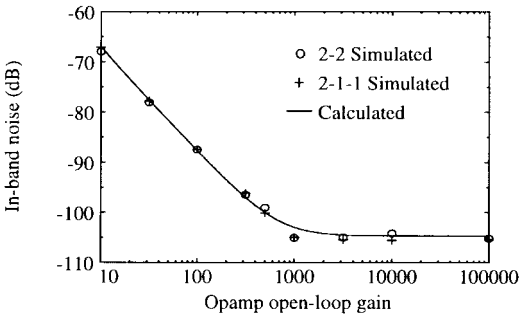

Fig. 9. In-band noise as a function of the op-amp open-loop gain.

term M^{-5} in the output power of the former can be deduced from previous reasoning taking into account that the second stage in the 2-1-1 is of first order. However, the contribution of this term is not measurable for practical values of M—the term in M^{-3} dominates for typical ranges of M (16 to 128). It is seen in Fig. 9, which shows the effect of the op-amp dc gain on the noise power in the band for $M = 32$ and $g = 0.25$. No difference is appreciable between both topologies regarding the sensitivity to integrator leakage.

B. Mismatching Between Coefficients

The equalities of Tables I and II, which nominally produce the correct cancellation of the quantization noise, are affected by mismatching of the physical components used to implement the integrator gains—capacitor ratios in the case of SC modulators. These mismatches introduce errors in the noise cancellation. This phenomenon can be modeled by introducing error terms in the digital and analog coefficients. Particularly, for the case of Table II

$$\begin{aligned} d_0 &= [1 - g_3'/(g_1g_2g_3)](1-\varepsilon_0) & g_1' &= g_1(1-\varepsilon_{g_1'}) \\ d_1 &= [g_3''/(g_1g_2g_3)](1-\varepsilon_1) & g_2' &= 2g_1'g_2(1-\varepsilon_{g_2'}) \\ d_2 &= [1 - g_3'/(g_1g_2g_3)]\varepsilon_{g_4'} & g_4' &= g_3''g_4(1-\varepsilon_{g_4'}). \\ d_3 &= [g_4''/(g_1g_2g_3g_4)](1-\varepsilon_3) \end{aligned} \tag{32}$$

Similar expressions are obtained for the 2-2 structure. In (32) each *epsilon* represents the relative error of the digital or analog coefficient, and can be calculated as

$$\begin{aligned} \varepsilon_0 &= \frac{\Delta g_3'}{g_3'} - \frac{\Delta g_1}{g_1} - \frac{\Delta g_2}{g_2} - \frac{\Delta g_3}{g_3} & \varepsilon_{g_1'} &= \frac{\Delta g_1'}{g_1'} \\ \varepsilon_1 &= \frac{\Delta g_3''}{g_3''} - \frac{\Delta g_1}{g_1} - \frac{\Delta g_2}{g_2} - \frac{\Delta g_3}{g_3} & \varepsilon_{g_2'} &= \frac{\Delta g_1'}{g_1'} + \frac{\Delta g_2}{g_2} \\ \varepsilon_3 &= \frac{\Delta g_4''}{g_4''} - \frac{\Delta g_1}{g_1} - \frac{\Delta g_2}{g_2} - \frac{\Delta g_3}{g_3} - \frac{\Delta g_4}{g_4} \\ \varepsilon_{g_4'} &= \frac{\Delta g_3''}{g_3''} + \frac{\Delta g_4}{g_4}. \end{aligned} \tag{33}$$

Performing analysis in the Z-domain with the digital coefficients given in (32) yields the following modulator output:

$$\begin{aligned} Y|_{2\text{-}2} = {} & Xz^{-4} + d_1(1-\varepsilon_1)(1-z^{-1})^4E_2 \\ & + 2(\varepsilon_{g_2'} - \varepsilon_1 - \varepsilon_{g_1'} - \varepsilon_{g_4'})z^{-1}(1-z^{-1})^3E_1 \\ & + (\varepsilon_1 + \varepsilon_{g_1'})z^{-2}(1-z^{-1})^2E_1 \end{aligned} \tag{34}$$

$$\begin{aligned} Y|_{2\text{-}1\text{-}1} = {} & Xz^{-4} + d_3(1-\varepsilon_3)(1-z^{-1})^4E_3 \\ & + d_1(\varepsilon_1 - \varepsilon_3)z^{-1}(1-z^{-1})^3E_2 \\ & + 2(\varepsilon_{g_2'} - \varepsilon_1 - \varepsilon_{g_1'} - \varepsilon_{g_4'})z^{-1}(1-z^{-1})^3E_1 \\ & + (\varepsilon_1 + \varepsilon_{g_1'})z^{-2}(1-z^{-1})^2E_1. \end{aligned} \tag{35}$$

Thus, in addition to the ideal quantization noise of the last stage, [see (4) and (6)], the noise of the remaining stages appears at the modulator output. Since the shaping functions of these new noise contributions have lower order than would be ideal, they can dominate the total in-band noise power. Calculation of this power under the usual assumption of $M \gg 1$ yields

$$\begin{aligned} P_Q|_{2\text{-}2} &= \frac{u_2^2}{12}\, d_1^2\, \frac{\pi^8}{9M^9} + \frac{u_1^2}{12}\left(\delta_A^2\, \frac{\pi^4}{5M^5} + \delta_B^2\, \frac{4\pi^6}{7M^7}\right) \\ P_Q|_{2\text{-}1\text{-}1} &= \frac{u_3^2}{12}\, d_3^2\, \frac{\pi^8}{9M^9} + \frac{u_1^2}{12}\left(\delta_A^2\, \frac{\pi^4}{5M^5} + \delta_B^2\, \frac{4\pi^6}{7M^7}\right) \\ & \quad + \frac{u_2^2}{12}\, d_1^2\delta_C^2\, \frac{\pi^6}{7M^7} \end{aligned} \tag{36}$$

where

$$\begin{aligned} \delta_A &= \varepsilon_1 + \varepsilon_{g_1'}, \quad \delta_B = \varepsilon_{g_2'} - \varepsilon_1 - \varepsilon_{g_1'} - \varepsilon_{g_4'} \\ \delta_C &= \varepsilon_1 - \varepsilon_3. \end{aligned} \tag{37}$$

Previous results are valid for any implementation style. Let us focus now on the SC implementation and try to find practical design guidelines. Using SC techniques, the analog coefficients are given by capacitor ratios

$$g_1 = \frac{C_i}{C_i^0} \Rightarrow \Delta g_i = g_i\left(\frac{\Delta C_i}{C_i} - \frac{\Delta C_i^o}{C_i^o}\right) \tag{38}$$

where Δg_i is a random variation of the nominal value g_i. From (38), and assuming that the mismatching in both capacitors are statistically independent, the equation of the standard deviation of the analog scalar is

$$\sigma_{g_i} = g_i\sqrt{\left(\frac{\sigma_{C_i}}{C_i}\right)^2 + \left(\frac{\sigma_{C_i^o}}{C_i^o}\right)^2}. \tag{39}$$

Note that the member on the right above contains the standard deviations of the capacitor values. These can in turn be calculated using the results in [19] as follows,

$$\sigma_{nC_u} = C\sqrt{\frac{n^{1/2}K_{le}}{C^{3/2}} + \frac{K_{lo}}{C} + \frac{nK_{ge}}{C} + K_{go}} \tag{40}$$

which assumes that a given capacitance C is divided into n unitary capacitors of value C_u, and where K_{le}, K_{ge}, K_{lo}, and K_{go} are constants related to the local and global effect of the edge errors (due to the etching process) and the oxide thickness variations, respectively. Since these constants are specific of the fabrication process, the only controllable variables in (40) are the unitary capacitor C_u and the number of these that form the capacitor C. Assuming that the capacitors C_i and C_i^o in (39) are formed by the connection of n_i and m_i unitary capacitors, respectively, results in

$$\begin{aligned} \sigma_{g_i} &= g_i\sqrt{\left(\frac{1}{n_i} + \frac{1}{m_i}\right)\left(\frac{K_{le}}{C_u^{3/2}} + \frac{K_{lo}}{C_u}\right) + \frac{2K_{ge}}{C_u} + 2K_{go}} \\ g_i &= n_i/m_i. \end{aligned} \tag{41}$$

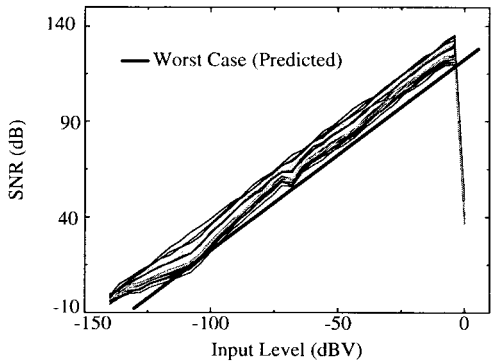

Fig. 10. SNR as a function of the input level with mismatching between coefficients (2-2).

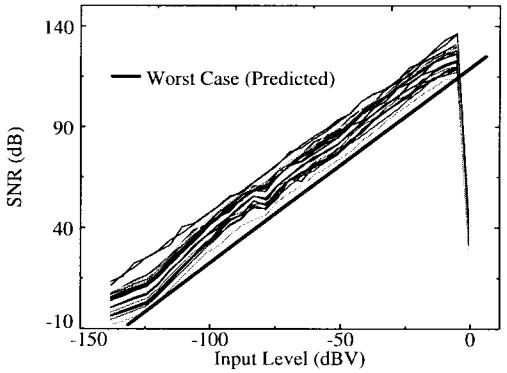

Fig. 11. SNR as a function of the input level with mismatching between coefficients (2-1-1).

TABLE IV
SIMULATION DATA AND RESULTS FOR 2-2 TOPOLOGY

Oversampling ratio	64
Reference voltages	1.0V
Unitary capacitance	0.25pF
Integrator gains	see Table 3
# tests	30
SNR-peak std. deviation	2.6%
Minimum SNR-peak	117dB

TABLE V
SIMULATION DATA AND RESULTS FOR 2-1-1 TOPOLOGY

Oversampling ratio	64
Reference voltages	1.0V
Unitary capacitance	0.25pF
Integrator gains	see Table 3
# tests	30
SNR-peak std. deviation	4.6%
Minimum SNR-peak	115dB

Expression (41) allows calculation of the standard deviation of each gain, and consequently that of the relative errors and combinations of these that appear in (33) and (37). However, it should be noticed that in (33) some coefficient variations are correlated since the coefficients have the same integration capacitor. Consider, for instance, the contribution of g_3 and g_3'' to ε_1, the relative error of d_1. From (38), one obtains

$$\sigma^2\left(\frac{\Delta g_3''}{g_3''}-\frac{\Delta g_3}{g_3}\right)=\sigma^2\left(\frac{\Delta C_3''}{C_3''}-\frac{\Delta C_3}{C_3}\right)=\frac{\sigma^2_{C_3''}}{C_3''^2}+\frac{\sigma^2_{C_3}}{C_3^2} \tag{42}$$

showing that the deviation in the integration capacitor C_3^o has been cancelled. This is reasonable since d_1 depends on the ratio g_3''/g_3, and hence the exact value of C_3^o does not matter.

Using (41), the worst case value of each relative error and their combinations can be estimated as three times the corresponding standard deviation. To evaluate the analytical expressions, Monte Carlo analysis has been performed through behavioral simulations assuming that each integrator gain presents a Gaussian distribution around its nominal value with standard deviation calculated from (41). The technological constants used are an update of those in [19]; the process is 1.2 μm CMOS n-well double-poly double-metal, and the updated constants are

$$K_{le}=5.8\times10^{-24}F^{3/2}\quad K_{ge}=1.932\times10^{-16}F$$
$$K_{lo}=1.133\times10^{-18}F\quad K_{go}=4\times10^{-4}. \tag{43}$$

With these values, for a typical unitary capacitor of 0.25 pF and an analog coefficient of 1/2, the standard deviation of the coefficient obtained applying (41) is 2.2%. However, the use of common centroid techniques for the implementation of capacitors makes it possible to attenuate the global effects (represented by the constants K_{ge} and K_{go}), reducing the standard deviation to 0.2%.

Fig. 10 shows a group of SNR curves obtained with the 2-2 topology, assuming that the scaling coefficients present a Gaussian distribution around their nominal value with standard deviations calculated from (41) considering compensated global effects (that is, $K_{ge}=K_{go}=0$). The corresponding simulation data appear in Table IV.

Fig. 11 and Table V present results from the 2-1-1 topology. Note that the analytic curve for the worst case (thick continuous line in Figs. 10 and 11) fits those obtained through statistic simulation in both architectures. The behavior simulations show that the 2-1-1 architecture is more sensitive to coefficient mismatching and presents a relative standard deviation in the SNR peak almost twice that of the 2-2 architecture (for the gains used).

IV. EXTENSION TO MULTIBIT QUANTIZATION

A few recent works have proposed to combine cascade architectures and multibit quantization in an attempt to attenuate the error induced by the internal D/A converter nonlinearity [10], [11], [20], [21]. The idea is to use a multibit quantizer only at the last stage of the cascade, keeping the others singlebit. Thus, the D/A converter nonlinearity error of this last stage is attenuated by a shaping function, provided by the cancellation logic, and filtered out by the digital decimator. Previous studies for a 2-1 and a 2-2 cascade modulator have

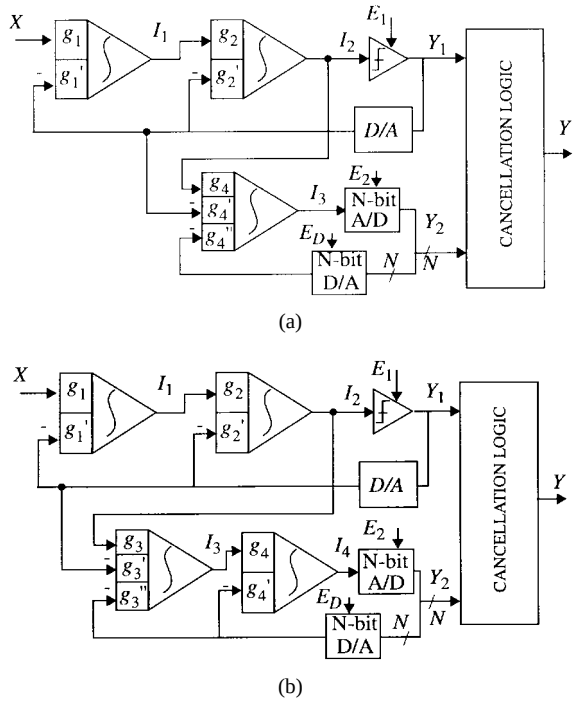

Fig. 12. Two cascade modulators with dual quantization: (a) Third-order two-stage (2-1mb) and (b) fourth-order two-stage (2-2mb).

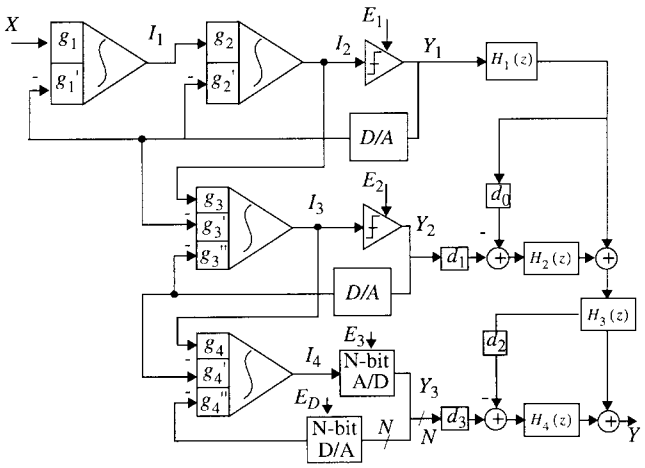

Fig. 13. Fourth-order three-stage cascade modulator with multibit quantization (2-1-1mb).

been presented in [10] and [21], respectively. Here we consider a 2-1-1 multibit architecture and compare its results to that of the former.

Fig. 12(a) and (b) shows the 2-1 and 2-2 cascade multibit modulators. In the presence of nonlinearity of the internal D/A converter, the Z-transform of the modulator outputs are given by

$$Y(z) \cong z^{-3}X(z) + d_1(1-z^{-1})^3 E_2(z) + d_1 z^{-1}(1-z^{-1})^2 E_D(z) \quad \{\text{2-1mb}\} \tag{44}$$

$$Y(z) \cong z^{-4}X(z) + d_1(1-z^{-1})^4 E_2(z) + d_1(1-z^{-1})^2 E_D(z) \quad \{\text{2-2mb}\} \tag{45}$$

where $X(z)$ represents the input signal, $E_2(z)$ is the quantization noise of an N-bit quantizer, and $E_D(z)$ is the noise associated to the nonlinearity of the last stage internal N-bit D/A converter. Note that this latter noise is multiplied by $(1-z^{-1})^2$ for both architectures. This means that the errors due to the internal D/A conversion are shaped after the cancellation stage as second-order errors. Based on the same principle, we propose to use multibit quantization in the third-stage of a 2-1-1 architecture (see Fig. 13). After digital cancellation,

$$Y(z) = z^{-4}X(z) + d_3(1-z^{-1})^4 E_3(z) + d_3(1-z^{-1})^3 E_D(z) \tag{46}$$

which shows that the D/A errors are attenuated in the signal band by a shaping function one order higher than for the previous architectures. As a result, better performance is obtained using the 2-1-1mb architecture for a given level of

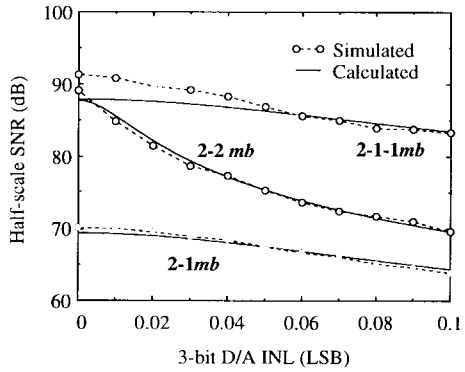

Fig. 14. Half-scale SNR as a function of the D/A INL for three cascade multibit architectures.

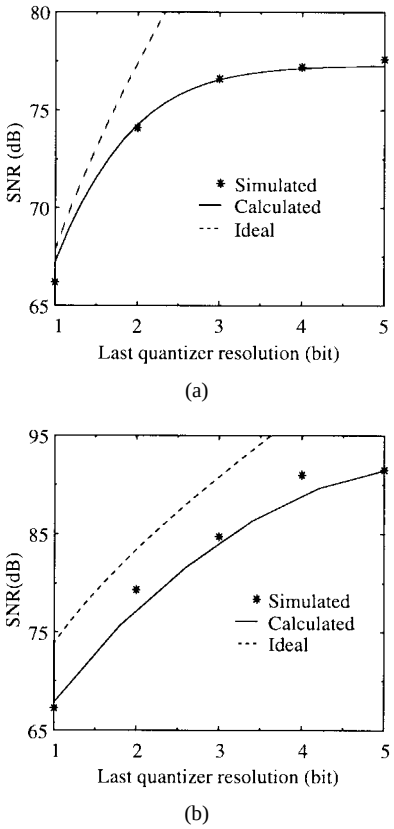

Fig. 15. SNR degradation as a consequence of the (a) integrator weight mismatching; and (b) the finite dc-gain of the integrators for a multibit 2-1-1 cascade modulator.

TABLE VI
COMPARATIVE EVALUATION

		2-2			2-1-1		
SINGLE-BIT CASE							
Oversampling ratio		32	64	128	32	64	128
Ideal behavior (Sim.)	SNR-peak (dB)	95	120	156	100	125	162
Non-ideal behavior (Simulated)	Required integrator output swing	$1.2V_r$			V_r		
	SNR-peak Standard deviation (dB)	0.74	2.4	4.7	1.64	4.6	7
	Worst Case SNR-peak (dB)	94	117	143	96	115	138
	Finite open-loop gain sensitivity	No practical differences					
Hardware complexity	# unitary capacitors	39			41		
	# comparators	2			3		
	# digital multipliers	2			3		
	# digital adders	2			3		
	# digital diferentiators	2			5		
EXTENSION TO MULTI-BIT (N=3)							
Oversampling ratio		16	32	64	16	32	64
Ideal behavior	SNR-peak (dB)	88	113	139	92	117	144
Non-ideal behavior	SNR-peak (dB) with 0.1LSB D/A non-linearity	70	84	101	84	105	124

nonlinearity in the D/A converter. This is better seen in the integrated noise power

$$P_{Q|2\text{-}1mb} = d_1^2 \left(\frac{u_{mb}^2}{12} \frac{\pi^6}{7M^7} + \sigma_D^2 \frac{\pi^4}{5M^5} \right)$$
$$P_{Q|2\text{-}2mb} = d_1^2 \left(\frac{u_{mb}^2}{12} \frac{\pi^8}{9M^9} + \sigma_D^2 \frac{\pi^4}{5M^5} \right)$$
$$P_{Q|2\text{-}1\text{-}1mb} = d_3^2 \left(\frac{u_{mb}^2}{12} \frac{\pi^8}{9M^9} + \sigma_D^2 \frac{\pi^6}{7M^7} \right) \quad (47)$$

where u_{mb} is the step between consecutive levels in the multibit quantizer and σ_D^2 represents the power of the D/A conversion error. In addition, the lower sensitivity of the 2-1-1mb to the D/A nonidealities is pointed out in Fig. 14. This shows the half-scale SNR as a function of the integral nonlinearity (INL) of a 3-bit D/A.

A. Influence of Other Nonidealities

The results obtained in Section III are fully applicable to cascade $\Sigma\Delta$M's with multibit quantizers. Thus, taking into account the finite dc-gain and capacitor mismatching, the in-band power for the 2-1-1mb $\Sigma\Delta$M can be approximated by combining (31), (36), and (47) to obtain

$$P_Q|_{2\text{-}1\text{-}1mb} = \frac{u_{mb}^2}{12} d_3^2 \frac{\pi^8}{9M^9} + \sigma_D^2 d_3^2 \frac{\pi^6}{7M^7} + \frac{u_{sb}^2}{12} \left(4\mu^2 \frac{\pi^2}{3M^3} + \delta_A^2 \frac{\pi^4}{5M^5} \right) \quad (48)$$

where u_{sb} represents the step between the two levels of the single-bit quantizers in the first and second stages. The presence of uncancelled quantization noise from the single-bit quantizer, the last term in (48), imposes an upper limit to the useful resolution of the last stage quantizer. Above this limit, the benefit of finer quantization (that is, lower u_{mb}) in the last stage is masked by this uncancelled noise. As a matter of example, Fig. 15 shows the half-scale SNR obtained by behavioral simulation for a 2-1-1mb modulator as a function of the number of bits of the last quantizer. These simulations include typical levels of weight mismatching and finite dc-gain in the integrators. The curve of Fig. 15(a) corresponds to the worst-case obtained in a Monte-Carlo analysis including mismatching in the integrator weights implemented using a unitary capacitor of 0.5 pF. In Fig. 15(b) a dc-gain of 1000 was assumed for the integrators. The oversampling ratio was 16 in both cases. Note that the curve in Fig. 15(a) saturates for $N > 3$ because the uncancelled first stage quantization noise dominates the in-band noise power. According to these results, using a quantizer with more than 3 bit resolution does not make sense in this case.

V. CONCLUSIONS

Table VI presents a summary of the conclusions derived from this work. Data corresponding to the single-bit case have been obtained for reference voltages of ± 1 V, a unitary capacitor of 0.25 pF, and $M = 32, 64,$ and 128. The minimum capacitor was of 1 pF so that the minimum number of parallel-connected unitary capacitors was four.

From the top part of Table VI the following conclusions are drawn

- The 2-2 single-bit modulator with the integrator gains in Table III presents slightly lower sensitivity to the capacitor mismatching than the 2-1-1 single-bit architecture. In both cases, but especially in the 2-1-1 single-bit, the worst case performance must be contemplated

in the design process. Generally speaking, it can be said that high-order cascade modulators are useful for low or medium oversampling ratios. Otherwise, the high matching requirements lead to unpractical designs.

- Both architectures have similar behavior with regard to the influence of the finite dc-gain.
- The hardware complexity is slightly lower for the 2-2 single-bit architecture.

The bottom part of Table VI refers to the multibit case. Data in this case have been obtained for a reference voltage of ± 1 V, and $M = 16$, 32, and 64. Note that, for given M, the loss of SNR due to the nonlinear D/A of the 2-2 modulator is approximately twice that of the 2-1-1.

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