Highly Linear 2.5-V CMOS $\Sigma\Delta$ Modulator for ADSL+

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***Abstract*—We present a 90-dB spurious-free dynamic range sigma–delta modulator ($\Sigma\Delta$M) for asymmetric digital subscriber line applications (both ADSL and ADSL+), with up to a 4.4-MS/s digital output rate. It uses a cascade (MASH) multibit architecture and has been implemented in a 2.5-V supply, 0.25-μm CMOS process with metal–insulator–metal capacitors. The prototypes feature 78-dB dynamic range (DR) in the 30-kHz to 2.2-MHz band (ADSL+) and 85-dB DR in the 30-kHz to 1.1-MHz band (ADSL). Integral and differential nonlinearity are within $\pm$0.85 and $\pm$0.80 $LSB_{14\ b}$, respectively. The $\Sigma\Delta$ modulator and its auxiliary blocks (clock phase and reference voltage generators, and I/O buffers) dissipate 65.8 mW. Only 55 mW are dissipated in the $\Sigma\Delta$ modulator.**

***Index Terms*—Analog-to-digital converter (ADC), asymmetric digital subscriber line (ADSL), MASH, sigma–delta modulation, switched-capacitor circuits.**

I. Introduction

SUPPORTED by a considerable commercial success, wireline solutions for broad-band access and home networking are evolving to provide ever increasing data rates and more functionality. An asymmetric digital subscriber line (ADSL) is an example of such applications and extensions of it like ADSL+ (with doubled number of channels) or very-high-data-rate digital subscriber line (VDSL), providing video-rate reception) are just round the corner. As this trend goes on, the demand for highly linear, fast analog front-ends challenges mixed-signal designers to achieve accuracies of 12–15 b for signal bandwidths ranging from 1.1 to 12 MHz [1].

Although these specifications seem *a priori* better suited for Nyquist architectures, such as pipeline analog-to-digital converters (ADCs) [2], these architectures do not exhibit enough linearity for some telecom applications, especially in low-voltage implementations, unless the power consumption is significantly increased. For this reason, oversampled ADCs have gained ground in this frequency range. Specifically, sigma–delta modulators ($\Sigma\Delta$Ms) [3], [4] exhibit high intrinsic linearity, making use of relatively simple analog circuitry, which render them worth exploring for broad-band wireline and baseband radio-frequency communications [5]–[22].

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Given the high signal bandwidths required in wireline communication, only low-oversampling ratio (M) $\Sigma\Delta$Ms are feasible. In order to keep the resolution levels with these low values of M, the well-known formulas for the dynamic range (DR) and the effective number of bits (ENOB) [3]

$$\mathrm{DR_{dB}} = 10\log\left[\frac{3}{2}(2^B-1)^2\frac{(2L+1)M^{2L+1}}{\pi^{2L}}\right]$$
$$\mathrm{ENOB} = \frac{\mathrm{DR_{dB}} - 1.76}{6.02} \quad (1)$$

dictate that either high-order loop filtering (increasing the $\Sigma\Delta M$ order L) or multibit quantization (increasing the resolution of the quantizer B), or both must be used. However, these strategies raise issues that jeopardize robustness of highly oversampled, low-order single-bit $\Sigma\Delta$Ms. On the one hand, high-order $\Sigma\Delta$ loops are prone to instability and the stabilization methods proposed have resulted in complex architectures whose DR is degraded with respect to that in (1) [3].This degradation is more notorious for single-bit quantizers, so that the combination of high-order loops with single-bit quantization is not a good choice for high-frequency designs [3]. On the other hand, multibit conversion entails extreme sensitivity to the nonlinearity of the digital-to-analog converter (DAC) in the feedback path and forces the use of correction/calibration techniques [23]–[25]. Unfortunately, since DACs cannot be efficiently linearized within an arbitrarily large resolution, the use of low-order multibit modulation may not be enough to obtain a given DR.

A direct solution to this problem is to increase both the modulator order and the internal quantizer resolution, giving rise to moderate-order (3–5), multibit architectures. In fact, the use of multibit quantization (typically up to 4 b) in single-loop high-order $\Sigma\Delta$Ms inherently improves their stability [3], so that these are good candidates to obtain high-resolution, high-frequency operation, provided that the nonlinearity problem is solved [8], [9], [13], [21]. With the same objective, the combination of high-order cascade (MASH) architectures [26] with multibit quantization has been proposed [18], [27]. These modulators gather the unconditional stability of cascade modulators (only second- and/or first-order stages are used) and the advantages of multibit quantization with relaxed requirements for the linearity of the DAC. The feasibility and efficiency of this approach, because it needs no correction/calibration mechanisms, has already been proven [10]–[12], [17]–[20].

In this paper, we present the design of a $\Sigma\Delta$M for ADSL+ applications in a 2.5-V, 0.25-μm CMOS process. With this

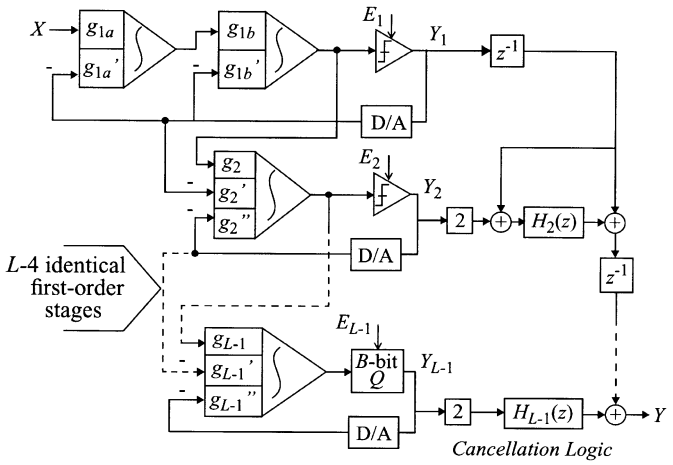


Fig. 1. Lth-order $\Sigma\Delta$ modulator using a $2-1^{L-2}$ cascade.

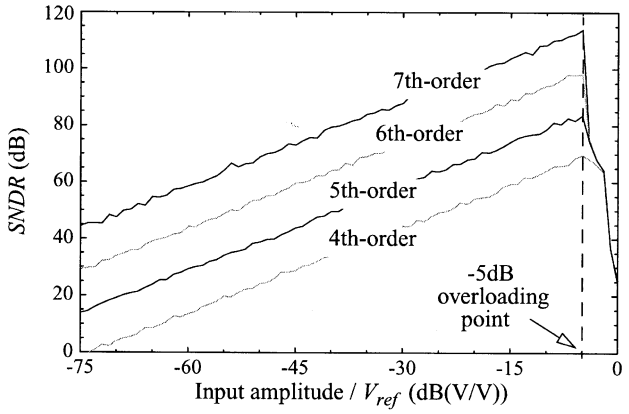


Fig. 2. SNDR versus input level for several modulator orders.

goal, a family of $\Sigma\Delta$M architectures capable of achieving high resolution with a low oversampling ratio are devised in Section II. Section III studies the impact of deep-submicrometer features on the architecture selection, providing optimized architecture parameters for the specifications considered. Circuit implementation and related design considerations are explained in Sections IV–VI. Finally, Section VII shows experimental results of the $\Sigma\Delta$M and compares its performance with state-of-the-art designs.

II. Low-Oversampling Cascade $\Sigma\Delta$ Modulators

Fig. 1 shows the generic block diagram of a family of high-order cascades. It is an Lth-order modulator formed by a second-order stage followed by $L-2$ identical first-order stages ($2-1^{L-2}\Sigma\Delta$M). The values of the integrator weights are

$$\begin{aligned} g_{1a} &= g'_{1a} = 0.25 \\ g_{1b} &= 1, \quad g'_{1b} = 0.5 \\ g_k &= 1, \quad g'_k = 0.5, \quad g''_k = 0.5 \\ k &= 2, \ldots, L-1. \end{aligned} \tag{2}$$

As in all cascade $\Sigma\Delta$Ms [26], the outputs of the $L-1$ stages are processed in the digital domain through simple operators $H_k(z) = (1-z^{-1})^k$ and combined to cancel out the quantization noise generated in each stage but the last one. Additionally, a pseudomultibit operation [18], [27] is achieved by including multibit quantization only in the last stage, while the remaining are single bit. Linearized z-domain analysis shows that the modulator output can be expressed as follows [4]:

$$\begin{aligned} Y(z) = z^{-L} \cdot X(z) + 2(1-z^{-1})^L \cdot E_N(z) \\ +2(1-z^{-1})^{(L-L_N)} \cdot E_{\mathrm{INL}}(z) \end{aligned} \tag{3}$$

where $X(z)$ stands for the input signal, which is simply delayed, $E_N(z)$ is the last-stage quantization error, which is shaped by an Lth -order function, and $E_{\mathrm{INL}}(z)$ represents the nonlinearity error of the last-stage DAC. Note that, since $E_N(z)$ is generated in a B-bit quantizer, the modulator response equals that of an ideal Lth-order B-bit $\Sigma\Delta$M, except for the factor 2. The aim of this factor, that equals $g''_{L-1}/(g'_{1a}g_{1b}g_2 \ldots g_{L-1})$, is to compensate for the signal scaling required to avoid premature overloading of the modulator. By integrating the error terms in (3) over the signal band, the in-band quantization error power is obtained [4] as

$$P_Q = \sigma^2_{mQ}\frac{4\pi^{2L}}{(2L+1)M^{2L+1}} + \sigma^2_{\mathrm{INL}}\frac{4\pi^{2(L-1)}}{(2L-1)M^{2L-1}} \tag{4}$$

where

$$\sigma^2_{mQ} = \frac{\left(\frac{2V_{\mathrm{ref}}}{2^B-1}\right)^2}{12} \quad \sigma^2_{\mathrm{INL}} = \frac{(2V_{\mathrm{ref}} \times INL)^2}{2} \tag{5}$$

are the total power associated with the last-stage quantization error and the DAC nonlinearity error, respectively, with INL being the DAC integral nonlinearity relative to the input full scale $(2V_{\mathrm{ref}})$.

Since the factor 2 in (3) quadruples the in-band power of these errors, a 1-b systematic loss of resolution is generated. However, this loss is small when compared to other cascade $\Sigma\Delta$Ms and, more importantly, it is constant, regardless of the number of stages. In fact, the most appealing feature of this architecture (with the set of coefficients proposed) is that it can be easily set to any order just by changing the number of identical first-order stages. As shown in Fig. 2, a correct operation is maintained with constant overloading point, regardless of the overall order.

The coefficients in (2) also have the following interesting properties.

1) The output swing required in all integrators is only the quantizer full-scale.
2) By proper sharing of the switched-capacitor (SC) input stages, they can be implemented with just two-branch integrators, which minimizes the number of unitary capacitors.
3) All first-order stages, but the last one in case of using multibit quantization, contain the same coefficients, so that they can be electrically identical.

This considerably simplifies the electrical and physical implementation of the modulator.

A. Nonideal Performance

SC implementations of cascade modulators suffer from certain nonideal behaviors more than their single-loop counterparts, namely: finite (and nonlinear) amplifier dc gain and ca-

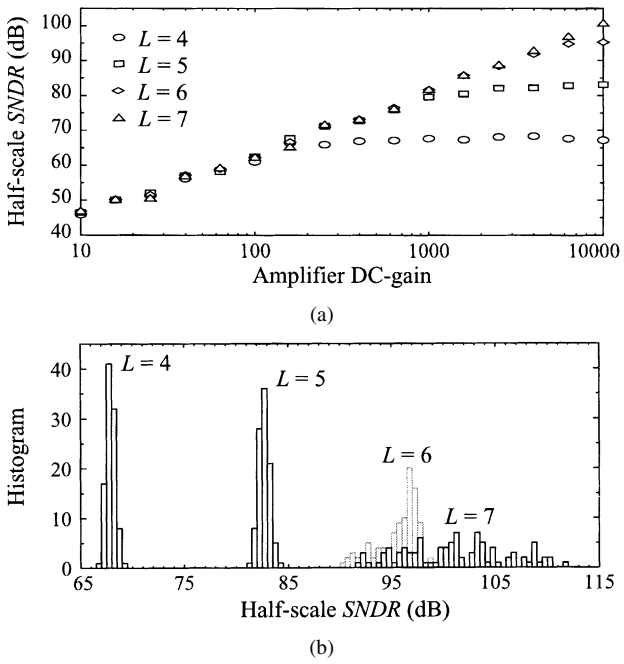


Fig. 3. Effect of (a) finite dc gain and (b) weight mismatch on the SNDR of single-bit $2-1^{L-2}\Sigma\Delta$Ms for $M=16$.

pacitor mismatch [4]. Both nonidealities modify the ideal integrator z-domain transfer function, thus altering the quantization error transfer function. Since this variation is not correlated to changes of the cancellation logic, mismatch appears between the analog and digital processing that precludes perfect cancellation of the low-order quantization error. Into first-order approximation, the in-band power of the error leakages is independent of L, because they are generated in the modulator first stage, which is the same for whatever L [4]

$$\Delta P_Q(A_v,\sigma_C)=\sigma_{sQ}^2\left(\frac{25}{48}\frac{\pi^2}{A_v^2M^3}+36\sigma_C^2\frac{\pi^4}{5M^5}\right)$$
$$\sigma_{sQ}^2=\frac{(2V_{\rm ref})^2}{12} \tag{6}$$

where A_v stands for the first-stage amplifier dc gain, and σ_C is the capacitor ratio standard deviation. If we compare (4) and (6) for a given M, it is clear that for certain values of A_v, σ_C, and L these effects may dominate the in-band error power, thus imposing an upper bound to the practical values of L.

In order to estimate this limit under realistic circuit imperfections, Fig. 3(a) shows the simulated half-scale SNDR as a function of the amplifier dc gain for $M=16$. Fig. 3(b) shows the SNDR histograms obtained from Monte Carlo simulation assuming 0.1% sigma in capacitor ratios—0.05% is currently featured by metal–insulator–metal (M-i-M) capacitors in CMOS processes. Under these conditions, mainly because of the matching sensitivity, the seventh-order architecture seems not worth implementing for $M=16$. Nevertheless, the sixth-order modulator provides a 90-dB worst-case SNDR with dc gain of 2500. Especially robust is the fifth-order cascade requiring a dc gain of 1000 to achieve 80-dB worst-case SNDR with $M=16$. It is important to remark that these gains are basically needed for the first-stage amplifiers. The dc-gain requirement for the integrators in the remaining $L-2$ stages

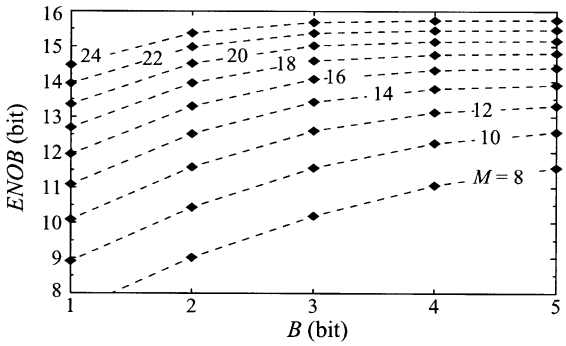


Fig. 4. ENOB versus last-quantizer resolution for a $2-1^2\Sigma\Delta$M in the presence of circuit imperfections.

of the cascade are much more relaxed. This is also applicable to other circuit imperfections such as electronic noise, finite dynamics, nonlinearity, and mismatch. This practice allows us to use simpler circuit topologies and layouts for these stages, thus saving area and power consumption.

Likewise, in practice, the number of bits in the last-stage quantizer (B) cannot be arbitrarily large. As shown in Fig. 4, for a given M, the evolution of the overall effective resolution with B tends to saturate due to the presence of leakage. Nevertheless, depending on the signal bandwidth, the reduction in oversampling ratio that can be achieved by resorting to multibit quantization may define the border between feasible and infeasible implementations. As we will show further on, proper selection of the three main design parameters (L, M, and B) is the key to really efficient implementations.

III. Deep-Submicrometer Design Considerations

Viability of cascade multibit ΣΔMs in deep-submicrometer CMOS is related to two main process features: supply voltage and capacitor performance. The supply voltage, through the selection of the reference voltages, defines the available dynamic range, but also makes an impact on the selection of the amplifier topology and its capability to trade open-loop dc gain, speed, and output swing [28]. An empirical upper bound for a feasible $V_{\rm ref}$ is given by

$$V_{\rm ref}=V_{\rm supply}-n_{\rm ob}V_{\rm sat};(\text{references are } \pm V_{\rm ref}) \tag{7}$$

where $V_{\rm sat}$ is the saturation voltage of the amplifier output devices and $n_{\rm ob}$ is the number of transistors in the output branch, which again depends on the specific amplifier topology. If a single-stage amplifier is used, cascode devices will be required to achieve enough dc gain, so that $n_{\rm ob}\geq 4$. This common choice is not adequate in low-voltage implementations, where an excessive value of $V_{\rm sat}$ will result in a ridiculously small value for $V_{\rm ref}$. Among the alternatives, we count on two-stage amplifiers [28], whose output branch can contain only two transistors $(n_{\rm ob}=2)$ still producing a large open-loop dc gain. This allows us to increase the value of $V_{\rm ref}$ up to useful levels at the price of an increased power dissipation. Apart from the amplifiers, the performance of the switches with supply voltages below 2.5 V needs careful control, especially for dynamic distortion considerations [29]. For broad-band ΣΔMs, solutions are in the clock-boosting strategies [30] or in the employment of

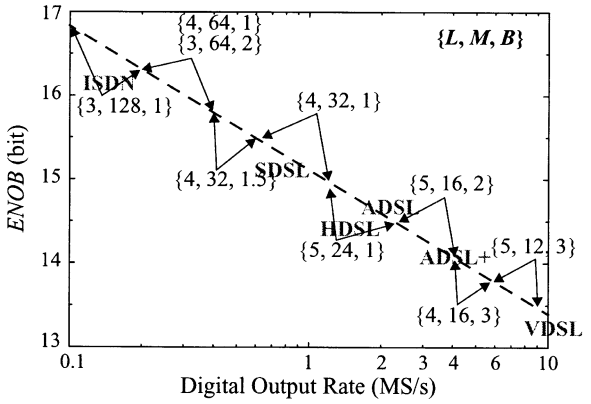


Fig. 5. Most efficient cascade $\Sigma\Delta$M for each region of the resolution-speed plane.

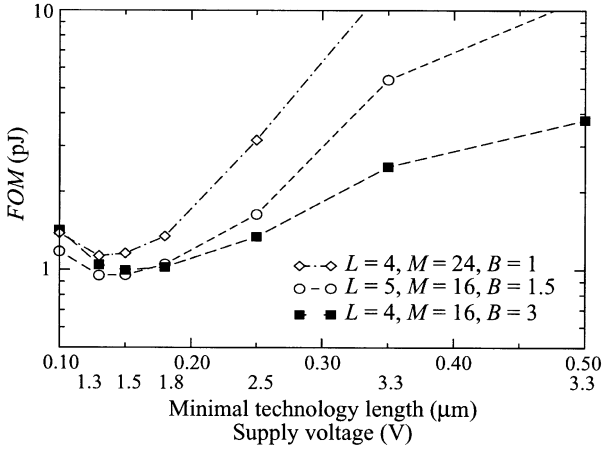


Fig. 6. Estimated evolution of the FOM with technology scaling for three cascade architectures obtaining 14 b@4.4 MS/s.

high-voltage devices available in double-oxide processes, with the subsequent increase in price, circuit complexity, and power dissipation.

The second most relevant technology feature has to do with the quality of the capacitor structures. According to the results shown in Section II, typical capacitor matching requirements range from 0.1% to 0.2% standard deviation. Low parasitics are also of extreme importance for an efficient implementation of a high-frequency modulator, and finally, we have the capacitor linearity requirements, which are less demanding provided that symmetrical fully-differential circuitry is used. Fortunately, M-i-M capacitors are now available in CMOS processes. They exhibit an excellent matching and linearity, with very small bottom parasitics.

In order to quantitatively evaluate previous assumptions, we have developed an analytical procedure to estimate the power consumption of different cascade single-bit and/or multibit $\Sigma\Delta$Ms. In the underlying expressions, detailed in the Appendix, both architecture and technological features are contemplated, together with simplifying assumptions inspired in practical design solutions. The aim here is not only to draw conclusions about architectural choices, but also to track their evolution under technology changes. To this end, the following figure-of-merit (FOM) has been used [31]:

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \text{DOR}} \times 10^{12} \tag{8}$$

where DOR stands for the digital output rate, i.e., the Nyquist rate.

In a first comparison step, the triads $\{L, M, B\}$ describing specific cascades have been evaluated along the curve in the resolution-speed plane shown in Fig. 5 (dashed line). Although this particular resolution-speed relationship is arbitrary, it fits the usual requirements for wireline telecom ADCs: integrated services digital network (ISDN), ADSL, VDSL, etc., which have been placed in the figure for illustration. For each section of the resolution-speed curve, the architecture with the minimum FOM has been noted. Observe that, as the output rate increases, the oversampling ratio decreases and, simultaneously, the increased number of bits in the multibit quantizer shows up to compensate for the oversampling reduction. Note that the 4.4-MS/s DOR employed in ADSL+ falls into the region led by the architecture $\{4, 16, 3\}$, i.e., a fourth-order 2–1-1 cascade with 3-b quantization in the last stage and using a 16 oversampling ratio, which will be our choice.

In a second step, we take advantage of the fact that some technology features enter the above formulation to predict how the performance of the cascade $\Sigma\Delta$Ms is going to evolve under technology changes. Fig. 6 shows the estimated evolution of the FOM of three cascade topologies, namely $\{4, 24, 1\}$, $\{5, 16, 1.5\}$, and $\{4, 16, 3\}$, aimed at obtaining 14 b at 4.4 MS/s. These are typical specifications for ADSL+ modems. Two facts are noticeable.

- Despite the reduction of the supply voltage, overall, the power dissipation does not decrease below 0.18 μm. This is basically due to the reduction in supply voltages, which imposes a reduction in the reference voltage and, hence, a compensating increase in the sampling capacitors. Since the incomplete settling error power must be also kept constant, this mechanism leads to an increased current absorption, which makes the overall power consumption increase below 0.18 μm. The location of the inflection point depends on the converter specifications. For instance, if for the same speed, the resolution is to be increased, the inflection point moves to the right in Fig. 6.
- Another aspect illustrated in Fig. 6 is the dynamic nature of the architecture selection in Fig. 5. Note that the $\{4, 16, 3\}$ $\Sigma\Delta$M outperforms for 0.25 μm and above, but it does not below 0.18 μm.

IV. SC Implementation

Fig. 7 shows the fully differential SC schematic of the $\{4, 16, 3\}$ $\Sigma\Delta$M. The first stage of the cascade includes two integrators—with one and two input branches, respectively—and switches controlled by the comparator outputs to feed the quantized signal back. The second stage uses an integrator with only two input branches to implement weights g_2, g_2', and g_2'', since the values in (2) allow distribution of g_2 between the two branches. The same applies for g_3 in the third stage. The third-stage integrator drives the 3-b ADC and the loop is closed by a 3-b DAC. The 1-of-8 output code of the ADC is converted

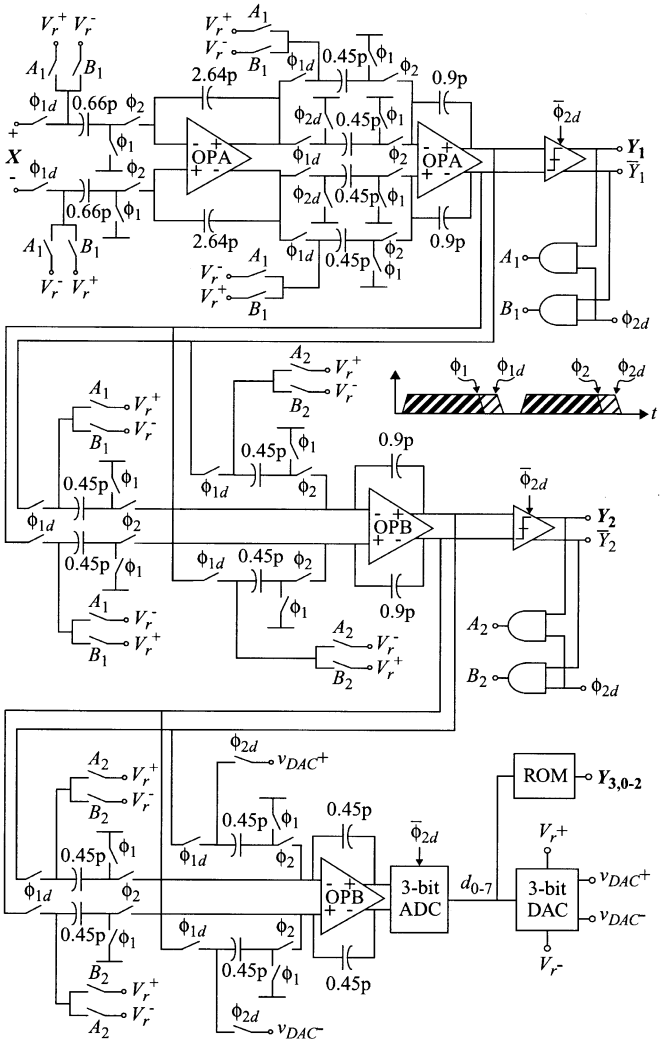


Fig. 7. SC implementation of the $2-1^2$ multibit ΣΔ modulator.

into binary by a read-only memory (ROM) that generates the corresponding bitstreams.

The modulator operation is controlled by two nonoverlapped clock phases. The integrator input signals are sampled during phase ϕ_1. During phase ϕ_2, the algebraic operations are performed and results are accumulated in the feedback capacitors. In order to attenuate the signal-dependent clock-feedthrough, delayed versions of the two phases (ϕ_{1d} and ϕ_{2d}) are also provided. This delay is incorporated only to the falling edges of the signals (switches turn off), while the rising edges are synchronized in order to increase the effective time-slot for the modulator operations [15]. The comparators and the last-stage ADC are activated at the end of ϕ_2—using $\bar{\phi}_{2d}$ as strobe—to avoid any possible interference due to the transient response of the integrators at the beginning of sampling.

V. Specifications for the Building Blocks

The converter specifications have been mapped onto basic building block requirements by following an optimization process supported by behavioral simulations [4]. Table I summarizes the modulator sizing achieving 13 b@4.4 MS/s. Five groups of specifications are enclosed: modulator, front-end integrator, amplifier, comparator, and A/D/A converter. In this procedure, the worst-case performance has been evaluated in the presence of variations in the process (for instance, changes in the capacitor absolute value), temperature, and supply. Table II shows a summary of the most significant contributions to the in-band error power. Main considerations made for this sizing are described next.

The first step of the modulator sizing is the selection of $V_{\rm ref}$. In this selection, both the overloading characteristics of the modulator and the nature of the signal being converted must be considered. In our case, the overloading point is nearly -5 dB

TABLE I
Modulator Sizing

Modulator	{4, 16, 3}	Topology	2-1-1
		Dual-quantization	1bit / 3bit
		Oversampling ratio	16
	Reference voltage		1.5V
	Clock frequency		70.4MHz
	Clock jitter		15ps
Front-End Integrator	Sampling capacitor		0.66pF
	Unitary capacitor		0.66pF
	Capacitor standard deviation (1-pF M-i-M)		0.05%
	Capacitor tolerance		±20%
	Bottom parasitic capacitor		1%
	Switch on-resistance		150Ω
Amplifier	Open-loop DC-gain		3000
	Equivalent input noise		$6\text{nV}/\sqrt{\text{Hz}}$
	Gain-bandwidth product (1.5-pF load)		265MHz
	Slew-rate (1.5-pF load)		800V/μs
	Differential output swing		±1.8V
Comparator	Hysteresis		20mV
	Offset		±10mV
	Resolution time		3ns
	Input capacitance		0.2pF
A/D/A Converter	Resolution		3bit
	DAC *INL*		0.5%*FS*

TABLE II
Main In-Band Error Contributions

	Nominal	Worst-Case
Quantization Noise	-88.1dB	-86.2dB
Ideal quantization noise	-90.3dB	
Amplifier DC-gain leakage	-99.8dB	
Capacitor mismatch leakage (σ_C = 0.05% | σ_C = 0.1% for 1pF)	-95.4dB	-89.4dB
DAC non-linearity error	-96.4dB	
Thermal Noise	-84.8dB	-82.2dB
kT/C noise	-88.1dB	-86.0dB
Amplifier noise	-87.5dB	-84.5dB
Clock Jitter	-90.1dB	
In-Band Error Power	-82.3dB	-80.3dB
Dynamic Range (extrapolated to the reference voltage)	82.8dB (13.5bit)	80.8dB (13.1bit)

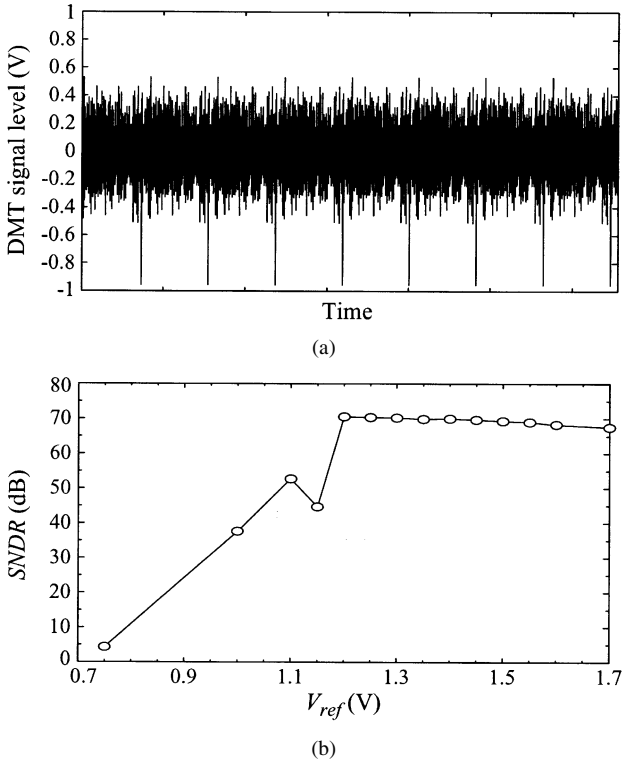


Fig. 8. (a) Time-domain representation of a −15-dB DMT signal. (b) SNDR of the converted DMT signal as a function of the reference voltage.

(see Fig. 2), while the largest input is the −15-dB discrete multitone (DMT) signal shown in Fig. 8(a). Note that, although its power is not too high, large peaks appear from time to time, thus yielding the high crest factor [32] peculiar to DMT signals (5.4 in our case). Fortunately, the duration of these peaks is short enough not to overload the modulator. In order to illustrate this, Fig. 8(b) shows behavioral simulation results of the modulator SNDR for such an input signal as a function of the reference voltage. In spite of the presence of a signal peak of approximately −1 V, the modulator SNDR is correct up to $V_{\rm ref} = 1.3$ V (note that this would never be the case for a 1-V amplitude input sinewave, since it would be inside the modulator overloaded region with 1.3-V reference). In order to provide a safety margin, $V_{\rm ref} = 1.5$ V was taken. Returning to (7), this reference voltage gives us a margin of 500 mV per output transistor in a two-stage fully differential amplifier supplied with 2.5 V. As shown in Fig. 7, $V_{\rm ref}$ is implemented using differential references, so that $V_{\rm ref} = V_r^+ - V_r^-$.

In Table II, the in-band error power of quantization error has been split up in its four contributions associated to: the ideal quantization error [first term in (4)], finite dc gain [first term in (6)], capacitor mismatch [second term in (6)], and last-stage DAC nonlinearity [second term in (4)]. Note that the quantization error leakage will be dominated by capacitor mismatch. Although M-i-M capacitors exhibit good matching—$\sigma_C = 0.05\%$ for 1-pF caps—the use of small unitary capacitors (0.66 pF) for dynamic considerations increases the sensitivity of the cascade, so that we have assumed twice that value for σ_C. The contribution of the 3-b DAC nonlinearity is 6 dB below the ideal quantization noise for INL $= 0.5\%$ FS, which is easily achievable without calibration. The noise leakage due to the amplifier dc gain is almost negligible for $A_v = 3000$. However, as we explain further on, this value will not be further relaxed in order to avoid excessive distortion due to dc-gain nonlinearity.

Following the discussion in Section III and in the Appendix, a small sampling capacitor ($C_S = 0.66$ pF) is used in order to reduce the capacitive load of the integrators and, hence, their power dissipation. So, white circuit noise becomes the dominant error source. A more exact expression (than the one used in the Appendix) for its in-band error power is [3]

$$P_{\rm Th} = P_{kT/C} + P_{\rm Th}^{\rm OTA} = \frac{4kT}{MC_S} + \frac{(2\pi){\rm GB}_{\rm eff}}{2M} S_{\rm Th,in} \quad (9)$$

where $S_{\rm Th,in}$ is the amplifier input-referred white noise and $\rm GB_{eff}$ is the effective amplifier gain–bandwidth product (in Hz), which during integration can be approximated to

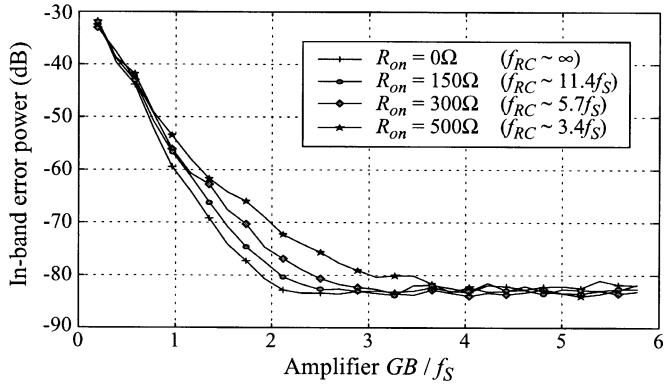
$${\rm GB}_{\rm eff} = \frac{\rm GB}{1 + \frac{\rm GB}{f_{\rm RC}}} = \frac{\rm GB}{1 + {\rm GB} \cdot (2\pi) \cdot 2R_{\rm on}C_S} \quad (10)$$

where GB is the amplifier gain–bandwidth product (in Hz), $R_{\rm on}$ is the switch on-resistance, and $f_{\rm RC}$ is the pole associated with the RC constant of the SC branch during integration.

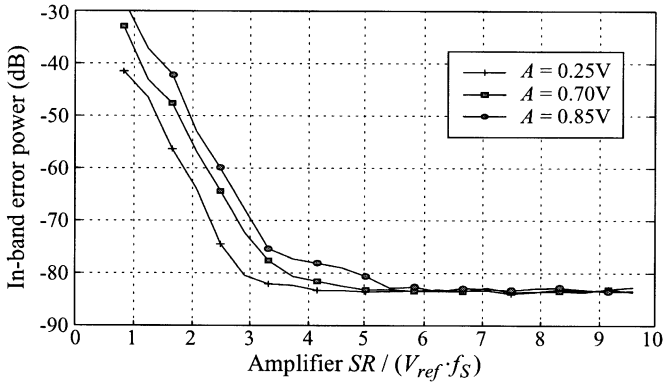
The first contribution in (9) yields a worst-case value of −86.0 dB—for maximum temperature (+110 °C) and −20% tolerance in the capacitor value. On the other hand, for GB and $R_{\rm on}$ fixed according to settling considerations to 265 MHz and 150 Ω, respectively, $\rm GB_{eff}$ will be 250 MHz. An equivalent thermal noise at the amplifier input of 6 $\rm nV\sqrt{Hz}$ is therefore enough to obtain a noise contribution similar to that of the kT/C noise (−87.5 dB). Besides, the worst-case amplifier white noise contribution corresponds to the largest $\rm GB_{eff}$, which varies along the process corners. Assuming that it can be as large as twice its nominal value (i.e., 500 MHz), this worst-case contribution yields −84.5 dB.

The limited amplifier GB introduces basically a gain error in the integrator transfer function. This error is especially important in the integrators of the first stage of the cascade, because the quantization error of this stage will leak to the modulator output. For the architecture considered operating with $M = 16$, the amplifier must fulfill GB $> 2.5 f_S$ to avoid degradation of the modulator performance due to incomplete settling, f_S being the sampling frequency.

If the finite on-resistance $R_{\rm on}$ of the switch is also considered, the effective amplifier response is slowed down, as stated in (10). This effect is illustrated in Fig. 9(a) that shows behavioral simulation results for the in-band error power as a function of the normalized amplifier GB, for different values of $R_{\rm on}$. The corresponding values of the normalized RC pole are also depicted. Note that, as the RC pole decreases, the amplifier GB must be increased in order to compensate for the slowdown. A switch resistance of 150 Ω is fixed for this design. On the one hand, as we show further on, this resistance can be obtained using standard CMOS transmission gates, without clock boosting. On the other, the amplifier GB must be increased just to GB $> 3.2 f_S$ in order to maintain the modulator performance. Assuming that approximately 85% of the clock period is left for the integrator operation (after ensuring nonoverlapping and delay in the clock-phase signals), the required GB is approximately 265 MHz.



(a)



(b)

Fig. 9. (a) In-band error versus normalized amplifier GB for different switch on-resistances. (b) In-band error versus normalized amplifier SR for different input amplitudes.

The required amplifier slew rate (SR) is established guarantying that the slew-rate limited evolution at the beginning of integration and sampling [33] is fast enough for the subsequent linear dynamic to settle to the desired accuracy. For this modulator, a normalized SR $\mathrm{SR}/(V_{\mathrm{ref}} \cdot f_S) = 5$ is sufficient to ensure correct performance. However, since the operation of the front-end integrator is partially SR limited, the dynamic will be also partially nonlinear and appreciable harmonic distortion may arise. This effect is illustrated in Fig. 9(b), where behavioral simulation results are shown for the modulator in-band error power versus the normalized amplifier SR, for different amplitudes of a sinewave input. Note that, for the correct conversion of an input sinewave of maximum amplitude (0.85 V), the normalized SR must be increased up to 6.5. Assuming that 85% of the clock period is left for the integrator operation, the required SR is approximately 800 V/μs.

Thanks to oversampling, some specifications in Table I referring to the front-end integrator can be relaxed for the rest of integrators. Specifically, the value of the sampling capacitor in those integrators can be progressively scaled down, since their contributions to the overall kT/C noise are attenuated in the signal band. Nevertheless, matching considerations and reliability preclude using very small capacitors. In this design the scaling of the nominal C_S (0.66 pF) is limited to 32%, which means that 0.45-pF unitary capacitors are used in the rest of integrators. On the contrary, the input-referred white noise of the amplifiers at the modulator back-end can be considerably increased without jeopardizing performance.

TABLE III
SCALING OF THE AMPLIFIER SPECIFICATIONS

SPECs	1st Integ	2nd Integ	3rd Integ	4th Integ
Unitary capacitor	0.66pF	0.45pF	0.45pF	
Gain-bandwidth product (1.5-pF load)	265MHz		210MHz	
Slew-rate (1.5-pF load)	800V/μs		350V/μs	
Open-loop DC-gain	3000		600	
Input equivalent noise	$6\mathrm{nV}/\sqrt{\mathrm{Hz}}$		$50\mathrm{nV}/\sqrt{\mathrm{Hz}}$	
Differential output swing	±1.80V		±1.60V	

A more aggressive reduction can be applied to the other circuit requirements. For instance, the amplifier dc gain of the third and fourth integrators can be reduced to 600, because the in-band powers of the respective quantization error leakages are proportional to M^{-5} and M^{-7}, and the effect of their nonlinearity is negligible when compared to that in the front-end integrator. Moreover, the SR can be relaxed to 350 V/μs, as their settling behaviors are not so important. Table III summarizes the specifications for the four integrators in the cascade after scaling.

VI. DESIGN OF THE BUILDING BLOCKS

A. Amplifiers

The triple tradeoff among dc gain, dynamics and output swing, always present in an amplifier [28], becomes tighter in a low-voltage implementation. We have already shown that the selection of the reference voltage and the topology of the front-end amplifier are interrelated in deep-submicron cascade ΣΔMs, the reason being that large enough V_{ref} requires two-stage amplifiers in order to achieve the dc gain and dynamic requirements. Fortunately, this is not the case for the amplifiers at the modulator back-end, whose dc gain can be largely relaxed, so that a single-stage amplifier may be enough. Therefore, in order to avoid over-sizing and optimize the power consumption, two different amplifiers have been designed: a high-dc-gain, high-speed amplifier for the first stage (OPA), and a modest dc-gain, high-speed amplifier for the third and fourth integrators (OPB).

OPA is implemented using a two-stage two-path compensated architecture, shown in Fig. 10(a). It uses a telescopic first-stage and both Miller and Ahuja compensation [34] through capacitors C_c and C_{ac}, respectively. The common-mode feedback nets (CMFB) employed in the first and second stages are dynamic, because they have no static consumption and help to circumvent voltage range problems. A p-type input scheme has been preferred, the main reason being the possibility of cancelling the body effect in the pMOS devices—one of the mechanisms for substrate noise coupling [35]. Another reason for this choice is that, in the target technology, $1/f$ noise of nMOS devices is considerably larger than that of pMOS ones. Although $1/f$ noise usually plays a secondary role in telecom converters, since it normally does not alias and the low-frequency region of the spectrum is commonly out of the signal band, the $1/f$ noise

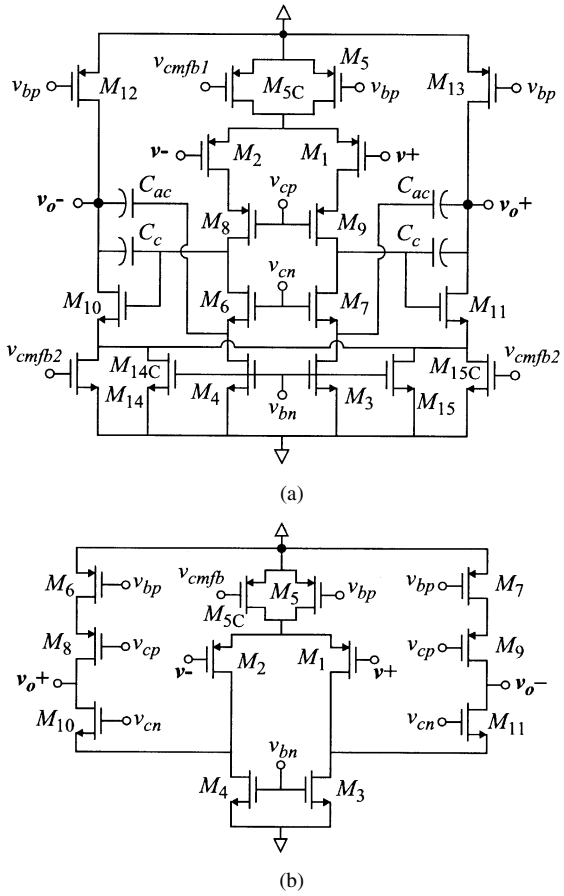


Fig. 10. (a) Two-stage amplifier (OPA). (b) Single-stage amplifier (OPB).

power spectral density (PSD) of very small devices can be huge [36] and sometimes poorly modeled, thus deserving special attention in deep-submicrometer implementations. This trend precludes using minimal length transistors, even more noticeably than if only matching considerations are taken into account. In our case, the devices contributing most to the amplifier noise are M_1, M_2, M_3, and M_4. In order to make the $1/f$ noise contribution negligible, the length of those devices was increased up to 0.5 μm for the pMOS and 2 μm for the nMOS. In the worst case, the in-band error power due to the $1/f$ noise of the front-end amplifier is –103.6 dB, low enough not to degrade the performance.

OPB is implemented using a folded-cascode architecture, shown in Fig. 10(b), which is enough to accomplish the moderate dc gain requirement with reduced power dissipation. An SC CMFB is also employed.

Table IV shows the features of OPA and OPB obtained by electrical simulation after full sizing. Results summarized correspond to the worst-case value of each parameter in a corner analysis—considering fast and slow device models, $\pm 5\%$ variation in the 2.5-V supply, and temperatures in the range $(-40\,^{\circ}\mathrm{C}, +110\,^{\circ}\mathrm{C})$.

The amplifier nonlinear features (mainly nonlinear dc gain and dynamics) deserve special attention in a low-voltage implementation. When the amplifier output voltage swings, the drain-to-source voltage of the output transistors changes, and so does the output impedance. This effect, illustrated in Fig. 11 for OPA, translates into a dependence of the open-loop dc gain on

TABLE IV
WORST-CASE ELECTRICAL SIMULATION RESULTS FOR THE AMPLIFIERS

SPECs	OPA	OPB
Open-loop DC-gain	73.5dB	56.8dB
Gain-bandwidth product (1.5-pF load)	331.5MHz	331.7MHz
Phase margin (1.5-pF load)	57.9°	67.7°
Slew rate (1.5-pF load)	883V/μs	373V/μs
Differential output swing	±1.86V	±1.72V
Input capacitance	129fF	343fF
Input equivalent noise	5.5nV/$\sqrt{\text{Hz}}$	5.1nV/$\sqrt{\text{Hz}}$
Power consumption	19.4mW	6.9mW

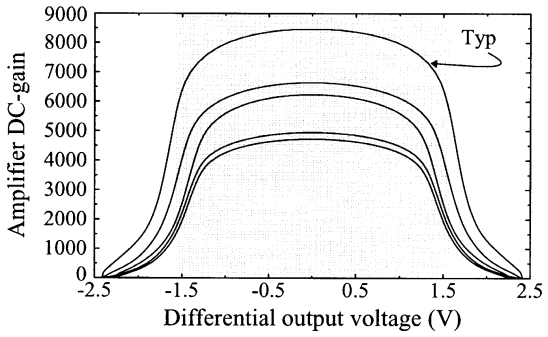


Fig. 11. DC gain nonlinearity of OPA at several process corners.

the output voltage, so that the dc gain reaches its maximum at the central point and decreases as the output approaches the rails. Such a nonlinearity is traditionally modeled by a second-order polynomial dependence of the gain on the output voltage [4], but this is only valid for small voltage excursions around the central point. On the contrary, in a 2.5-V implementation, it is expected that small-gain regions of the dc curve (shadowed areas in Fig. 11) are often visited during normal operation of the modulator. In order to accurately account for this nonlinearity in behavioral simulations, we have resorted to a table look-up procedure from amplifier dc curves obtained by electrical simulation. A similar approach has been employed for validating the actual transient response of the front-end integrator. This step is aimed at avoiding inaccuracies of the single-pole SR limited behavioral model employed [33] when applied to the two-stage amplifier with nonconstant SR in the first integrator.

B. Switches

The design of the CMOS switches has been tackled with two main considerations in mind. First, the nonzero on-resistance heavily affects the integrator dynamic, slowing down its transient response. Second, the switch on-resistance can be highly dependent on voltage in low-voltage implementations. The sampling process with such a nonlinear resistance causes dynamic distortion [29] at the $\Sigma\Delta$M front-end, the more evident the larger the signal frequency. Among the solutions to these problems, resorting to larger aspect ratios increases parasitics and power dissipation, whereas including clock-boosting [30] increases complexity and leads to a less robust design.

According to settling considerations, resistances in the range of 150 Ω can be tolerated in combination with the amplifier dynamics. In our process, such a value can be obtained using

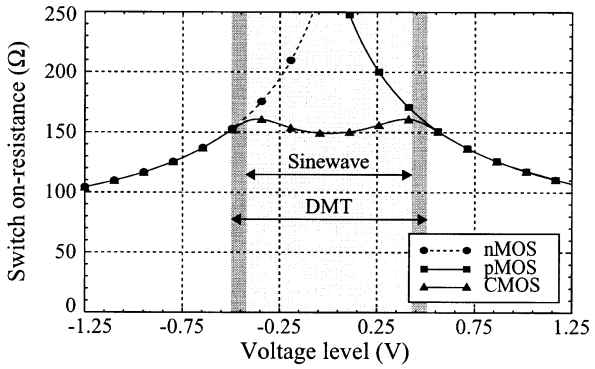


Fig. 12. Switch on-resistance versus the voltage across it.

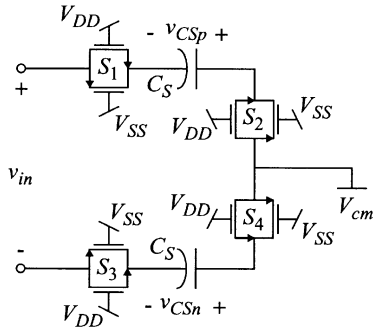


Fig. 13. Circuit for the evaluation of the distortion introduced by the switches.

standard-threshold CMOS transmission gates, with no need for clock boosters. The sizes of the pMOS and nMOS devices were selected to equalize their transconductances, keeping the resistance of the transmission gate as linear as possible. Fig. 12 shows its nominal dc characteristic.

In order to evaluate the distortion, the nonlinear sampling has been extensively simulated using the differential circuitry in Fig. 13. Note that the distortion will be mainly determined by switches S_1 and S_3 (connected to the input), whereas S_2 and S_4 are connected to the central voltage that is constant. Electrical simulations have been performed to compute the first five in-band harmonics for a 0.85-V, 366-kHz input sinewave. Also, the DMT signal in Fig. 8(a) has been considered. Fig. 14 shows the worst-case results obtained for both type of inputs during the corner analysis: The worst-case total harmonic distortion (THD) is -96 dB for the input sinewave and the maximum multitone power ratio (MTPR) [32] of the converted DMT signal is -81 dB. Both figures are small enough for our application, so that clock-boosting is not required.

C. Quantization Blocks

The resolution specifications for the comparators in the first and second stage are not very demanding: offset and hysteresis smaller than 10 and 20 mV, respectively. However, the maximum comparison time is only 3 ns—a quarter of the worst-case clock period. For this reason, the latched comparator in Fig. 15 has been adopted. It includes a differential pair input transconductor [37], which attenuates the impact of common-mode interferences, a regenerative stage, and an SR latch. In this circuit, the small voltage imbalance created across the nMOS switch controlled by ϕ_{2d} during the reset phase is rail-to-rail regenerated during the positive-feedback comparison phase. The latter starts when $\overline{\phi}_{2d}$ goes high, thus making the latch react before the integrator output changes at the beginning of ϕ_1. This strategy avoids using an extra SC stage at the comparator front-end. Differenced supply paths are used for the preamplifier and the regenerative latch in order to reduce the sensitivity to digital switching noise and supply bouncing.

The 3-b A/D/A converter in the last stage has been implemented with a flash ADC and a resistive-ladder DAC, as shown in Fig. 16 [18]. The resistive-ladder is also used to generate the voltage references of the ADC. The latter has a fully differential flash architecture, where the thermometer output code is translated into a 1-of-8 code using AND gates. For improving robustness against common-mode interferences, seven differential comparators, similar to those in the first and second stage of the cascade, form the ADC front-end, each of them with two input pairs to perform the subtraction of the two differential signals being compared. Apart from this, the only difference with those in the first- and second-stage comparators is that the input transistors have been reduced in size in order to decrease the capacitive load of the fourth integrator.

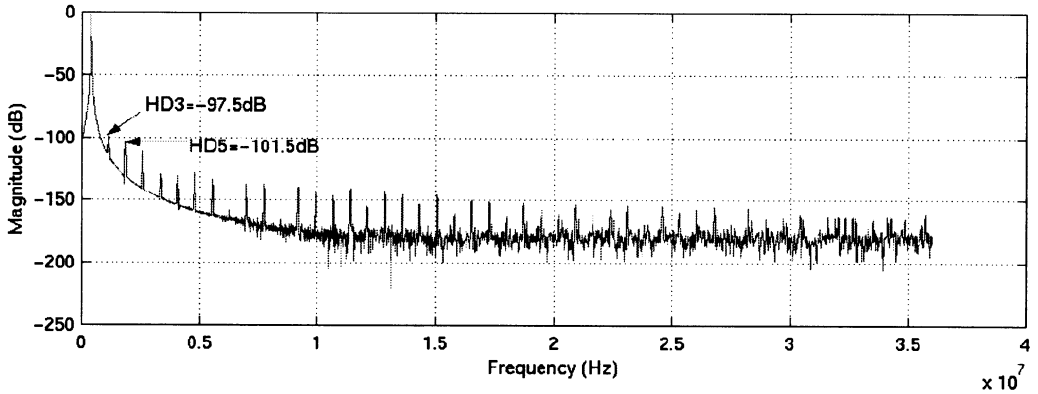
The DAC consists of 14 segments of 50-Ω poly resistors, the most important source of INL being resistor mismatch, which improves with device area. Thus, in order to guarantee that INL $\leq 0.5\%$FS, each of the 50-Ω resistors is obtained by connecting larger devices in parallel.

D. Auxiliary Blocks

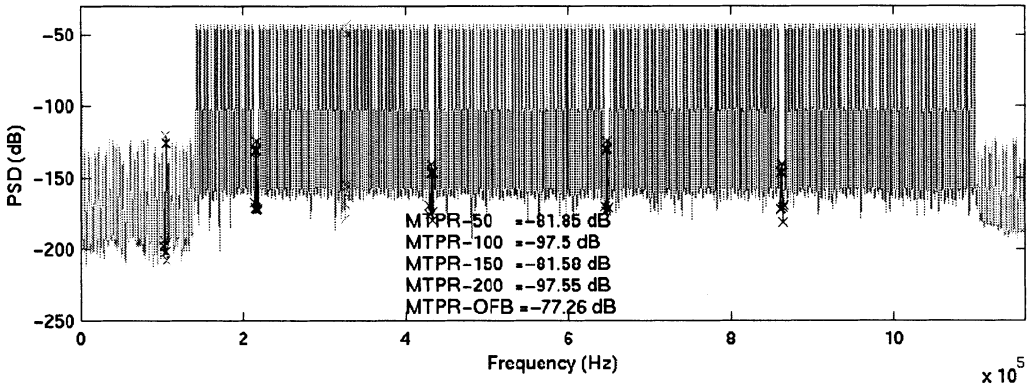
Fig. 17 shows the clock driver that generates the nonoverlapped clock phases—ϕ_1, ϕ_2—from an external clock signal. Delayed versions of the phases—ϕ_{1d}, ϕ_{2d}—are also generated to avoid signal-dependent clock-feedthrough. As shown in Fig. 7, the delay is incorporated only to the turn-off of the switches (falling edges of the signals) in order to increase the time slot available for sampling and integration [15]. Complementary versions of the phases are also generated to control the CMOS switches. All signals are properly driven at the output using a buffer tree that equalizes the differences in capacitive load from phase to phase. After ensuring reliable nonoverlapping time and phase delay, the worst-case effective phase eye is 6 ns, which means that approximately 85% of the clock period is left for the modulator operation.

The reference voltages required for the modulator operation, namely $V_r^+ = 2.0$ V and $V_r^- = 0.5$ V, together with the central voltage V_{cm} are on-chip generated by the circuit shown in Fig. 18. Its main design considerations are fast settling and that the output impedance of the V_r^+ and V_r^- lines must be low enough to avoid dynamic distortion at the integrators [38]. In our case, 7-Ω maximum output impedance is obtained along the signal band through the combined use of an on-chip resistive amplifier and two big external capacitors. An extra external capacitor is connected between the reference voltages, valued according to the $(\text{pad} + \text{wire} + \text{lead} + \text{pin})$ parasitics, so that the spurious components around half the sampling frequency are removed from the differential reference voltage.

A second-order passive antialiasing filter is also included on-chip. Its bandwidth can be programmed to accomplish

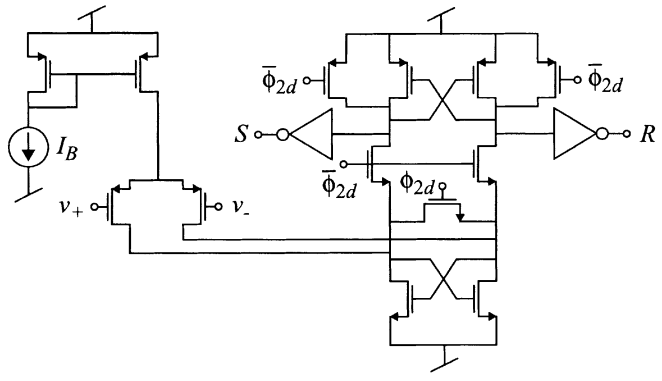


(a)

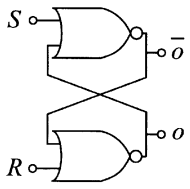


(b)

Fig. 14. Worst-case dynamic distortion introduced by the switch for a (a) 0.85-V, 366-kHz sinewave input signal and (b) −15-dB DMT input signal.



(a)



(b)

Fig. 15. Comparator. (a) Preamplifier and regenerative latch. (b) SR latch.

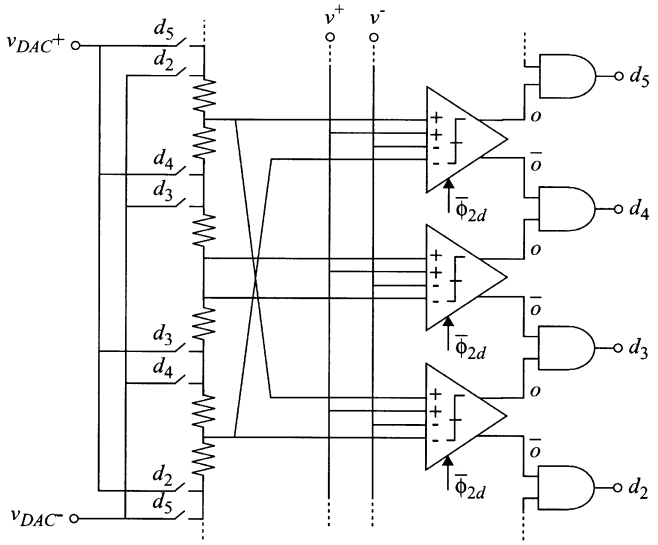


Fig. 16. Partial view of the A/D/A converter.

either ADSL (up to 1.1 MHz) or ADSL+ (up to 2.2 MHz) band requirements.

VII. Experimental Results

Fig. 19 shows a microphotograph of the modulator and auxiliary blocks fabricated in a 0.25-μm CMOS process. It occupies 2.78 mm^2 and dissipates 65.8 mW (55 mW corresponding to the $\Sigma\Delta$M itself) from a 2.5-V supply. Apart from the modulator described here, other blocks pertaining to the final application (not shown) were included in the prototype chip, among them a phase-locked loop (PLL) and a decimation filter. These blocks were arranged so that the $\Sigma\Delta$M could be tested as a stand-alone block or in combination with the PLL and the digital filter. The latter configuration is aimed at reducing the switching activity of the digital buffers at the pad-pin level—a major

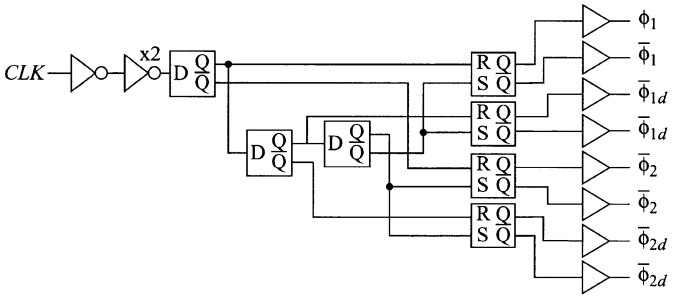


Fig. 17. Clock phase generator and drivers.

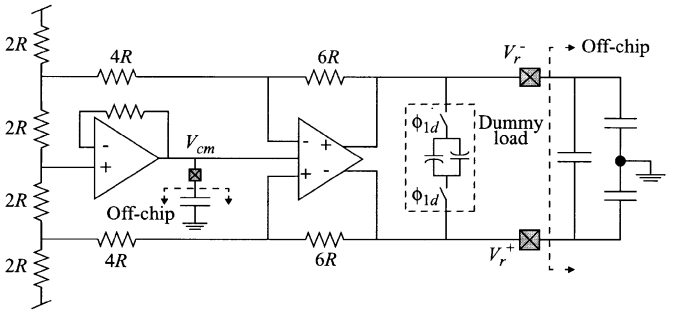


Fig. 18. Reference voltage generator.

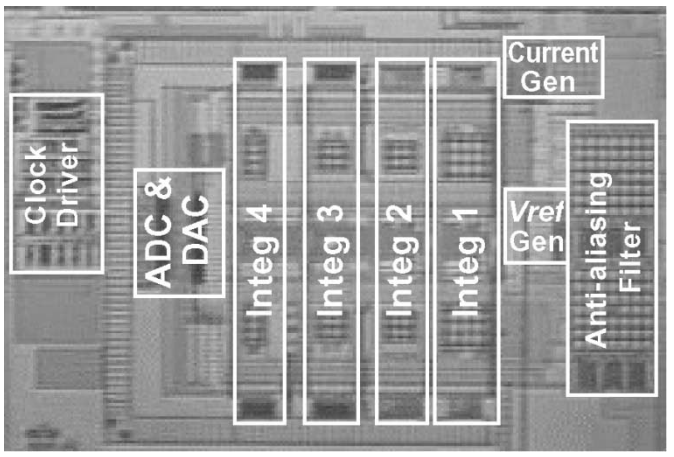


Fig. 19. Microphotograph of the ΣΔM in 0.25-μm CMOS.

source of performance degradation. Also, with the objective of attenuating the impact of switching noise, the following mixed-signal recipes, valid for nonepi high-ohmic substrates [35], were adopted in the prototype: 1) increased distance among analog and digital blocks; 2) use of separate analog, mixed, and digital supplies, which are distributed on-chip through distinguished low-impedance paths; 3) placement of guard-rings (with dedicated pads and pins) surrounding the different chip sections, in order to avoid spreading of switching noise and provide a quiet substrate for the sensitive analog blocks; 4) preserved layout symmetry and extensive use of common-centroid techniques aimed at gaining insensitivity to common-mode interferences; 5) shielding of the clock buses along the chip in order to reduce cross-talk and provide a low-

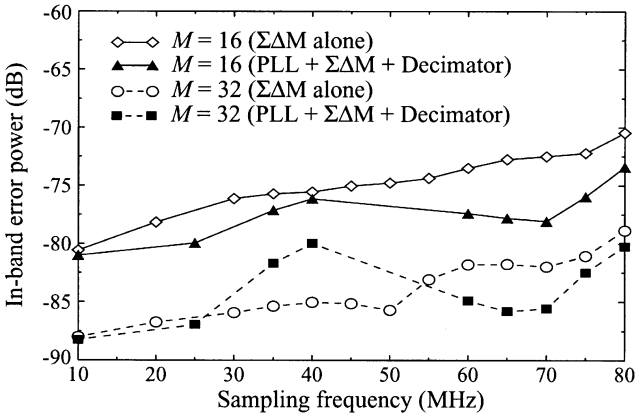


Fig. 20. In-band error power as a function of the modulator sampling frequency.

impedance return path; 6) extensive use of on-chip decoupling, including a mixed on/off-chip decoupling scheme for the analog supply [39]; and 7) multiple bonding for reducing wiring inductance.

In order to avoid socket parasitics, each prototype sample was mounted onto a dedicated four-layer printed circuit board (PCB), including typical measures for signal integrity, such as separate analog, mixed, and digital ground planes, intensive decoupling and filtering, and proper impedance termination [40]. The input signal was provided by a high-resolution, −100 dB THD, sinusoidal source with floating differential output, its common-mode voltage referenced to the on-chip generated central voltage V_{cm}. The output samples, either from the modulator bitstreams or from the digital filter, were acquired by a digital tester that also provided the master clock stimulus and the supply voltages.

Fig. 20 shows the total in-band error power versus the modulator sampling frequency, for the nominal oversampling ratio $(M = 16)$ and twice this value. For each value of M two curves are plotted, corresponding to clock-rate acquired (ΣΔM alone) output samples and decimated (PLL + ΣΔM + Decimator) output samples. Note that in the former case the in-band error power increases as the sampling frequency increases. This effect, explained by the increasing switching noise injected by the I/O buffers, causes a degradation of around 9 dB in performance at the nominal sampling frequency (70.4 MHz). Nevertheless, when both the PLL and decimator are used, so that the switching frequency of input and output buffers are divided by 4 and 16, respectively, the loss of performance is reduced to 3 dB. Note also that although the digital filter activity generates an increase of the in-band error power at intermediate sampling frequencies, its impact is largely suppressed at the nominal rate, thus demonstrating the validity of the decoupling schemes used, especially at the reference voltages. A similar behavior is obtained for $M = 32$.

Fig. 21 shows a 16 384-point fast Fourier transform (FFT) of the decimated converter output for a 0.5-V, 160-kHz input sinewave. Despite the large signal level, no significant harmonic distortion is observed. In fact, in Fig. 21, spurious-free dynamic range (SFDR) is 90 dB, whereas THD computed up to the fifth

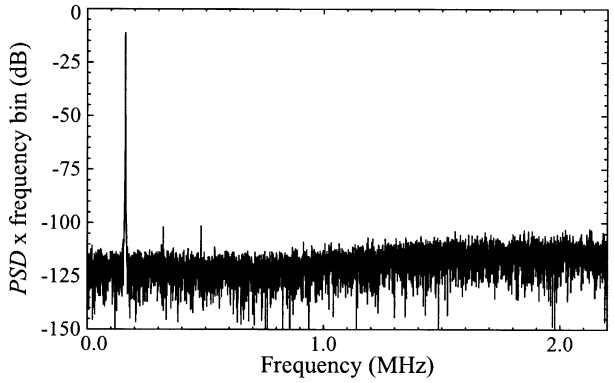


Fig. 21. Output spectrum for a 0.5-V, 160-kHz input sinewave at nominal sampling frequency.

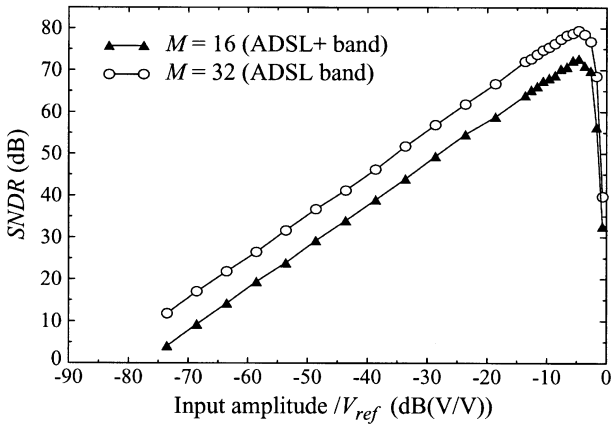


Fig. 22. SNDR as a function of the input level.

harmonic is -87 dB, so that the signal-to-noise ratio (SNR) almost coincides with the SNDR. The latter is shown in Fig. 22 for both $M = 16$ and $M = 32$, the error power being computed in the ADSL + band (from 30 kHz to 2.2 MHz) and in the ADSL band (from 30 kHz to 1.1 MHz), respectively. The dynamic range is 78 dB (12.7 b) for $M = 16$ and 85 dB (13.8 b) for $M = 32$, with SNDR peaks of 72.7 dB and 80 dB, respectively.

The good linearity of the converter also manifests as low integral and differential nonlinearity (INL and DNL, respectively). Both curves are shown in Fig. 23. They have been obtained applying the code-histogram method [41] to 89 output data records, each one containing 8192 consecutive output samples for a 0.8-V, 59.62-kHz input sinewave. The only difference among the data records is the phase of the sinewave, which can not be controlled. However, this fact helps to hit the converter output codes in a more uniform way, thus requiring fewer samples than in the case in which all were taken consecutively. The INL, DNL units in Fig. 23 are LSBs of 14 b in a ± 0.8-V full scale, i.e., 1 LSB $= (2.08)/(2^{14} - 1) = 9.77\ \mu$V. The measured INL and DNL are within ± 0.85 and ± 0.80 $\text{LSB}_{14\,\text{b}}$, respectively. These low values are obtained thanks to the use of pseudomultibit quantization (with no need of correction/calibration of the DAC nonlinearity) and a careful control of the distortion introduced by the front-end amplifier and switches.

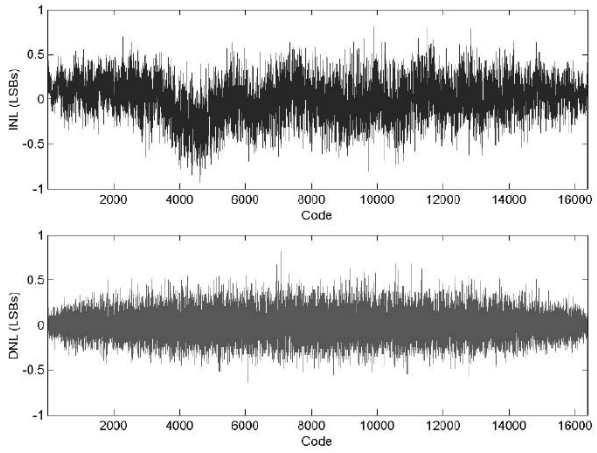


Fig. 23. Measured INL and DNL. Vertical-axis units are LSBs of 14 b.

TABLE V
STATE OF THE ART $\Sigma\Delta$Ms WITH DOR $\geq$ 1MS/s

REF	*DOR* (MS/s)	*ENOB* (bit) (from *DR*)	Process	Supply (V)	Power (mW)	*FOM* (pJ)
[5]	4	11.3	0.18µm Digital	1.8	3.3	0.33
[6]	4	15.0	0.5µm Analog	2.5	150	1.14
[7]	2.5	15.0	0.5µm Analog	5	105	1.28
[8]	1	13.0	0.35µm BiCMOS	2.7	11.88	1.45
[9]	2.5	15.8	0.65µm Analog	5	295	2.07
ΣΔM here *M* = 32	2.2	13.8	0.25µm M-i-M	2.5	65.8	2.10
ΣΔM here *M* = 16	4.4	12.7	0.25µm M-i-M	2.5	65.8	2.25
[10]	2.2	15.0	0.18µm dual	3.3	180	2.50
[14]	2.2	15.0	0.5µm Analog	3.3	200	2.77
[12]	2.2	13.0	0.7µm Analog	5	55	3.05
[13]	1.25	12.83	0.18µm dual	2.7	30	3.29
[11]	1.5625	13.0	0.35µm Analog	2.5	50	3.91
[13]	3.84	11.67	0.18µm dual	2.7	50	4.00
[15]	2	14.80	1µm Analog	5	230	4.03
[16]	2.2	14.0	0.35µm Analog	3.3	150	4.16
[17]	2.2	13.0	0.35µm Digital	3.3	78.2	4.34
[18]	2.1	12.0	1µm Digital	5	41	4.77
[16]	2.2	13.0	0.35µm Analog	3.3	99	5.49
[21]	1.25	13.7	0.25µm M-i-M	2.5	100	6.01
[21]	2	13.0	0.25µm M-i-M	2.5	105	6.41
[20]	1.4	13.0	0.7µm Analog	3.3	81	7.06
[9]	12.5	12.0	0.65µm Analog	5	380	7.42
[19]	2.5	14.5	0.6µm Analog	5	550	9.49

As a matter of conclusion, the $\Sigma\Delta$M here has been compared with other recently reported designs featuring DOR $\geq$ 1 MS/s, whose performances are summarized in Table V. Their effective resolution (ENOB) and FOM value, defined in (8), have been plotted as a function of DOR in Fig. 24(a) and (b), respectively. In spite of the performance loss due to switching noise (around half a bit), the modulator here achieves one of the lowest FOM reported so far. In particular, the FOMs obtained are surpassed by only two CMOS designs with supply voltage equal to or below 2.5 V [5], [6].

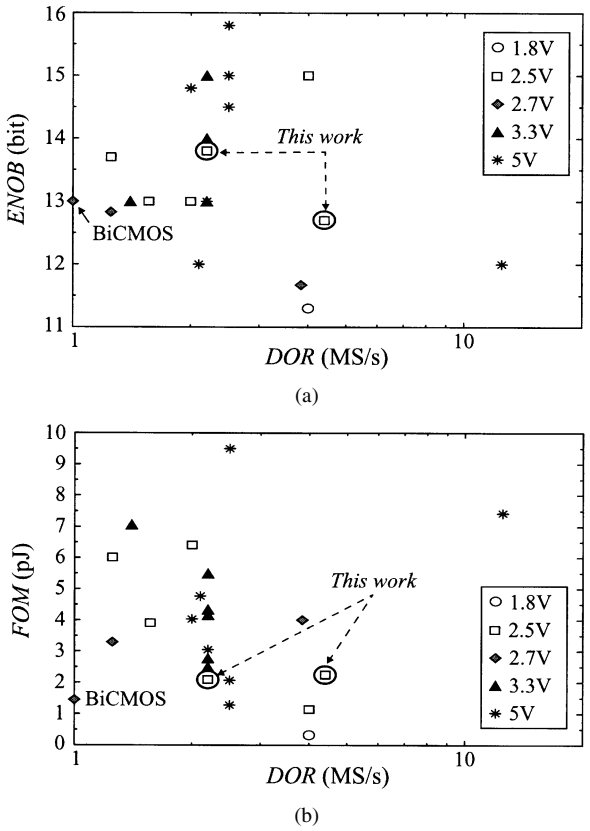


Fig. 24. State-of-the-art high-frequency ΣΔMs in the (a) ENOB–DOR plane and (b) FOM–DOR plane.

APPENDIX
POWER ESTIMATOR FOR CASCADE ΣΔMS

In the presence of circuit imperfections, the dynamic range of a ΣΔM can be roughly expressed as follows [4]:

$$\mathrm{DR} = 3 \cdot 2^{2\mathrm{ENOB}-1} \cong \frac{\frac{V_{\mathrm{ref}}^2}{2}}{P_Q + P_{\mathrm{Th}} + P_{St}} \tag{11}$$

where P_Q, P_{Th}, and P_{St} are the in-band powers of quantization error, white circuit noise or thermal noise, and incomplete settling error, respectively.

For the sake of simplicity, we will assume for now that the incomplete settling error can be controlled by design so that $P_{St} \ll P_Q$, P_{Th}. An approximate expression for P_Q is obtained by adding up (4) and (6). Concerning P_{Th}, it will be usually dominated by white noise injected by the switches and the front-end amplifier, whose PSD is folded back over the baseband by undersampling. A conservative expression for the in-band power of white noise can be derived [3] as

$$P_{\mathrm{Th}} \cong \frac{16kT}{3MC_S} \tag{12}$$

where C_S is the value of the sampling capacitor.

Equations (4)–(7) and (12) show that the dynamic range of a cascade ΣΔM can be roughly expressed as a function of the following design parameters: V_{supply}, L, M, C_S, A_v, and σ_C, to which we have to add B and INL if the last-stage quantizer is multibit. So, for given values of A_v, σ_C, and INL, the minimum value of the capacitor C_S required to obtain a given DR can be obtained as a function of M, L, and B. Once C_S is known, the equivalent load for the amplifier in the integrator can be estimated as [33]

$$C_{\mathrm{eq}} \cong C_S + C_p + C_l\left(1 + \frac{C_S + C_p}{C_o}\right) \tag{13}$$

where C_o, the integrator feedback capacitance, is related to C_S through the integrator weight, $C_o = C_S/g_i$, and C_p and C_l stand for the integrator summing node and output parasitics, respetively. Estimating the latter two capacitances is a difficult task because of their extreme dependence on the actual amplifier design.

Usually, the main contribution to C_p is the amplifier input parasitics. In a fully differential topology, this is formed by the input transistor gate-to-source capacitance C_{gs} (both channel and overlap contributions) and its overlap gate-to-drain capacitance $C_{\mathrm{gd}}^{\mathrm{ov}}$ amplified by Miller effect [28]. Thus, neglecting C_{gb}, we have

$$\begin{aligned} C_p &\cong C_{\mathrm{gs}}^{\mathrm{ch}} + C_{\mathrm{gs}}^{\mathrm{ov}} + C_{\mathrm{gd}}^{\mathrm{ov}}(1 + A_{v_1}) \\ &= \frac{2}{3}C'_{ox}W_{in}L_{in} + C'_{\mathrm{ox}}W_{\mathrm{in}}\Delta L_{\mathrm{in}}(A_{v_1} + 2) \end{aligned} \tag{14}$$

where C'_{ox} is the gate oxide capacitance density and ΔL_{in} stands for the lateral diffusion of drain/source regions below the gate, both technology-dependent parameters. Apart from the input transistor dimensions (W_{in}, L_{in}), the other unknown variable in (14) is its input-to-output gain A_v. This is equal to the complete amplifier gain for single-stage amplifiers or to the first-stage gain if multistage topologies are used. It can even be around unity if cascode devices are used, such as in folded- or telescope-cascode amplifiers [28]. Now, making use of the well-known (as much as inadequate) square-low expression for the input transistor drain current, we have

$$C_p = \frac{2L_{\mathrm{in}}I_{D,\mathrm{in}}}{\mu V_{\mathrm{OVD}}^2}\left[\frac{2}{3}L_{\mathrm{in}} + \Delta L_{\mathrm{in}}(A_{v_1} + 2)\right] \tag{15}$$

where $V_{\mathrm{OVD}} \equiv V_{\mathrm{GS}} - V_T$ is the input transistor overdrive voltage.

The other unknown capacitance in (13), C_l, has two main contributions: The first one is due to the bottom parasitic of the integration capacitor C_o, and the second one is due to the amplifier itself. The former contribution can vary a lot, depending on the type of capacitors. With modern M-i-M structures it turns out to be very small, ranging from less than 1% to 5% of C_o. Because of this, C_l tends to be dominated by the amplifier output parasitic load, which strongly depends on the actual output devices and, overall, on the amplifier topology. Even the supply voltage, via output swing and dc gain requirements, makes an impact on the transistor sizes and hence on C_l. For a given amplifier schematic, the latter influence makes C_l slightly increase under technology scaling and shrinking supply voltages, because wider output devices are required to accommodate similar output swings. All things considered, a reliable estimation of this capacitance prior to sizing the amplifier is not possible. Based on previous design experiences, we will assume a constant value equal to 2.5 pF.

Returning to the settling error power P_{St}, an accurate estimation would involve the following calculations. For example, just for a single-pole amplifier model, complicate expressions are derived [4] if a nonlinear (SR limited) settling is considered.

Further complexity arises from considering both sampling and integration incomplete charge transference and the contribution of the nonzero switch on-resistance [33]. Hence, we will simplify our treatment assuming that the slew-rate of the amplifier is large enough and the switch on-resistance small enough to neglect their impact on the integrator transient response, so that the settling is linear with time constant equal to $C_{\rm eq}/g_m$. This being the case, it takes a number $\ln(2^{\rm ENOB})$ of time constants to settle within ENOB resolution, that is, the following relation should be fulfilled:

$$\ln\left[2^{(\rm ENOB+1)}\right]\frac{C_{\rm eq}}{g_m} \leq \frac{T_S}{2} \tag{16}$$

where T_S is the sampling period. Note that we have added an extra bit in order to make room for the inaccuracy of this simplified model. The above expression can be used to estimate the minimum value of the transconductance parameter as

$$g_m = 2f_S \ln[2^{(\rm ENOB+1)}]C_{\rm eq} \tag{17}$$

where $f_S \equiv 1/T_S$ is the sampling frequency. This is the transconductance required for a single-stage amplifier with equivalent output load $C_{\rm eq}$. For multistage amplifiers, the previous relation must be carefully tackled because both parameters, total transconductance and equivalent output load, lose control of the dynamics. However, provided that the main pole of the amplifier is set by the input stage and an eventual inter-stage compensation capacitor, (17) can still be used to determine the input stage transconductance, that is related to the input transistor current as follows:

$$g_m = \frac{2I_{D,\rm in}}{V_{\rm OVD}}. \tag{18}$$

Equations (13), (15), (17), and (18) can be handled in an iterative way to determine the current required through the input transistors of the amplifier, whose actual topology sets the power consumption. Whenever possible, a single-stage amplifier should be used for its better performance/power figure. However, as technologies scale down and supply voltages shrink, two-stage amplifiers are gaining ground. Moreover, in practice, two gain stages are not enough to achieve the overall gain requirement, so that the first one often includes cascode devices in a telescope cascode configuration. Let us consider this topology as an archetype in modern deep-submicrometer technologies. The current through the first stage has been already estimated as $2I_{D,\rm in}$. Assuming for the sake of simplicity a fixed ratio $\eta_{\rm io}$ between the currents flowing through the input and output branches, the total current through the amplifier can be estimated as

$$I_B \cong 2I_{D,\rm in} + 2\eta_{\rm io}I_{D,\rm in} + I_{D,\rm in} = [2(1+\eta_{\rm io})+1]I_{D,\rm in} \tag{19}$$

where an extra $I_{D,\rm in}$ is added to account for the biasing stage.

With (19), the power dissipation of the first amplifier can be estimated. That of the remaining amplifiers in the cascade stages can be decreased, following the scaling rule commonly applied to the amplifier requirements in $\Sigma\Delta$Ms. This power reduction may come from either a relaxed set of specifications or the subsequent amplifier topology simplification. Sometimes, even when a two-stage amplifier may be required for the first integrator, it is possible to use a single-stage topology for the rest of integrators. So, we can write

$$I_{B,\rm total} = I_B\left(1+\sum_{i=2}^{L}\chi_i\right) \tag{20}$$

where χ_i is the ratio of the current absorption of the ith amplifier to the first one. From this, the static power dissipated in amplifiers is

$$P_{\rm op,sta} = I_B V_{\rm supply}\left(1+\sum_{i=2}^{L}\chi_i\right). \tag{21}$$

Besides this static consumption, which usually accounts for 80% of the total power, there are other contributing blocks, namely:

- $L-1$ latched comparators used as single-bit quantizers and those in the last-stage multibit quantizer, usually implemented by a flash ADC, i.e., (2^B-1) more latches. This consumption must include the static power dissipated in a convenient preamplifying stage.
- Last-stage multibit DAC (if $B>1$). The relaxed requirements for this block allows us to implemented it with a resistor ladder. Its main design considerations are resistor matching and linearity (both causing INL) and the fact that it must drive enough current to provide a good settling. The current requirement scales with the sampling frequency and the capacitive load involved. The latter can be considered almost constant because the last-stage capacitors should be set to the minimum required to achieve certain level of matching (thermal noise playing a secondary role). So, we can empirically write

$$P_{\rm DAC} \cong V_{\rm supply}I_{\rm DAC,ref} \times \frac{f_S}{f_{S,\rm ref}} \tag{22}$$

  where $I_{\rm DAC,ref}$ is the current through the DAC required for operating at a certain frequency of reference $f_{S,\rm ref}$.
- Dynamic power in SC stages. The dynamic power dissipated to switch a capacitance C_u between the reference voltages at a frequency f_S can be estimated as $C_u f_S V_{\rm ref}^2$, which tends to increase in high-speed, high-resolution converters. Its actual value depends on the integrator weights used. In our case, the following expression provides a good estimate:

$$P_{\rm SC} = 2\times[5C_{u_1}+4(L-1)C_{u_2}]f_S V_{\rm ref}^2 \tag{23}$$

  where the factor 2 comes from the differential implementation, C_{u_1} is the unitary capacitor in the first integrator, whereas C_{u_2} is the one in the rest of integrators, usually smaller than C_{u_1}.
- Small digital blocks: flip-flops, gates, cancellation logic, etc. Apart from being small, they do not make any difference for the architectures considered and will be neglected here. Of course, this does not apply to the decimation filter, whose power consumption is comparable to that of the $\Sigma\Delta$M. Moreover, since the order of the digital filter must equal $L+1$, high-order $\Sigma\Delta$Ms require more complex filters than low-order ones. However, an increase of the modulator order entails a decrease of the oversampling ratio and the filter can be operated at a lower frequency,

dissipating less power. To our purpose, we can consider an essentially constant decimation filter power consumption.

By adding up all the contributions, the power dissipation of the ΣΔM can be estimated as

$$\text{Power} \cong P_{\text{op,sta}} + P_{\text{DAC}} + \left[(L-1) + (2^B - 1)\right] P_{\text{comp}} + P_{\text{SC}}. \quad (24)$$

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