Design Issues and Experimental Characterization of a Continuously-Tuned Adaptive CMOS LNA

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***Abstract*—This paper presents the design implementation and experimental characterization of an adaptive Low Noise Amplifier (LNA) intended for multi-standard Radio Frequency (RF) wireless transceivers. The circuit —fabricated in a 90-nm CMOS technology— is a two-stage inductively degenerated common-source topology that combines PMOS varactors with programmable load to make the operation of the circuit continuously tunable. Practical design issues are analyzed, considering the effect of circuit parasitics associated to the chip package and integrated inductors, capacitors and varactors. Experimental measurements show a continuous tuning of NF and S-parameters within the 1.75-2.23GHz band, featuring NF<3.7dB, S_{21} >19.6dB and IIP3> −9.8dBm, with a power dissipation < 23mW from a 1-V supply voltage.** [1]

I. Introduction

The integration of increasingly complex Radio Frequency (RF) front-end circuits into mainstream nanometer CMOS technologies imposes a number of challenges and trade-offs that makes their design a key issue to guarantee the quality of service of the resulting wireless hand-held terminals. Among other RF building blocks, the design of the Low Noise Amplifier (LNA) is particularly critical due to its early position at the very beginning of the receiver chain, what makes this circuit a limiting factor in the overall system performance [1].

The difficulty of designing nanometer CMOS LNAs is aggravated in the case of multi-standard applications, in which these circuits must operate over different frequency ranges, whereas keeping reduced number of passive circuit elements to increase integration [2]. As a consequence, most reported multi-standard LNAs increase the number of integrated passive elements (basically capacitors and inductors) as compared to their mono-standard counterparts [3]–[5]. Therefore, the silicon area – mainly occupied by those elements – is not clearly reduced as compared to using switchable mono-standard LNAs [6].

The work in this paper contributes to this topic and presents the practical implementation and experimental measurements of a continuously reconfigurable CMOS LNA. The circuit adapts its performance to the requirements of different standards without increasing the number of inductors as compared to a typical mono-standard LNA. It employs a two-stage topology with programmable load to separately control the input impedance, Noise Figure (NF) and signal gain. A PMOS-varactor based tuning network is used in both stages in order to make the resonance frequency continuously programmable without penalizing the LNA noise performance. Experimental measurements demonstrate a correct operation of the circuit.

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II. LNA topology and circuit Analysis

Fig. 1 shows the complete schematic of the proposed LNA, which consists of a two-stage topology with separate tuning networks. The input stage is an inductively degenerated common-source structure — using bonding inductor L_s — to provide a specified real part for the input impedance and signal gain at a given frequency. Programmable biasing is used to separately control the real part of the load of both stages, implemented by transistors $\mathrm{M_{pNF2}}$ and $\mathrm{M_{pGAIN2}}$. In this way, NF and forward gain, S_{21} , can be individually controlled by diode-connected transistors $\mathrm{M_{pNF1}}$ and $\mathrm{M_{pGAIN1}}$, respectively. Thus, the drain current of these transistors, I_{bNF} and I_{bGAIN}, are adapted to properly biasing the gate of $\mathrm{M_{pNF2}}$ and $\mathrm{M_{pGAIN2}}$, with reduced power dissipation.

The noise factor (F) and input impedance, Z_{in}, of the LNA are approximately given by [1]:

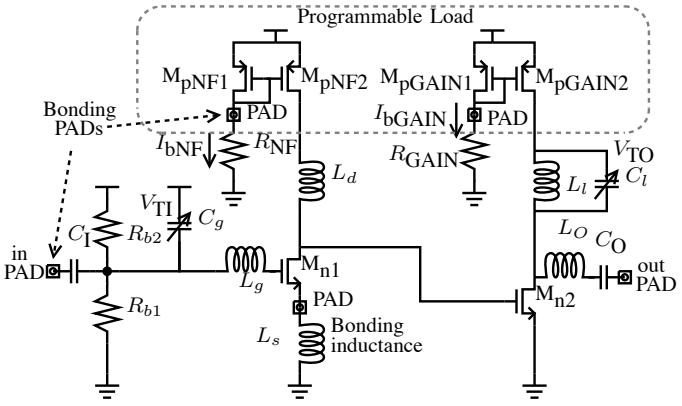


Fig. 1. Schematic of the proposed adaptive LNA.

$$\mathrm{F} \simeq 1 + \left(\frac{\omega_0 \gamma}{\omega_T \alpha Q}\right)\left[1 - 2|c|Q\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \left(\frac{\delta\alpha^2}{5\gamma}\right)\left(1+Q^2\right)\right] \quad (1)$$

$$Z_{\mathrm{in}} \simeq \frac{C_{\mathrm{I}} + C_{gsn1}}{sC_{\mathrm{I}}C_{gsn1}} + s(L_g + L_s) + \omega_T L_s\left[1 - s\omega_T L_s C_g\right] \quad (2)$$

where

$$\begin{aligned} \alpha &\simeq \frac{g_{mn1}}{g_{dsn1}} \quad Q \simeq \frac{\omega_T}{\omega_0 R_{RF} g_{mn1}} \\ \omega_0 &\simeq \frac{1}{\sqrt{C_{gsn1}(L_g + L_s)}} \quad \omega_T \simeq \frac{g_{mn1}}{C_{gsn1}} \end{aligned} \quad (3)$$

with c being the correlation factor; δ and γ are technology parameters; R_{RF} is the RF source resistance; g_{dsn1}, g_{mn1} and C_{gsn1} are respectively the small-signal drain-source conductance, transconductance and gate-source capacitance of $\mathrm{M_{n1}}$.

The tuning mechanism of the LNA is achieved by varying the resonance frequencies of the passive input- and output-tuning networks, respectively given by:

$$w_{\mathrm{in}} \simeq \frac{1}{\sqrt{C_{gsn1}\left[L_g + L_s - \left(\omega_T L_s\right)^2 C_g\right]}} \quad (4)$$

$$w_{\mathrm{out}} \simeq \frac{1}{\sqrt{L_l C_l}} \quad (5)$$

where C_g and C_l are implemented by accumulation PMOS varactors.

III. Practical Design Issues

The above analysis assumed ideal circuit elements, particularly varactors and inductors. In practice, circuit parasitics cause these elements to behave as RLC filters that may severely degrade the performance of the LNA [1]. This is specially important in the case of reconfigurable/adaptive RF circuits like the one reported in this paper, because of the many different specifications to be covered by the same circuit.

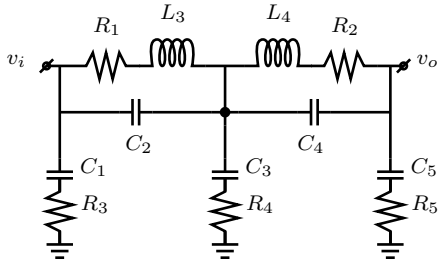
A. Analysis of Circuit Parasitics

In order to evaluate the impact of circuit parasitics, main figures were analyzed replacing every inductor and varactor with the equivalent circuit shown in Fig. 2 [1]. As a result, a more realistic expression for the input impedance is found,

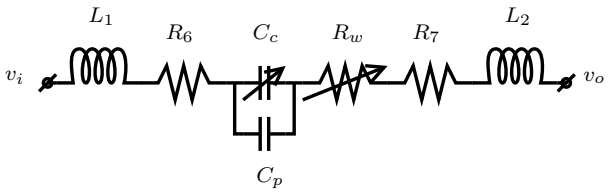
$$Z_{\mathrm{in}} \simeq \frac{Z_{Cg} Z_{3lg}}{Z_{ib}} + \frac{Z_{3lg}(sC_{\mathrm{I}} Z_{Cg} + 1) + Z_{Cg}}{Z_{2lg} sC_{\mathrm{I}}} \quad (6)$$

where

$$\begin{aligned} Z_{ib} &\simeq \frac{1}{sC_{gsn1}} + (\omega_T + 1)sL_s \\ Z_{2lg} &\simeq R_{5g} + \frac{1}{sC_{5g}} \quad Z_{Cg} \simeq 2R_{7g} + \frac{1}{s(C_{cg} + C_{pg})} \\ Z_{3lg} &\simeq \frac{R_{1g} + sL_{3g}}{1 + sC_{2g}(R_{1g} + sL_{3g})} \end{aligned} \quad (7)$$



(a)



(b)

Fig. 2. Equivalent RLC circuit for (a) inductors and (b) varactors.

Replacing the inductors and varactors in Fig. 1 with the circuits shown in Fig. 2, the expression of S_{21} results in:

$$\begin{aligned} S_{21} \simeq &\left(\frac{4g_{mn1} Z_{2lg} Z_{1ld} Z_{Cg}}{sL_s g_{mn1} Z_{1ld}^2 + s^2 C_{gsn2} L_s Z_{1ld} Z_{Cg}}\right) \cdot \\ &\left(\frac{g_{mn2} R_L Z_{1lo} Z_{2ll} Z_{Cl}}{2Z_{1lo}^2 Z_{2ll} Z_{Cl} + Z_{2ll}(R_L + Z_{Cg})}\right) \end{aligned} \quad (8)$$

where

$$\begin{aligned} Z_{1ld} &\simeq R_{3d} + \frac{1}{sC_{1d}} \quad Z_{1lo} \simeq R_{3o} + \frac{1}{sC_{1o}} \\ Z_{2ll} &\simeq R_{5l} + \frac{1}{sC_{5l}} \quad Z_{Cl} \simeq 2R_{7l} + \frac{1}{s(C_{cl} + C_{pl})} \end{aligned} \quad (9)$$

R_L is the load resistance; g_{mn2} and C_{gsn2} are respectively the small-signal transconductance and gate-source capacitance of $\mathrm{M_{n2}}$.

B. Chip package parasitics

The above expressions have been used in combination with electrical simulations using Cadence SpectreRF to design the LNA. For that purpose, the circuit in Fig. 3 was used. This circuit includes the package and the external components to be included in the PCB. A 4mmx4mm 12-pin QFN plastic package has been used. This package has been modeled using Cadence PKG tool in order to take into account their associated parasitics during the design process.

IV. Experimental Results

The LNA has been designed to fulfill the requirements of a multi-standard wireless direct-conversion receiver considering a continuously-tuned operating frequency within the 1.75-2.23 GHz band. The circuit was implemented using a 90-nm CMOS technology with a single 1-V supply voltage. Fig. 4(a) shows a microphotograph of the chip highlighting their main parts,

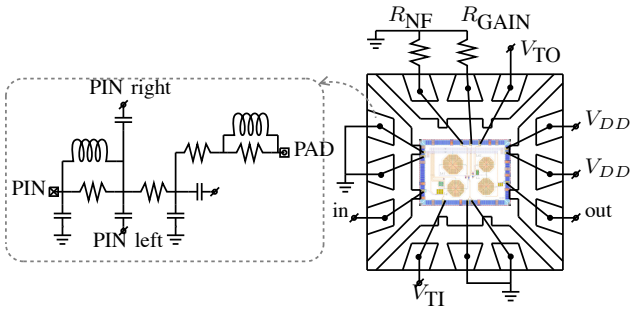


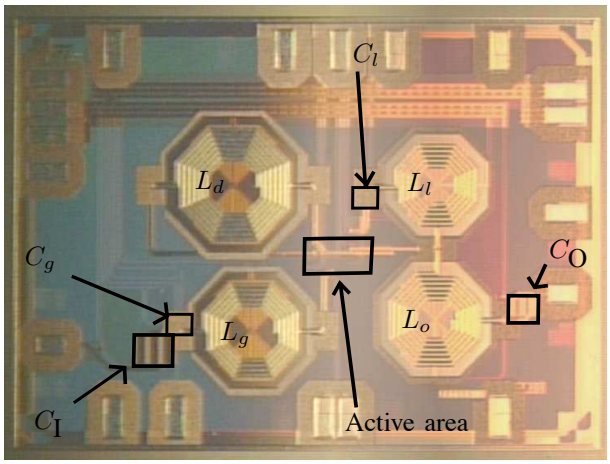
Fig. 3. Equivalent circuit of the chip package.

namely integrated inductors, capacitors, PMOS varactors and CMOS active area. Integrated inductors have octagonal shape with a patterned ground shield. Input/output capacitors are implemented by M-O-M structures, which are based on the combination of stacked and finger metal-metal capacitors. All pads are Electrostatic Discharged (ESD) protected. The die area, including pads, is 1.8 mm^2, with the core occupying 1.0 mm^2. As usual, a significant portion of this area is used by integrated inductors. However, in this circuit, and contrary to most reported multi-standard LNAs, the number of inductors is not increased as compared to the mono-standard case, with the subsequent area saving. The chip has been tested using the PCB shown in Fig. 4(b), that includes the necessary filtering for biasing and power supplies as well as off-chip resistors and connectors for the instruments.

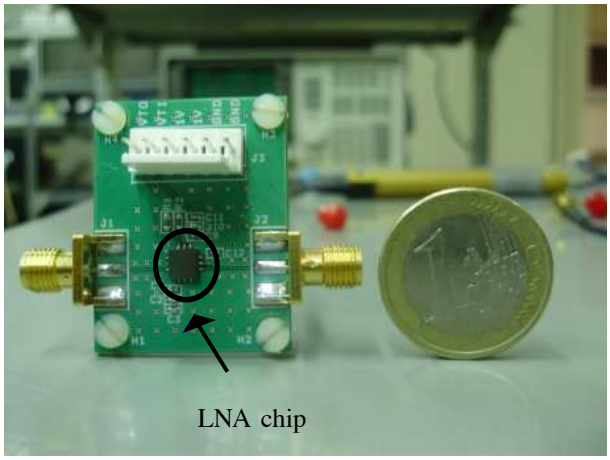
Fig. 5 shows the measured NF vs. input frequency corresponding to different values of tuned frequencies, demonstrating the reconfigurability capability of the proposed circuit with a programmable NF within the band of interest. The overall minimum value is 2.5dB, obtained at 1GHz.Reconfiguration of S-parameters is illustrated in Fig. 6, whereas input reflection coefficient, S_{11} (Fig. 6(a)) and forward gain, S_{21} (Fig. 6(b)) are shown. The value of S_{21} varies from 19.8dB at 2.23GHz to 23.4dB at 1.9GHz, whereas S_{11} is always below -10dB. Note that —although not shown in Fig. 6 for the sake of clarity— the operation of the circuit can be continuously tuned within the band of interest, 1.75-2.23GHz. This feature is a direct consequence of using PMOS varactors in the resonant tank, providing approximately 500-MHz tuning range. Indeed, this is a peculiarity of the presented chip as compared to previously reported multi-standard LNAs, mostly based on using switchable LC tanks to select the operating frequency in a discrete way and using varactors to fine tuning the selected band. On the contrary, the proposed LNA achieves a coarse continuous frequency tuning capability, just using varactors. Indeed, this is a first step towards using a tuning frequency range of several GHz —required in future software radios.

The operation of the circuit has been tested for a couple of standard specifications within the band of interest, namely: GSM and WCDMA. As an illustration, Fig. 7 shows S-parameters for both standards, highlighting the values at the center frequency of each standard band.

Finally, Table I sums up the measured performance of the



(a)



(b)

Fig. 4. (a) Chip Microphotograph and (b) PCB.

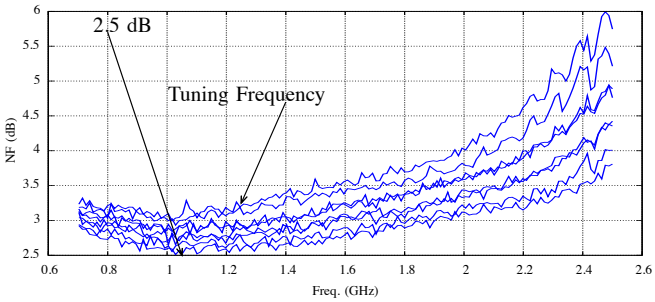
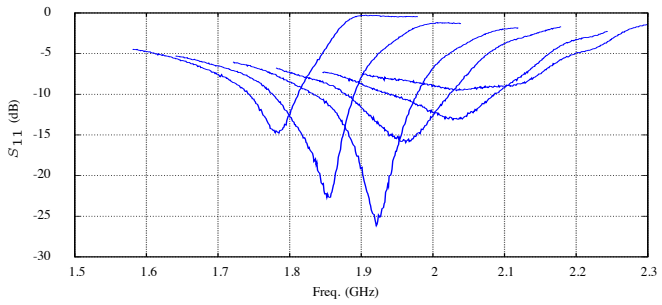


Fig. 5. NF reconfiguration.

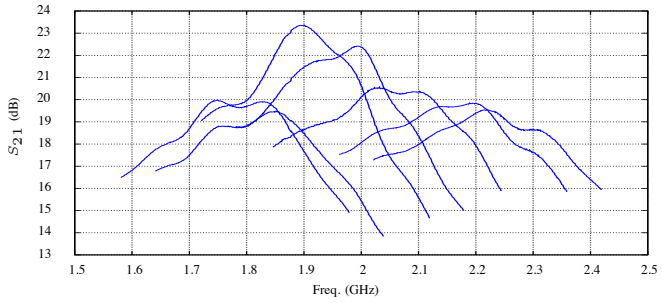
LNA by showing their main figures of merit. This performance is compared with reported multi-standard CMOS LNAs. Note that the circuit in this paper compares favorably to previous LNAs while showing continuous frequency tuning capability.

Conclusions

The experimental performance of a continuously-tuned CMOS LNA has been presented. The chip has been fabricated in a 90-nm CMOS technology and uses a single 1V supply

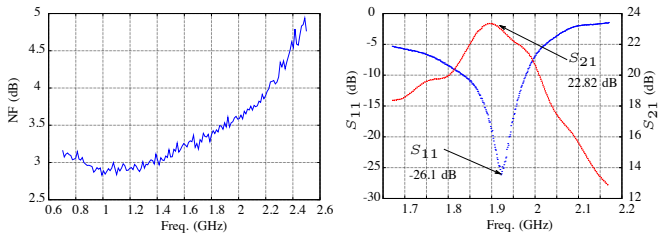


(a)

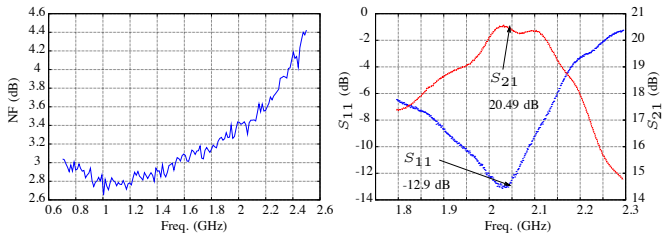


(b)

Fig. 6. Illustrating the reconfiguration of S-parameters: (a) S_{11} (b) S_{21}.



(a)



(b)

Fig. 7. Measured NF and S-parameters for (a) GSM and (b) WCDMA.

voltage. The combination of adaptive biasing and PMOS-varactor based tuning networks allows us to adapt the performance of the circuit to a number of specifications in a continuous way. Laboratory measurements show a competitive behavior as compared with the state-of-the art on multi-standard LNAs, whereas keeping a reduced number of inductors — similar to the mono-standard case. To the best of the authors' knowledge, the chip presented in this brief, constitutes one of the first experimental evidences of real digitally-controlled LNAs, showing a frequency tuning range of approximately 500-MHz around a 2GHz operation frequency.

REFERENCES

[1] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. United Kingdom: Cambrige University Press, 2 ed., 2004.

[2] M. Brandolini, P. Rossi, D. Manstretta, and F. Svelto, "Toward Multi-standard Mobile Terminals - Fully Integrated Receivers Requirements and Architectures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 1026–1038, 2005.

[3] V. Vidojkovic *et al.*, "Fully-integrated DECT/Bluetooth multi-band LNA in 0.18um CMOS," *IEEE International Symposium on Circuits and Systems*, pp. 565–568, 2004.

[4] Y. Koolivand, O. Shoaei, A. Zahabi, H. Shamsi, and P. Jabedar-Maralani, "A new technique for design CMOS LNA for multi-standard receivers," *IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 3231–3234, 2005.

[5] C.-W. Ang, Y. Zheng, and C.-H. Heng, "A Multi-band CMOS Low Noise Amplifier for Multi-standard Wireless Receivers," *IEEE International Symposium on Circuits and Systems*, pp. 2802–2805, 2007.

[6] P.-I. Mak, S.-P. U, and R. Martins, "Transceiver Architecture Selection: Review, State-of-the-Art Survey and Case Study," *IEEE Circuits and Systems Magazine*, 2007.

[7] F. Tzeng, A. Jahanian, and P. Heydari, "A Multiband Inductor-Reuse CMOS Low-Noise Amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, pp. 209–213, Mar 2008.

[8] Z. Li, R. Quintal, and K. O, "A dual-band CMOS front-end with two gain modes for wireless LAN applications," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2069–2073, Nov 2004.

[9] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 288–301, Jan 2002.

[10] H. Song, H. Kim, K. Han, J. Choi, C. Park, and B. Kim, "A Sub-2 dB NF Dual-Band CMOS LNA for CDMA/WCDMA Applications," *IEEE Microwave and Wireless Components Letters*, vol. 18, pp. 212–214, Mar 2008.

[11] S.-W. Kao, M.-C. Kuo, C.-S. Wang, Y.-B. Lee, C.-H. Chen, P.-U. Su, and T.-Y. Yang, "A Low-Power Dual-Band WLAN CMOS Receiver," *Asian Solid-State Circuits Conference*, pp. 397–400, 2005.

[12] C.-R. Wu and L.-H. Lu, "A 2.9-3.5-GHz tunable low-noise amplifier," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 206–209, 2006.

[13] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello, "A 0.13um CMOS front-end, for DCS1800/UMTS/802.11b-g with multiband positive feedback low-noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 981–989, Apr 2006.

TABLE I
LNA PERFORMANCE AND COMPARISON WITH STATE OF THE ART

Ref.	Standard	IIP_3 (dBm)	NF (dB)	P_{DC} (mW)	S_{21} (dB)
[5]	GSM 900	-12.8	4.6	32.4	18
	WLAN b/g	-15.3	4.43		24
	WLAN a	-14.7	4.42		23
[7]	WLAN b/g	-21.4	3.1	1.08	10
	WLAN a	-6.7	3.8	1.02	
[8]	ISM	-6.6	2.6	3	22.8
	UNII	-1	6.2	9.1	22.2
[9]	WLAN b/g	0	2.3	4	14
	WLAN a	5.6	4.5		15.5
[10]	CDMA	-5.8	1.75	7.5	8.42
	WCDMA	-5.3	1.97		10.97
[11]	WLAN b/g	4	2.8	16	14
	WLAN a	-3	3.9	19	16
[12]	2.9GHz–3.5GHz	-10	3.6	18	6
[13]	GSM	-7.5	5.2	24	28.5
	WCDMA	0	5.6		29.5
	WLAN b/g	-4.8	5.8		23.4
This Work	1.78 GHz	-9.74	3.62	23	19.74
	1.84 GHz	-10.24	3.65		19.6
	1.92 GHz (GSM)	-10.11	3.62		22.82
	1.98 GHz	-10.22	3.59		22.31
	2.045 GHz (WCDMA)	-10.5	3.43		20.49
	2.1 GHz	-10.5	3.48		20.53