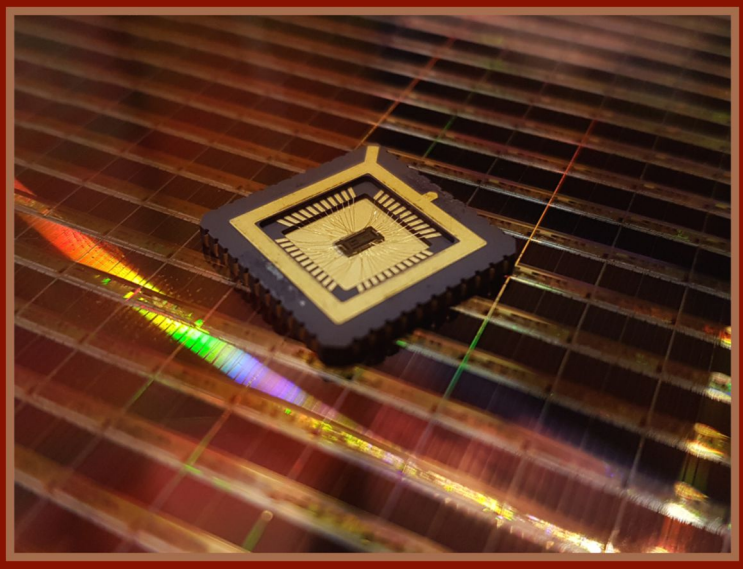
Doctoral Thesis

Industrial Electronics and Telecommunications Engineering

Performance enhancement in the design of amplifier and amplifier-less circuits in modern CMOS technologies



Author: Elena Cabrera Bernal

Supervisors: Antonio Jesús Torralba Silgado

Clara Isabel Luján Martínez

Electronic Engineering Department

Higher Technical School of Engineering

University of Seville

2018

Doctoral Thesis

Industrial Electronics and Telecommunications Engineering

Performance enhancement in the design of amplifier and amplifier-less circuits in modern CMOS technologies

Author:

Elena Cabrera Bernal

Supervisors:

Antonio Jesús Torralba Silgado

Clara Isabel Luján Martínez

Electronic Engineering Department

Higher Technical School of Engineering

University of Seville

Seville, 2018

Tesis doctoral: Performance enhancement in the design of amplifier and amplifier-less circuits in modern CMOS technologies

Autor: Elena Cabrera Bernal

Tutores: Antonio Jesús Torralba Silgado

Clara Isabel Luján Martínez

El tribunal nombrado para juzgar el Proyecto arriba indicado, compuesto por los siguientes miembros:

Presidente:

Vocales:

Secretario:

Acuerdan otorgarle la calificación de:

Sevilla, 2018

El Secretario del Tribunal

A mi familia.

Acknowledgements

They are some many, the people to whom I have to show my gratitude, that I am afraid some lines may not be enough.

Shall I start with my supervisors, Antonio Torralba and Clara Luján, as they gave me the opportunity of starting, developing and completing this exciting research, guiding me, with their expertise and wisdom, all along the path that has led me to the conclusion of this work.

Must also thank the economic support from the Government of Spain that granted me under the program FPI-MICINN.

I am also deeply grateful to Salvatore Pennisi, my advisor during my internship at the University of Catania and Esther Rodríguez, my advisor at Imperial College London. Not only they taught me about electronics, but also made me feel welcomed and at home. I want to mention also Jaime Ramirez as every talk I have had with him has been really inspiring.

Thanks to all my research group at the University of Seville, especially Fernando Muñoz and Ramón G. Carvajal whose technical advice has been essential. Not to forget Enrique López, Jose Ramón García and Fernando Marquez, always willing to help, and all my colleagues in the office, whose company has made everything funnier and easier to stand.

Every day, I am surprised how lucky I have been to share this period with not only a colleague but also a friend, Jose María Hinojo. The shared coffees, bacon and technical discussions (in the Spanish meaning of the word) may never be forgotten. This would have been much harder without you.

Y por encima de todo, gracias a mi familia. Es por ellos que hoy soy lo que soy. Gracias a mi padre, a mi madre, a mi hermana, por ser un ejemplo a seguir, por su apoyo, paciencia y cariño incondicional. Gracias también a Seba que ha vivido a mi lado esta etapa, con todos sus malos y buenos momentos. Sois lo mejor que tengo. Os quiero.

Elena Cabrera Bernal

Sevilla, 2018

Abstract

In the context of nowadays CMOS technology downscaling and the increasing demand of high performance electronics by industry and consumers, analog design has become a major challenge.

On the one hand, beyond others, amplifiers have traditionally been a key cell for many analog systems whose overall performance strongly depends on those of the amplifier. Consequently, still today, achieving high performance amplifiers is essential.

On the other hand, due to the increasing difficulty in achieving high performance amplifiers in downscaled modern technologies, a different research line that replaces the amplifier by other more easily achievable cells appears: the so called amplifier-less techniques.

This thesis explores and contributes to both philosophies. Specifically, a low-voltage differential input pair is proposed, with which three multistage amplifiers in the state of art are designed, analysed and tested. Moreover, a structure for the implementation of differential switched capacitor circuits, specially suitable for comparator-based circuits, that features lower distortion and less noise than the classical differential structures is proposed, an, as a proof of concept, implemented in a $\Delta\Sigma$ modulator.

1 INTRODUCTION

"Integrated circuits will lead to such wonders as home computers - or at least terminals connected to a central computer - automatic controls for automobiles, and personal portable communications equipment."

-G.E. Moore, 1965-

1.1 Motivation.

During the last decades, humanity has experimented the greatest technological revolution since the Industrial Revolution of the 19th century. In fact, the technological changes have been so fast that great differences exist between today's lifestyle and the one just few decades ago.

This technological revolution goes abreast CMOS technology development as, since the idea of manufacturing several transistors on a single substrate was conceived, the number of transistors integrated in the same area has increased following Moore's Law [1], thus reducing the associated manufacturing cost and making electronics accessible to everyone. As a consequence of the popularization of electronics, the demand of high performance hand-helded battery powered devices has grown enormously and, hence, high performance electronics are nowadays required in any field.

Furthermore, CMOS technology scaling also entails the reduction of the supply voltages in order to ensure circuit reliability and lifetime. However, in modern sub-micrometric technologies, the reduction of the transistor size and the power consumption budget implies a serious degradation of transistors' performance and, therefore, the design of high performance analog circuits becomes more challenging [2],[3].

In this context, analog circuit design is going through a new paradigm, where high performances must be achieved either by new design techniques or by revisiting and adapting the traditional designs to the new technological challenges. Both design trends have been explored throughout this thesis.

1.2 Research Goals.

One of the most important blocks in traditional design is the amplifier. Achieving high gain and, in general, high performance in amplifiers has become more difficult to achieve, as in modern technologies intrinsic device gains and supply voltages have decreased. As a consequence, two different design philosophies have arisen:

- Amplifiers designed with new techniques able to provide the required performances.
- Alternative design techniques that eliminate the need of amplifiers.

The aim of this thesis is to explore and contribute to both approaches.

1.3 Contributions.

As results of the performed research, the following contributions to the design of amplifier and amplifier-less circuits in modern CMOS technologies are presented, for both philosophies:

- Amplifiers designed with new techniques able to provide the required performances.
    - A Low-Voltage Bulk-Driven Three-Stage Class-AB Operational Transconductance Amplifier.
    - A Low-Voltage Bulk-Driven Three-Stage Class-AB Operational Transconductance Amplifier with Bulk-Driven Slew-Rate Boosting.
    - A Low-Voltage Bulk-Driven Four-Stage Class-AB Operational Transconductance Amplifier with Bulk-Driven Slew-Rate Boosting.
- Alternative design techniques that eliminate the need of amplifiers.
    - A new Differential structure for switched capacitor circuits, specially suitable for comparator-based switched capacitor circuits.

1.4 Thesis Organization.

This thesis is organized in four chapters as follows: after this first introductory chapter, on chapter 2, the first line of this thesis is explored. After a brief revision of low voltage amplifier techniques, three low-voltage bulk-driven multistage OTAs are presented and analysed. On chapter 3 the second line is explored, starting with

a review of the main amplifier-less techniques and then presenting a new technique for differential switched capacitor circuits. The last chapter summarizes the conclusions of this research and identifies the future work that can be derived from it.

2. LOW-VOLTAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

One of the most important blocks in analog microelectronics, is undoubtedly, the operational amplifier (OpAmp). It is used in a wide range of applications such as voltage regulation, filtering or analog to digital conversion among others, what makes it one of the most critical cell in any analog or mixed-signal system.

OpAmps are usually composed by a differential transconductance stage, one or more high-gain stages, a compensation network and an output buffer, that allows to drive low-resistance loads. OpAmps that are not intended to drive low resistance loads are usually called Operational Transconductance Amplifier (OTA) [4].

In this chapter, the first line of this thesis is explored: the classical OTA cell is revisited in order to achieve competitive performances at extremely low voltage solution with the aim of making it suitable for modern technologies. For that purpose, three multistage low voltage bulk-driven OTAs are presented.

2.1. Low Voltage Amplifier Design Techniques.

On the one hand, low power is one of the most important areas in nowadays electronics. The huge consumer demand of portable devices with great autonomy makes low power a key feature for product competitiveness. Therefore, the interest in low voltage has significantly increased due to the limitation in power consumption. On the other hand, in modern submicrometric technologies the maximum allowed voltage supply has decreased more abruptly than the threshold voltage, V_{th}, dramatically reducing the available voltage swing in classical OTA topologies. Nevertheless, achieving high enough gains has become more challenging as transistor's output resistance is reduced and, with the decrease of biasing voltages, the effective transconductance has also decreased [2]. Moreover, classical techniques such as cascoding are no longer appropriate for low voltage design.

Consequently, low voltage design techniques are lately receiving plenty of interest. An overview of the most important ones is presented below.

2.1.1. Threshold lowering.

As the main problem to achieve an appropriate signal swing in modern technologies is due to the high V_{th} values altogether with the reduced supply voltage, the more straightforward idea to implement a low voltage design is by reducing it. In some technologies, there are special transistors that perform low V_{th} o even zero V_{th}, but this usually implies higher costs and/or the use of special technologies.

Still, there is another option: in standard devices the V_{th} values can be reduced using the bulk [5]–[10]. The threshold voltage is given by

$$V_{th} = V_{th0} + \gamma \left(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|} \right) \qquad (2\text{–}1)$$

where, V_{th0} is the zero-bias threshold voltage, γ is the bulk effect factor and ϕ_F is the Fermi potential.

This technique can only be used in p-type MOS transistors in standard CMOS technologies.

2.1.2. Subthreshold.

Biasing transistors in the subthreshold region is an alternative way of increasing the voltage swing in a low voltage design [11]–[13]. Under these biasing conditions the gate-source voltage, V_{gs}, is slightly lower that V_{th} and the drain source voltage, V_{ds}, only needs to be around one hundred millivolts to be in saturation [14], thus the voltage headroom is increased compared to strong inversion operation.

Transistors in the subthreshold region are usually biased with small currents,

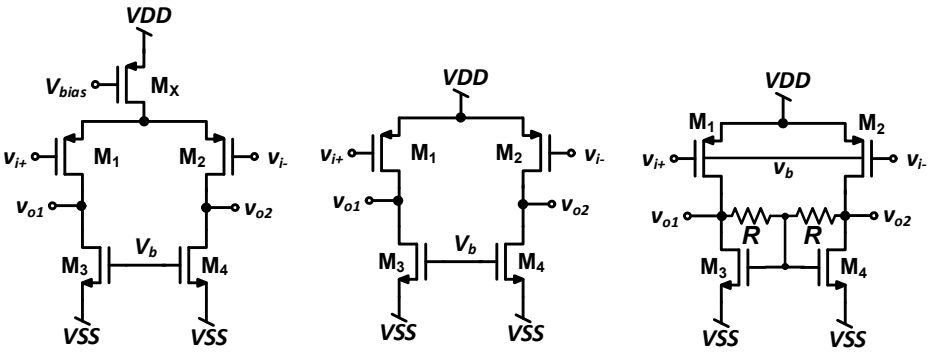
what is advantageous in a low power design context. However, low biasing currents entails less slew rate and bandwidth.

That is why this design technique is very common when low power consumption is required and speed is not a concern, for instance in biomedical applications [15].

2.1.3. Non-Tailed Pair.

The classical single-ended-OTA differential input stage is depicted in Figure 1 (a). It is well-known that in this structure, transistor M_X implements a current source that sets the bias current through the input pair transistors, M_1 and M_2. However, M_X consumes one V_{ds_sat}[1] of the available voltage headroom. Hence, getting rid of it will increment the voltage swing, making the structure suitable for low voltage design.

In Figure 1 (b) the non-tailed version of the classical input stage is depicted. Removing the tail current, however, makes this stage pseudo-differential and with a severe deterioration of common-mode rejection ratio, needing additional techniques to achieve reasonable rejection [16]. A fully-differential version, with better common-mode rejection ratio can be achieved by the non-tailed input stage shown in Figure 1 (c) [10]. Nevertheless, both input stages of Figure 1 (b) and Figure 1 (c) need additional methods to control de biasing current through the input pair should be added as the lack of the tail current makes them extremely dependent on temperature and process variations [7]–[10], [17], [18].



(a) (b) (c)

Figure 1: (a) Differential input stage of a classical OTA (b) Non-tailed version of the classical input stage (c) Non-tailed fully differential input stage.

2.1.4. Floating Gate Transistors.

Floating Gate (FG) transistors were first proposed in [19] for the design of a low voltage differential input pair. The operation of FG transistors consist on a

[1] V_{ds_sat} is the V_{ds} saturation voltage.

weighted capacitive coupling at the gate of a conventional MOS transistor as shown in Figure 2.

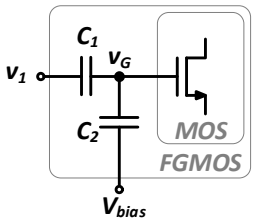


Figure 2: Floating Gate transistor.

Capacitor values are usually chosen to ensure that $C_2 \gg C_1$ and, given that

$$v_G = V_{bias}\frac{C_2}{C_1 + C_2} + v_1\frac{C_1}{C_1 + C_2} \tag{2–2}$$

the transistor can be properly biased through C_2 and V_{bias} while v_1 drives the signal, that is attenuated at the gate of the transistor, ensuring a wide input range [19], [20].

The main disadvantage of this technique is the reduction of the input stage transconductance and, thus, the total gain and bandwidth. Moreover, C_2 implementation may increase the consumed area. In deeply scaled technologies, the gate leakage current increases, jeopardizing the FG transistor behaviour.

2.1.5. Quasi-Floating Gate Transistors.

Similarly to FG transistors, in Quasi-Floating Gate (QFG) transistors [21], the input signal in capacitively coupled to a conventional MOS transistor, but instead of biasing the gate by a large capacitor, it is weakly connected to V_{bias} through a large resistor, R_{large}, as shown in Figure 3.

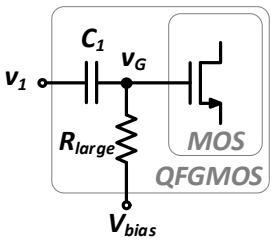


Figure 3: Quasi-Floating Gate transistor.

The gate voltage, v_G can be calculated as,

$$v_G = V_{bias}\frac{1}{1 + sR_{large}C_1} + v_1\frac{sR_{large}C_1}{1 + sR_{large}C_1} \tag{2–3}$$

Thus, for $s=0$ the gate is biased to the V_{bias} voltage, while the input signal v_1 will

be high pass filtered. However, as R_{large} should be large enough, the cut off frequency of the filter should be placed at frequencies lower than the minimum operating frequency of the circuit.

QFG transistors does not suffer from the transconductance reduction that affects FG transistors and, in practice, R_{large} can be implemented using transistors in cut off region (pseudoresistors) reducing the FG area consumption. However, experimental results show that they suffer slow large signal dynamics when the circuit is turned on. Those dynamics are not usually well modelled in computer aided design (CAD) software, so special attention must be paid when performing simulations [22]. In modern technologies passive resistors with relatively large values are feasible to integrate, so that, if the operating frequency is high enough, there is no need to use pseudoresistors.

2.1.6. Complementary Input Pair.

With the aim of increasing the input voltage swing in headroom-limited designs, two complementary pairs can be used as OTA input stage [23]–[26] as shown in Figure 4 [23].

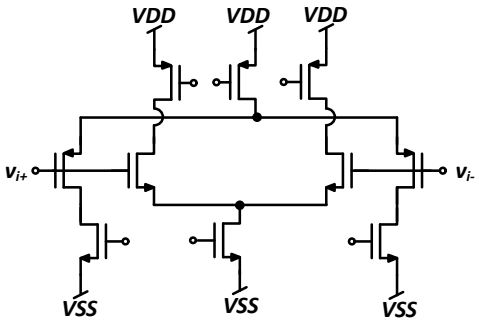


Figure 4: Complementary input pair.

The main idea is to have at least one pair operating over the complete input voltage range. Hence, when the input is too high for the p-type pair, the n-type is going to be active, and vice versa.

Despite complementary pairs indeed achieve rail-to-rail behaviour, the transconductance, as well as the slew rate, suffer important variations across the input signal swing, as the circuit passes through three different "states": only p-type pair active, both pairs active, only n-type pair active.

2.1.7. Level Shifting.

Similarly as in the complementary input pair, using two input pairs of the same, *p* or *n* type plus level shifters, can ensure rail-to-rail operation [27]. The idea is, again, turning on one of the pairs when the other turns off.

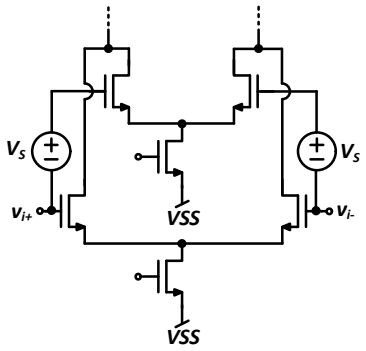


Figure 5: Double input pair with level shifters.

Level shifting presents the same disadvantages of transconductance and slew rate input dependence. It needs additional techniques to stabilize those parameters and additional circuitry to implement the level shifters.

2.1.8. Bulk Driven.

Bulk driven circuits use the bulk transconductance, g_{mb}, instead of the gate transconductance, g_m. The main advantage of driving the input though the bulk is that it has no threshold voltage associated and, as a result, the V_{th} limitation is avoided, making it specially suitable for low voltage designs.

Figure 6 (a) shows the regular gate driven transistor where the input is applied though the gate terminal and the bulk terminal is set to a constant bias voltage. In Figure 6 (b) a bulk driven transistor is depicted, where the input is applied through the bulk and the gate terminal is connected to a bias voltage that properly bias the transistor.

Figure 6: (a) Gate driven and (b) bulk driven PMOS transistors.

As this technique requires the bulk terminal to be accessible, in standard *n*-well technologies, only *p*-channel transistors can be bulk driven. The main disadvantage is the fact that g_{mb} is significantly smaller than g_m and, in amplifier design, this leads to poor DC gain and gain-bandwidth performances with larger noise and offset.

Specifically, if strong inversion is assumed, then the drain current is given by $I_D = \frac{\beta}{2}(V_{SG} - |V_{th}|)^2$. If the threshold voltage is substituted by $V_{th} = V_{th0} + \gamma\left(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}\right)$, then [28],

$$g_{mb} \equiv \frac{\partial I_D}{\partial V_{SB}} = \frac{|\gamma|}{2\sqrt{2|\phi_F| + V_{BS}}}\sqrt{2\beta I_D} = \frac{|\gamma|}{2\sqrt{2|\phi_F| + V_{BS}}} g_m = \eta g_m \qquad (2\text{–}4)$$

Depending on the technology $0.1 < \eta < 0.4$. The rest of the parameters have their usual meanings, being γ the body effect parameter, ϕ_F the Fermi potential and $\beta = \mu C'_{ox}(\frac{W}{L})$.

2.2. State of Art of Sub-1V Operational Transconductance Amplifiers.

In this section, the State of Art of Sub-1V OTAs is presented. First, previous works found on literature are briefly discussed and summarized, to finish with a comparison of their performances.

In order to discuss the different approaches found on literature, a chronological order is going to be followed here. In 2001 Lehmann et al. [5], propose a gate-driven folded cascade OTA implemented by a current driven bulk technique. In this proposal, the threshold voltage of the input pair is lowered by driving the bulk with a current instead of a voltage avoiding the possibility of forward biasing the bulk-source diode by maintaining the bulk current controlled under a certain value. Results demonstrate that the solution is able to work under 1 V supply in a 3.3 V technology with proper small signal performances but with poor SR.

In [29], Stockstad et al. propose a weak inversion OTA whose input pair is bulk-driven, but the input is applied through depletion-mode transistors used as buffers to minimize bulk currents. They achieve 70 dB gain and rail-to-rail behaviour at the input and the output under a 0.9 V supply in a 2.5 μm technology, with a reduced power consumption. However, the unity gain bandwidth is only 5.6 kHz.

Yao et al. propose, in [30], a single-stage gate-driven fully differential OTA, based on a current mirror amplifier with gain enhancement. Although it has very good small signal behaviour with a low power consumption, its slew rate is poor.

In [6] Chatterjee et al. propose two 0.5 V fully-differential OTA, both biased in moderate inversion. The first approach is bulk-driven while the second one is driven by the gate and implements threshold lowering through the bulk of *n*-type transistors, thus requiring triple-well devices. The proposed OTAs achieve good performances, but extremely limited input common-mode range.

In [31] Ferreira et al. propose an improved version of the traditional two-stage Miller OTA, operating at weak inversion and combining bulk-driven input and level-shifters to provide rail-to-rail operation. It effectively achieves low voltage (0.6 V in a technology of 2.5 V) and low power, but speed and slew rate are not particularly good.

In [32], Zuo et al. propose a two-stage bulk-driven folded-cascode OTA with transconductance enhancement able to operate under 1 V in a technology whose nominal supply voltage is 3.3 V. Although it achieves good small signal performances, the large signal behaviour is rather poor

Ferreira et al. presents, in [33], a two-stage bulk-driven folded-cascode OTA in weak inversion, able to operate under 0.25 V and very low-power consumption. It achieves very good performances, considering the extremely low supply and power consumption, by enhancing the transconductance and, also, the output resistance of transistors at the expense of area consumption.

In [16], a three-stage bulk-driven OTA with non-tailed input pair operating in subthreshold is presented by Abdelfattah et al.. The OTA is able to operate even under 0.35 V in a technology with a nominal supply voltage of 1.2 V. They show good measured performances but under a quite small loading capacitance.

Tang et al. propose in [34] a rail-to-rail bulk-driven two-stage OTA that operates under 0.9 V in a technology with a nominal supply of 1.8 V. It also implements a transconductance stabilization technique. Although it achieves good speed and slew rate, it consumes too much current.

Finally, in [7] Grasso et al. propose a gate-driven two-stage non-tailed OTA with threshold lowering that operates under 0.9 V in a 3.3 V technology, achieving a good common-mode range but limited slew rate.

Table 1 summarizes the main performance of the works that have been discussed here.

Year, Ref.	Tech [µm]	Supply [V]	DC Current [µA]	C_L [pF]	DC Gain [dB]	UGBW [MHz]	PM [°]	Average SR [V/µs]	CMRR [dB]	FoM_S [MHz·pF /mW]	FoM_L [V·pF/ (µs·mW)]
2001 [5]	0.5	1	40	20	69	2	57	0.5	-	1000	250
2002 [29]	2.5	0.9	0.5	12	70	0.0056	62	-	26	149	-
2003 [30]	0.25	0.8	10	18	50	1.2	60	0.2	-	2700	450
2005 [6]	0.18	0.5	220	20	52	2.5	-	2.89	78	455	525
	0.18	0.5	150	20	62	10	-	2.0	74	2666	533
2007 [31]	0.35	0.6	0.916	15	69	0.011	65	0.014	74	300	382
2013 [32]	0.35	1	197	15	88	11.67	66	1.95	40	889	148
2014 [33]	0.13	0.25	0.072	15	60	0.002	52	0.0007	-	1667	583
2015 [16]	0.065	0.5	366	3	46	38	57	43	35	623	705
	0.065	0.35	49	3	43	3.6	56	5.6	46	630	980
2015 [34]	0.18	0.9	290	17	76	7.11	72	2.98	55	463	194
2017 [7]	0.35	0.9	27	10	65	1	60	0.25	45	411	102

Table 1: Performance comparison of Sub-1V OTAs.

The two traditional Figures of Merit (FoM) [35]–[37] shown in equation (2-5) have been evaluated and included in Table 1.

$$FoM_S = \frac{UGBW \cdot C_L}{Power}$$
$$FoM_L = \frac{SR \cdot C_L}{Power} \qquad (2\text{–}5)$$

FoMS and FoML allow a comparison of small signal and large signal performance, respectively. In both cases higher values mean better performances: in FOMS (where subscript *S* stands for "small signal") higher unity-gain bandwidth, UGBW, and load capacitance, CL, at low power consumption is preferred, whereas in FOML (where subscript *L* stands for "large signal") higher slew rate, SR, higher, CL and low power consumption is preferred.

Figure 7 graphically shows the FoMs of each publication discussed above. It can be observed that the amplifiers with better FoML [16] present poor FoMS and viceversa [6], [30].

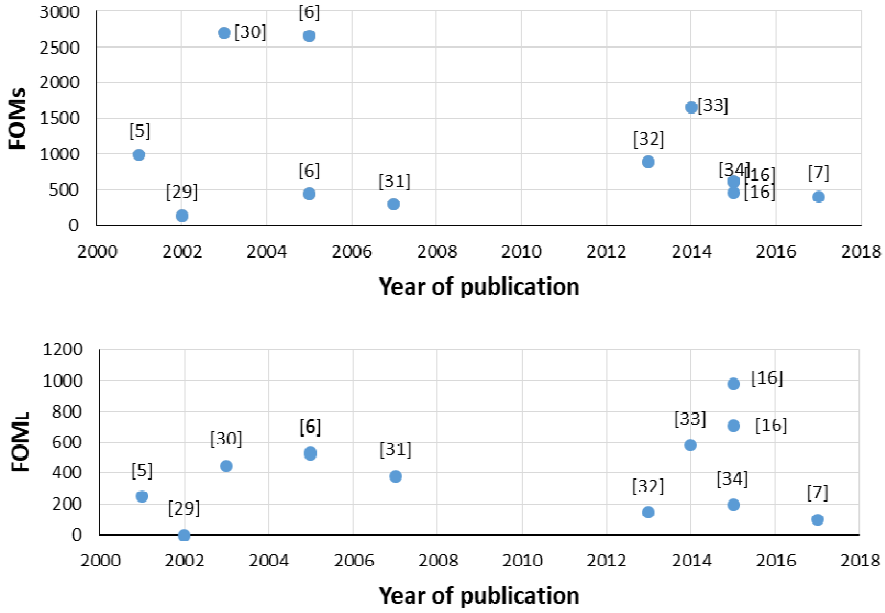


Figure 7: FOMS and FOML Vs Year of Publication of Sub-1V OTAs.

2.3. Contributions.

Taking advantage of more than one of the described low-voltage techniques is a common strategy [6], [7], [16], [24], [29], [31], [33], [38], [39].

For the OTAs proposed in this thesis, with the aim of achieving good small and large signal performances, a bulk-driven version of the non-tailed differential input pair of Figure 1 (c) is used as the first stage of all the three contributions, what allows extremely reduced biasing voltage and, as the quiescent current through the input pair is fixed by the gates while the input is driven through the bulk, no additional bias current control is required. This input stage is interesting, as it can implement either single-ended or fully-differential solutions as it is.

As a proof of concept, three single-ended OTA are proposed. In order to provide adequate DC gain, the first two proposed OTAs adopt three-stage architectures [13], [16] while the last one is a four-stage [40]. Class-AB outputs are chosen to enhance the large signal performances, and, additionally, for the last two contributions, the classical Class-AB output is improved taking once again advantage of the bulk terminal. The three proposed OTAs were fabricated in a standard 180 nm CMOS technology in order to validate their performances.

2.3.1. Non-Tailed Bulk-Driven Differential Input Stage.

The Non-Tailed Bulk-Driven Differential pair, used as the input stage for the three proposed OTAs, is the bulk-driven version of the input stage proposed on [8] and it is depicted in Figure 8. It is composed by transistors M_1 and M_2, whose quiescent currents are accurately set by transistor M_R, whose body is tied to the virtual ground (i.e., $(VDD+VSS)/2$). Hence, M_R-M_1 and M_R-M_2 form two accurate current mirrors, provided that also the bulk of M_1-M_2 is connected to the analog ground. The active load of the first stage is implemented by transistors M_3-M_4 and two resistors, R. Due to the fact that no DC current flows through resistors, the drains and gates of M_3-M_4 are at the same potential. This stage is specially suitable for low voltage design, as the minimum supply voltage (VDD-VSS) can be as low as $V_{DS1,2} + V_{GS3,4}$. Moreover, resistors R accurately set the output DC common-mode voltage, what would not happen in the bulk-driven version of the classical non-tailed pair of Figure 1 (b).

The transistors and biasing values used for the three implementations are summarized in Table 2.

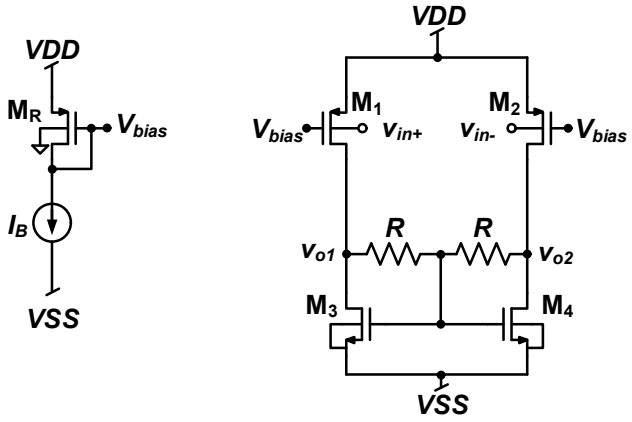


Figure 8: Non-Tailed Bulk-Driven Differential Pair.

Device	Value	Device	Value
M_R, M_1, M_2	12µm/540nm	I_B	4 µA
M_3, M_4	2µm/540nm	R	250 kΩ
		VDD-VSS	0.7 V

Table 2: Transistors dimensions and device values of the Non-Tailed Bulk-Driven Differential Pair.

As the three proposed OTAs share exactly the same implementation of the first stage, they also share the performances directly related to the first stage behaviour. Specifically: differential gain of the first stage, common mode rejection ratio (CMRR), input common mode range (ICMR) and noise.

2.3.1.1. Differential Gain.

In the input stage of Figure 8, the use of resistors R in the active load enables fully differential operation of an otherwise pseudo-differential pair M_1-M_2. In order to illustrate this fact, a single-ended small-signal voltage, v_d, is applied at one input (e.g., the bulk of M_1), while grounding the second input (bulk of M_2).

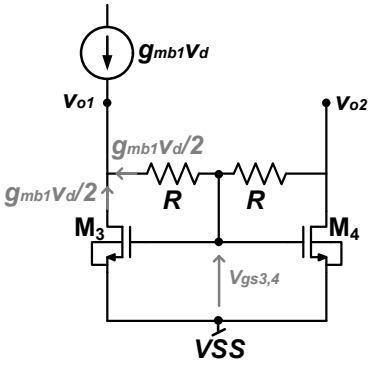


Figure 9: Circuit for differential behaviour demonstration.

As depicted in Figure 9, voltage v_d is converted into a current, $g_{mb1}v_d$, one half of which will flow through the resistor series and the other half through transistor M_3 because M_3 and M_4 have the same gate-source voltage, $v_{gs3,4}$, and the same transconductance, $g_{m3,4}$, and must, consequently, carry the same current. Figure 9 shows then that a differential output voltage, v_{o1}-v_{o2}, is generated. The expression of the individual output voltages can be approximated by

$$\begin{aligned} v_{o1} &= v_{gs3,4} - g_{mb1}R\frac{v_d}{2} \\ v_{o2} &= v_{gs3,4} + g_{mb1}R\frac{v_d}{2} \end{aligned} \tag{2–6}$$

where the output resistances of the transistors have been neglected[2]. Given that $g_{mb1,2}\frac{v_d}{2} = g_{m3}v_{gs3,4}$, then:

$$\begin{aligned} v_{o1} &= g_{mb1,2}\left(\frac{1}{g_{m3,4}} - R\right)\frac{v_d}{2} \\ v_{o2} &= g_{mb1,2}\left(\frac{1}{g_{m3,4}} + R\right)\frac{v_d}{2} \end{aligned} \tag{2–7}$$

Assuming that $g_{m3,4}R \gg 1$, then (2-6) yields $v_{o1} = -v_{o2} = g_{mb1}R\frac{v_d}{2}$, demonstrating differential operation, since the application of v_d from only one input terminal produces a differential output, as opposed to a pseudo-differential topology. For the symmetry of the circuit, the same result holds also if the input signal is applied to the bulk of M_2.

As a conclusion, the (single ended) gain of this first stage, can be approximated by[3]

$$A_d = \frac{v_{o2}}{v_d} \approx \frac{g_{mb1,2}R}{2} \tag{2–8}$$

2.3.1.2. Common Mode Rejection Ratio.

Under a common mode excitation, as no current flows through resistors R, the drain and source terminal of M_3 and M_4 are set to the same potential. Referring to Figure 10, and taking in to account that $g_{mb1} = g_{mb2} = g_{mb1,2}$ and $g_{m3} = g_{m4} = g_{m3,4}$, this absence of current thought the resistors implies that $g_{mb1,2}v_{cm}$ must equal $g_{m3,4}v_{gs3,4}$. Therefore, the common mode gain is

[2] More accurate expression of the output voltage should include the parallel of R, $r_{ds1,2}$ and $r_{ds3,4}$, instead of R alone.

[3] To note that in a fully-differential implementation, the gain of the proposed input stage will be in the order of that achieved in the classical differential non-tailed pair of Figure 1 (b) as long as R is large enough.

$$A_{cm} = \frac{v_{o2}}{v_{cm}} = -\frac{g_{mb1,2}}{g_{m3,4}} \tag{2–9}$$

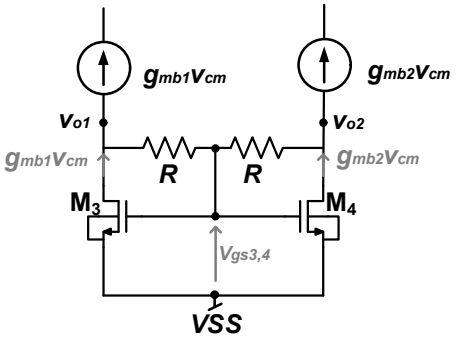


Figure 10: Circuit for differential input stage CMRR analysis.

This outcome can be easily understood by considering that if no current flows through the resistors then M_3 and M_4 operate as they are connected in diode and offer an equivalent resistance equal to $1/g_{m3,4}$.

Hence, the (single ended) CMRR, defined as $|A_d/A_{cm}|$, is given by:

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = \frac{1}{2}\frac{g_{mb1,2}R}{\frac{g_{mb1,2}}{g_{m3,4}}} = \frac{1}{2}g_{m3,4}R \tag{2–10}$$

From (6) we see that $R >> 1/g_{m3,4}$ must be chosen to obtain adequate CMRR values. In the classical implementation of Figure 1(b) the CMRR value is equal to 1, so in this terms, the proposed structure presents a valuable improvement.

2.3.1.3. Input Common Mode Range.

The input common mode range (ICMR) of the proposed differential pair is, in practice, limited by the maximum allowable input current.

Due to its bulk driven input, the input current is expected to be relatively high if compared to a gate driven input stage. As V_{BS} changes from *VDD* to *VSS* this current is going to increase as the bulk-source *pn* junction becomes more forward biased [28].

Hence, the maximum allowable input current has been chosen to be 4 nA at 27°C. As the quiescent current through the input transistors is set to 4 μA, the input current is thus 1000 times smaller and, thus, negligible. By simulation, this $V_{BS} = V_{BSmax} = 550$ mV, what means an ICMR of 550 mV, from 150 mV to 700 mV.

2.3.1.4. Noise.

Noise performance of bulk driven circuits is also worsened if compared to its gate

driven counterpart [41]. For the proposed stage of Figure 8, considering only white noise for simplicity, the equivalent input-referred noise voltage power spectral density (PSD) of the proposed amplifier can be approximated as

$$S_{V,in} \approx 2S_{V1,2}\left(\frac{g_{m1,2}}{g_{mb1,2}}\right)^2 + 2S_{V3,4}\left(\frac{g_{m3,2}}{g_{mb1,2}}\right)^2 + S_{VR,in} \tag{2–11}$$

where S_{Vi} is the well-known gate-referred noise voltage Power Spectral Density (PSD) of transistor M_i, $S_{VR,in}$ in the input-referred equivalent noise contribution of resistors R, k is the Boltzmann's constant and T is the absolute temperature.

For the calculation of $S_{VR,in}$, the simplified small signal model illustrated in Figure 11 is used to find the voltage gain between v_{nR} and the outputs of the first stage, v_{o1} and v_{o2}.

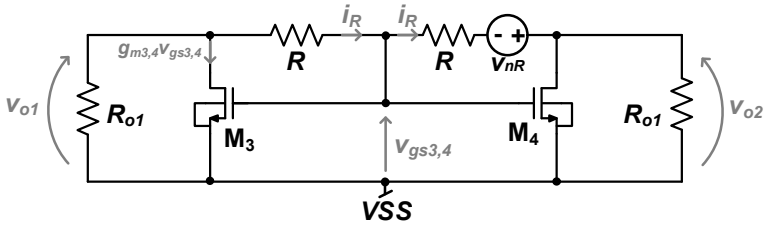


Figure 11: Schematic for resistors R noise analysis.

Then, it can be seen that

$$\begin{gathered} i_R = g_{m3,4}v_{gs3,4} + \frac{v_{o2}}{R_{o1}} = -g_{m3,4}v_{gs3,4} - \frac{v_{o1}}{R_{o1}} \\ v_{o1} = v_{gs3,4} + Ri_R \\ v_{o1} = v_{gs3,4} - Ri_R + v_{nR} \end{gathered} \tag{2–12}$$

where R_{o1} is the output resistance of the stage $R_{o1} = r_{ds3,4}//r_{ds1,2}$.

Then, the transfer functions can be calculated as

$$\begin{aligned} \frac{v_{o1}}{v_{nR}} &= \frac{g_{m3,4}R - 1}{2\left(1 + g_{m3,4}R_{o1}\right)\left(1 + \frac{R}{R_{o1}}\right)} \approx \frac{1}{2}\cdot\frac{R}{R + R_{o1}} \\ \frac{v_{o2}}{v_{nR}} &= \frac{1 + g_{m3,4}(R + 2R_{o1})}{2\left(1 + g_{m3,4}R_{o1}\right)\left(1 + \frac{R}{R_{o1}}\right)} \approx \frac{1}{2}\cdot\frac{R + 2R_{o1}}{R + R_{o1}} \end{aligned} \tag{2–13}$$

where the approximations hold for $g_{m3,4}R >> 1$ and $g_{m3,4}R_{o1} >> 1$.

Due to the symmetry of the circuit, v_{o1}/v_{nR} represents also the transfer function from the noise source of the left-side resistor to v_{o2}. This noise contribution of the left-side resistor is lower than that of the right-side resistor as can be seen by comparing both equations of (2-13) which imply the product of 0.5 by a quantity lower than the unity and greater than the unity, respectively. Finally, $S_{VR,in}$ is

evaluated by considering that the gain from the inverting input to the output of the first stage is $A_d = -\frac{g_{mb1,2}(R_{o1}//R)}{2}$. Therefore we get:

$$S_{VR,in} = S_{VR}\frac{1}{4}\left[\left(\frac{R}{R+R_{o1}}\right)^2 + \left(\frac{R+2R_{o1}}{R+R_{o1}}\right)^2\right]\left(\frac{2}{g_{mb1,2}(R_{o1}//R)}\right)^2 \tag{2–14}$$

Being $S_{VR} = 4kTR$ then:

$$S_{VR,in} = 4kTR\left(\frac{1}{g_{mb1,2}R_{o1}}\right)^2\left[1+\left(1+\frac{2R_{o1}}{R}\right)^2\right] \tag{2–15}$$

Therefore, according to (2-11)

$$\begin{aligned} S_{V,in} &= 2S_{V1,2}\left(\frac{g_{m1,2}}{g_{mb1,2}}\right)^2 + 2S_{V3,4}\left(\frac{g_{m3,4}}{g_{mb1,2}}\right)^2 + S_{VR,in} \\ &= 2\frac{2}{3}4kT\frac{1}{g_{mb1,2}}\left(\frac{g_{m1,2}}{g_{mb1,2}}+\frac{g_{m3,4}}{g_{mb1,2}}\right) \\ &\quad + 4kTR\left(\frac{1}{g_{mb1,2}R_{o1}}\right)^2\left[1+\left(1+\frac{2R_{o1}}{R}\right)^2\right] \end{aligned} \tag{2–16}$$

where the well know $S_{Vi} = \frac{2}{3}4kT\frac{1}{g_{mi}}$ has been substituted. The noise generated in the resistors can be neglected if $(g_{m1,2}+g_{m3,4})R_{o1} \gg \frac{3}{4}\frac{R}{R_{o1}}\left[1+\left(1+\frac{2R_{o1}}{R}\right)^2\right]$ condition that is usually met. Thus,

$$S_{V,in} \approx \frac{16}{3}kT\frac{1}{g_{mb1,2}}\frac{g_{m1,2}+g_{m3,4}}{g_{mb1,2}} \tag{2–17}$$

Finally, if $g_{m3,4} \ll g_{m1,2}$ is selected, the noise of $M_{3,4}$ could be neglected too, yielding to an equivalent input-referred noise voltage PSD of

$$S_{V,in} \approx \frac{16}{3}kT\frac{1}{g_{mb1,2}}\frac{1}{\eta} = \frac{16}{3}kT\frac{1}{g_{m1,2}}\frac{1}{\eta^2} \tag{2–18}$$

where $\eta = g_{mb1,2}/g_{m1,2}$ However, $g_{m3,4} \ll g_{m1,2}$ cannot be easily set since large $g_{m3,4}$ values are needed from (2-10) to achieve sufficient CMRR without requiring excessively large R values. When compared to the classical approach of Figure 1 (b) additional resistors R add more noise.

Noise in multistage amplifiers is usually dominated by the first stage provided that this first stage has a voltage gain considerably larger than unity.

2.3.1.5. Large signal behaviour.

Due to its non-tailed structure, the proposed input stage large signal behaviour is not limited by the tail current and, in fact, can deliver and sink instantaneous currents larger than its nominal quiescent current, which is characteristic of Class-AB circuits.

In order to further explain this, let us assume a unity-gain voltage follower configuration, where a negative step is applied to the positive input as shown in Figure 12. When the positive input goes down, the v_{gs} of transistor M_4 increases so M_4 can instantaneously sink higher currents than its nominal value.

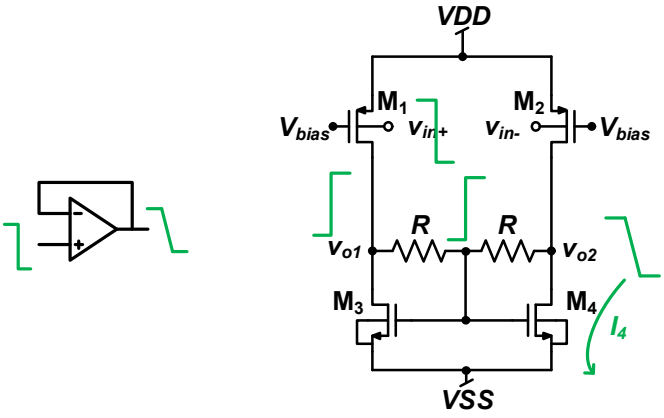


Figure 12: Large Signal behavior. Negative Step.

The opposite happens when a positive step is applied: v_{gs} of M_4 decreases almost switching off M_4, so M_2 delivers currents directly from *VDD* that again are larger than its quiescent values.

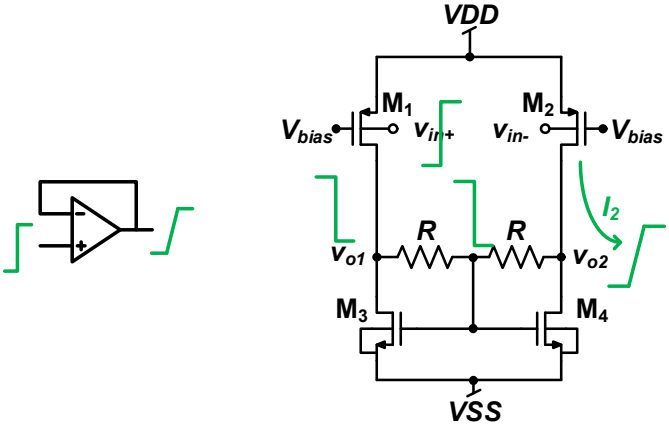


Figure 13: Large Signal behavior. Positive Step.

This Class-AB behavior is an additional enhancement of the input stage when compared to the classical one shown on Figure 1 (b).

Due to the advantages of the proposed bulk-driven non-tailed input stage in terms of CMRR, DC common mode output and large signal behavior when compared to the classical non-tailed stage, it has been chosen as the input stage for the three OTAs proposed in this thesis. This input stage is particularly advantageous for the implementation of fully-differential solutions, anyway, single-ended OTAs has been implemented in this thesis as a proof of concept for the validation and test of its performances. Fully differential implementation is straightforward and part of the future work.

2.3.2. Low-Voltage Bulk-Driven Three-Stage Class-AB OTA.

Using the proposed input stage of Figure 8, together with Class-AB stages the complete OTA of Figure 14 is proposed with the aim of achieving both good large and small signal performances under low voltage supply. It is made up of three gain stages: the already explained differential input stage (M_1-M_4), a second common-source stage (M_5-M_6) and a third common-source stage (M_7-M_{10}). The implemented transistors dimensions and device values for this design are summarized in Table 3.

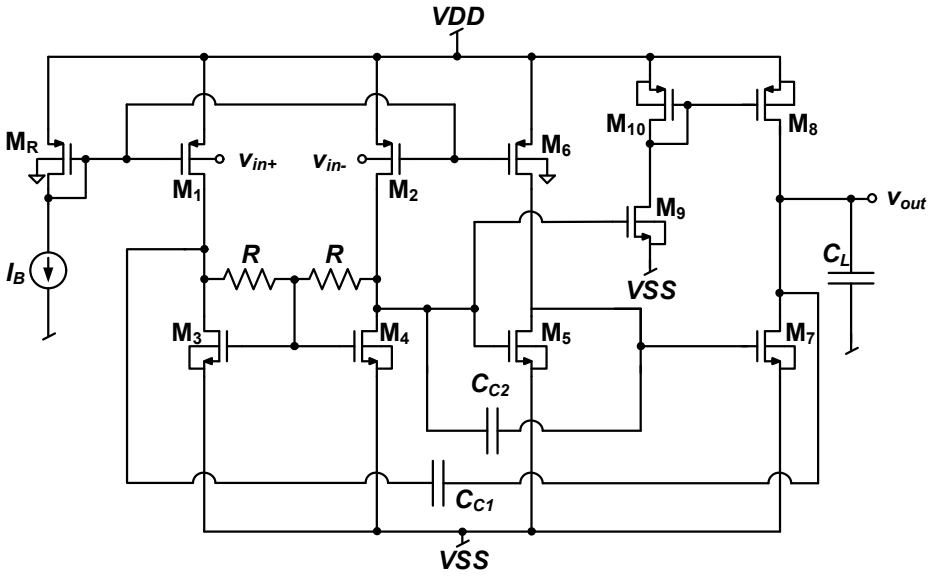


Figure 14: Three-stage Class-AB OTA.

Device	Value	Device	Value
M_R, M_1, M_2, M_{10}	12µm/540nm	I_B	4 µA
M_3, M_4, M_9	2µm/540nm	C_{C1}	550 fF
M_5, M_7	5µm/540nm	C_{C2}	30 fF
M_6, M_8	30µm/540nm	R	250 kΩ
C_L	20 pF	VDD-VSS	0.7 V

Table 3: Transistors dimensions and device values of the Three-Stage Class-AB OTA.

Transistor M_R, whose bulk is tied to the virtual ground, as explained in the above section, sets the quiescent current of the differential pair (M_1-M_2) and load (M_3-M_4) of the first stage. At the same time, M_R also sets the quiescent current of transistor M_6 that acts as the load of the second stage. Due to the fact that no DC current flows through resistors *R*, the drains of M_3-M_4 are at the same potential of their gates and, consequently, the DC current of M_5 is also accurately set by (pseudo) current-mirror ratios of M_4 and M_5

$$I_{D5} = I_{D4}\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4} \tag{2–19}$$

The matching between the DC currents of M_5 and M_6, causes the drain of M_5 to be theoretically at the same potential of the drain of M_4, ultimately defining the current of M_7, again through a mirror ratio

$$I_{D7} = I_{D4}\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} \tag{2–20}$$

Note that current I_{D8} is set through current mirror M_8-M_{10} and pseudo current mirror M_9-M_4. Therefore, to theoretically nullify systematic offset, I_{D8} must be equal to I_{D7} leading to

$$\frac{\left(\frac{W}{L}\right)_8\left(\frac{W}{L}\right)_9}{\left(\frac{W}{L}\right)_{10}\left(\frac{W}{L}\right)_4} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} \tag{2–21}$$

A final comment regards the Class-AB behaviour of the third stage. Both transistors M_7 and M_8 can deliver a maximum signal current that is not limited by any DC value. Indeed, M_7 is in common source configuration, whereas the current in M_8 increases when V_{in+} increases because v_{GS9} also increases.

2.3.2.1. Frequency compensation.

Frequency compensation of the differential (open loop) gain is obtained through Miller capacitors C_{C1} and C_{C2} and a current buffer [42] implemented by M_3-M_4, with a similar technique to that developed in [37] for a nested-Miller-compensated OTA.

The simplified small signal model of the OTA of Figure 14 is depicted in Figure 15, where the parasitic capacitances have been neglected for simplicity and R_{oi} represents the resistance of the output node of the i^{th} stage. Values of transconductances and resistances for the proposed OTA are provided in Table 4: .

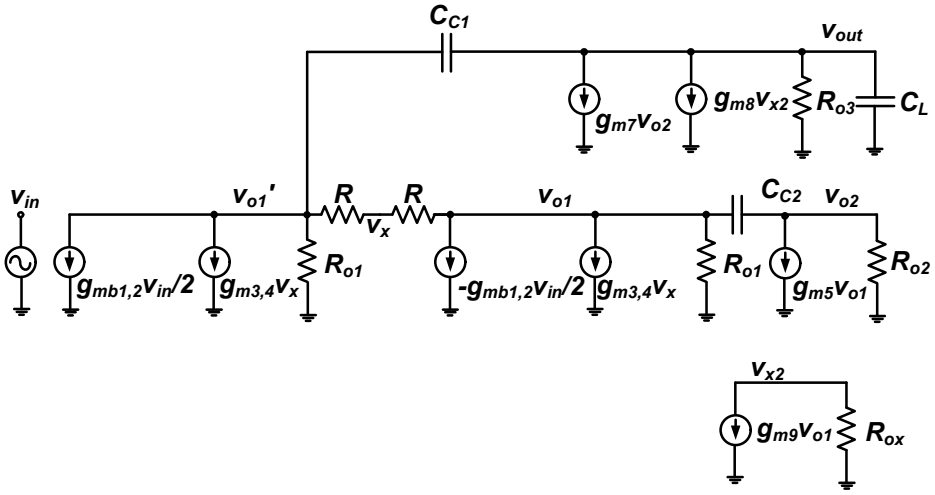


Figure 15: Small signal model of the Three-stage Class-AB OTA.

Trans-conductance	Value [μA/V]	Trans-conductance	Value [μA/V]	Output resistance	Value [kΩ]
$g_{mb1,2}$	12	g_{m7}	150	$R_{o1}=r_{ds1}//r_{ds3}$	1535
$g_{m1,2}$	65	g_{m8}	150	$R_{o2}=r_{ds5}//r_{ds6}$	214
$g_{m3,4}$	65	g_{m9}	60	$R_{o3}=r_{ds7}//r_{ds8}$	224
g_{m5}	162	g_{m10}	60	$R_{ox}=r_{ds1}//(1/g_{m10})$	16
g_{mb6}	30				

Table 4: Transconductances and output resistance values of the Three-Stage Class-AB OTA.

Solving the simplified small signal model circuit leads to the following open loop gain transfer function:

$$A(s) \approx A_0 \frac{\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)(as^2+bs+1)} \tag{2–22}$$

Assuming $g_{mi}R_{oi}$, $g_{mi}R$ >>1, simple equations can be provided for the DC gain, A_0, zero, z_1, and dominant pole, p_1, as well as for the coefficients of the polynomial of the complex conjugate poles, a, b.

$$\begin{aligned} A_0 &= \frac{g_{mb1}g_{m5}g_{m7}RR_{o1}R_{o2}R_{o3}}{2(R+R_{o1})} \\ z_1 &= \frac{g_{m5}g_{m3}}{g_{m5}C_{C1}-g_{m3}C_{C2}} \\ p_1 &= \frac{2(R+R_{o1})}{g_{m5}g_{m7}C_{C1}RR_{o1}R_{o2}R_{o3}} \\ a &= \frac{C_{C2}C_L(g_{m3}+2g_{m5})}{g_{m3}g_{m5}g_{m7}} \\ b &= \frac{C_L(C_{C1}+g_{m5}C_{C2}R_{o2})}{g_{m5}g_{m7}C_{C1}R_{o2}} \end{aligned} \tag{2–23}$$

The damping coefficient of the pair of complex poles is given by

$$\xi = \frac{b}{2\sqrt{a}} = \frac{C_{C1}+C_{C2}g_{m5}R_{o2}}{2C_{C1}R_{o2}}\sqrt{\frac{C_Lg_{m3}}{g_{m5}g_{m7}C_{C2}(2g_{m5}+g_{m3})}} \tag{2–24}$$

Given $g_{mb1,2}$, C_L and C_{C1}, one can derive from (2-24) a suitable value of C_{C2} in order to avoid peaking in the frequency response and to obtain a phase margin in the range of 60 to 70 degrees. Besides, $g_{m5}/g_{m3}>C_{C2}/C_{C1}$ can be chosen in order to obtain a negative zero from (2-23) useful to increase the phase margin.

From (2-23) the gain-bandwidth product, $\omega_{GBW,}$ is given by

$$\omega_{GBW} = \frac{g_{mb1,2}}{C_{C1}} \tag{2–25}$$

Substituting the values given in Table 4 on the above equations, the calculated transfer function can be plotted. In Figure 16 the calculated Bode is depicted altogether with the postlayout simulated Bode diagram.

It can be seen that at low frequencies the equations provide a good approximation. In the vicinity of the unity gain frequency, the effect of parasitics makes the simulated and the calculated Bode differ. However, the proposed simplified model provides manageable equations and reasonably

good modelling. Further details regarding these discrepancies are provided on Appendix A.

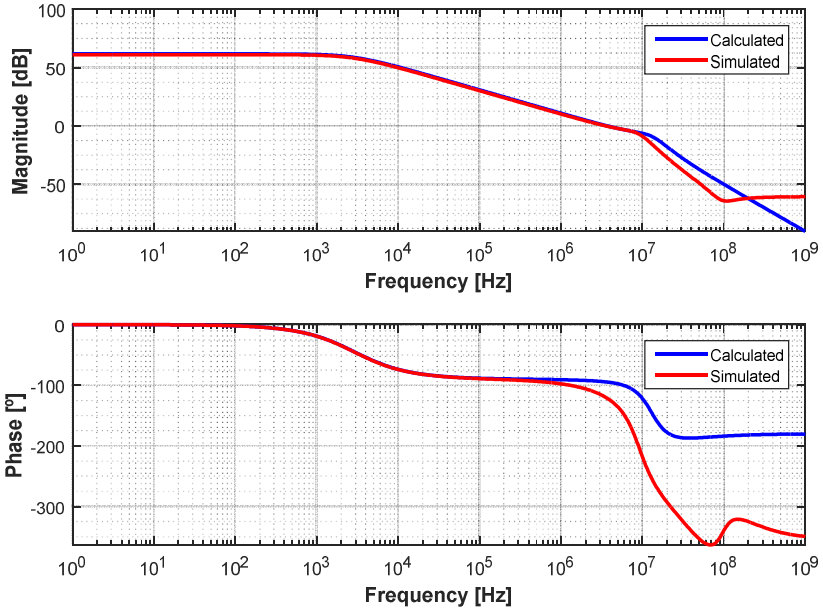


Figure 16: Calculated and simulated frequency response of the Three-Stage Class-AB OTA.

2.3.2.2. Slew Rate.

The slew rate (SR) of an OTA is the maximum output voltage rate. It occurs when the maximum current flowing into a capacitor is limited [4]. Hence, in multistage amplifiers the SR is going to be determined by the slowest stage, i.e., $SR=\min[I_x/C_x]$, where I_x is the maximum charging of discharging current of the load capacitor of the x-th stage, C_x.

For the proposed OTA implementation, the slowest stage is the last one as the loading capacitor C_L is the largest. The negative SR is determined by common source transistor M_7, whose maximum instantaneous current is in principle larger than the maximum current that the load transistor, M_8, can provide. This makes the positive slew rate smaller that the negative one. This fact is partially alleviated making the output stage Class-AB, as explained before, using the current mirror formed by transistors M_8 and M_{10}, however, still with this Class-AB operation the maximum current that M_8 can provide to the load capacitor, C_L is still smaller than the one that M_7 provides, so that the unbalanced positive and negative SR persists. Simulations show positive SR of 2.16 V/μs and negative SR of 4.42 V/μs for nominal corner.

2.3.2.3. Power Supply Rejection Ratio.

The Power Supply Rejection Ratio (PSRR) defines the capability of a circuit to reject the variations of the power supply. It is defined as [4]

$$PSRR = \frac{\Delta V_{supply}}{\Delta V_{out}} A(s) \tag{2–26}$$

A common strategy to determinate the PSRR is using the voltaje-follower configuration, where the output is fedback to the negative input of the OTA and the positive input is set to the analog ground. PSRR+ and PSRR- can be then calculated as PSRR+ = V_{dd} / V_{out} and PSRR- = V_{ss} / V_{out} [4].

Figure 17 shows the low-frequency small signal model used for calculating the positive PSRR at DC, where $r_{dsi} = 1/g_{dsi}$ is the drain-source resistance of transistor *i*.

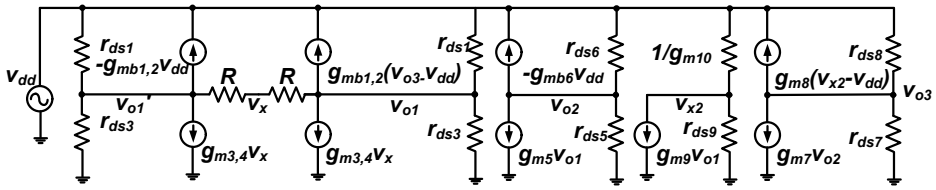


Figure 17: Small signal model for the calculation of PSRR+ at low frequencies for the Three-Stage Class-AB bulk-driven OTA.

Solving the circuit, the numerator and denominator of PSRR+ are given by

$$\begin{aligned} NUM_{PSRR+} &= g_{mb1,2}\, g_{m3} g_{m5} g_{m7} R R_{o1} R_{o2} \\ DEN_{PSRR+} &= 2[(R + R_{o1} + g_{m3}\mathrm{R}_{o1}^2 + g_{m3}\mathrm{R}R_{o1})(g_{m8} + g_{ds8} - g_{m8}g_{m10}R_{ox} \\ &\quad - g_{m7}(g_{mb6} + g_{ds6})R_{o2}) \\ &\quad + R_{o1}(R + R_{o1})(g_{mb1} + g_{ds1})(g_{m5}g_{m7}R_{o2} + g_{m8}g_{m9}R_{ox})] \end{aligned} \tag{2–27}$$

For the calculation of the PSRR-, the low-frequency small signal model of Figure 18 was solved, giving a negative PSRR numerator and denominator that can be approximated by

$$\begin{aligned} NUM_{PSRR-} &= g_{mb1,2}\, g_{m3} g_{m5} g_{m7} R R_{o1} R_{o2} \\ DEN_{PSRR-} &= 2[(R + R_{o1} + g_{m3}\mathrm{R}_{o1}^2 + g_{m3}\mathrm{R}R_{o1})(g_{m7} + g_{ds7} \\ &\quad - g_{m8}R_{ox}(g_{m9} + g_{ds9}) - g_{m7}(g_{m5} + g_{ds5})R_{o2}) \\ &\quad + R_{o1}(R + R_{o1})(g_{m3} + g_{ds3})(g_{m5}g_{m7}R_{o2} + g_{m8}g_{m9}R_{ox})] \end{aligned} \tag{2–28}$$

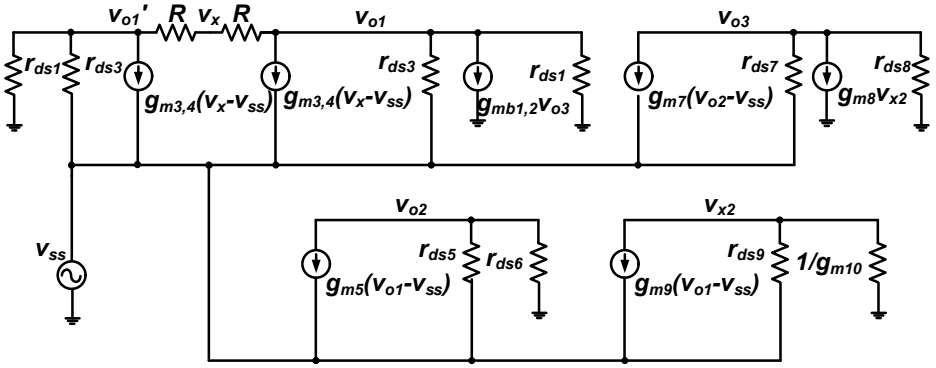


Figure 18: Small signal model for the calculation of PSRR- at low frequencies for the Three-Stage Class-AB bulk-driven OTA.

Substituting the transconductance and resistance values of Table 4 on the provided equations, a positive and negative PSRR of 60 dB and 71 dB are obtained, while in simulations 62 dB and 72 dB, respectively, are obtained, validating the equations.

2.3.2.4. Implementation and validation.

As it has been mentioned before, the proposed OTA has been designed and implemented in a standard 180 nm CMOS technology with threshold voltages around $V_{thp} = 0.35$ V and $V_{thn} = 0.45$ V. The design operates under a 0.7 V single supply.

Transistors' aspect ratios and transconductances, as well as the rest of the design parameters and values were summarized in the tables of Table 3 and Table 4. Resistors are physically implemented with 1792 Ω/□ high-resistive poly. Each resistor occupies 13.47 μm × 1.67 μm. Figure 19 shows a microphotograph of the chip the designed layout, which occupies a total area of 0.019 mm².

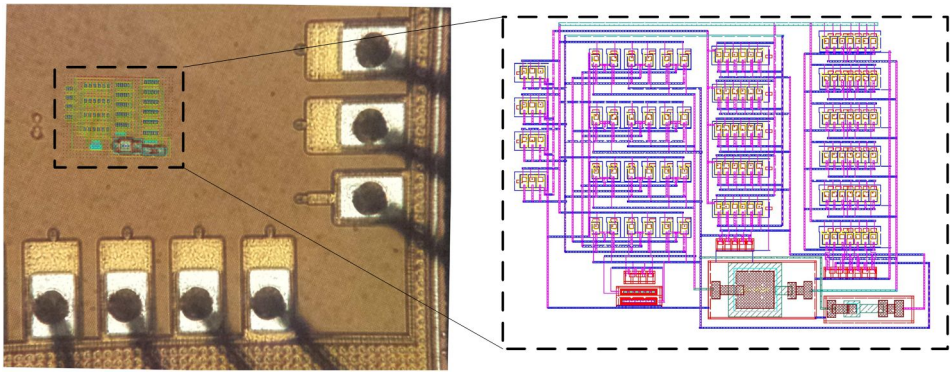


Figure 19: Microphotograph of the chip and layout of the Three-stage Class-AB OTA.

The proposed OTAs were designed for a certain technology option (Option 1) but due to foundry imposition they were finally fabricated in a different option (Option 2). That issue has negatively impacted on the measured performances.

Specifically, it has been observed that Option 2 has smaller transconductances, bigger output resistances and higher bulk and gate-related parasitics.

To note that the simulation results provided throughout all this chapter correspond to the technology option Option 1 for which the OTAs were designed.

Appendix B provides more details regarding the technology options.

In order to check the robustness of the standby current control in the last stage of the proposed structure, a MonteCarlo simulation is performed (process and mismatch, 1000 iterations). The associated histogram is plotted in Figure 20.

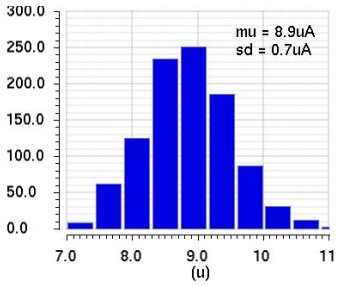


Figure 20: Histogram of the standby current of the third stage of the Three-stage Class-AB OTA.

From this analysis, a mean quiescent current of 8.9 μA is obtained (aspect ratios designed for 10 μA). The standard deviation is only 0.7 μA.

Input Common Mode Range.

As stated before, the maximum ICMR is actually limited by the maximum allowable input current, that was set to 1000 times the drain current of the input pair (4 nA) so that it can be neglected, resulting in a simulated ICMR of 550 mV_{pp} (from 150 mV to 700 mV).

The input current has been measured at 20°C, obtaining the results shown in Figure 21.

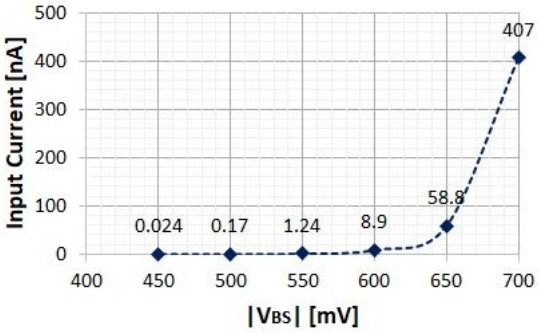


Figure 21: Measured input current versus bulk-source voltage @ 20°C of the Three-stage Class-AB OTA.

It can be observed from the results that the actual measured input current for $|V_{BS}|$=550 mV is lower than the estimation of the simulator; actually, 1.24 nA. This was expectable not only because the design was fabricated in another technology option but also because the current of a forward-biased *pn* junction is usually overestimated in simulators [28].

Regarding the dependence with temperature of the input current, it is going to be presumably strong, as, again, it corresponds with the temperature dependence of the current through a *pn* junction that approximately doubles each 10°C [4]. Thus, according to the measurements it can be inferred that if the ICMR is limited to 550 mV, then the input current will remain below 100 nA up to 80°C.

A final comment regarding the input current stands for the possibility of latch up to occur if $|V_{BS}| > 0.6$ V. With the ICMR limitation, the maximum $|V_{BS}|$ is limited to $|V_{BS}|_{max} = 550$ mV so the bulk-source diode should not enter conduction, hence latch up should not occur. Despite this, usual layout precautions (double guard rings) have been also taken. Indeed, during experimental verification latch up has not happened, even if the ICMR was forced to a higher value (~0.7 V).

Frequency response.

The nominal postlayout simulated frequency response Bode plot is represented in Figure 22. Additionally, Figure 23 shows the results of MonteCarlo analysis (process and mismatch, 1000 iterations) for the DC gain, unity gain bandwidth (UGBW) and phase margin (PM).

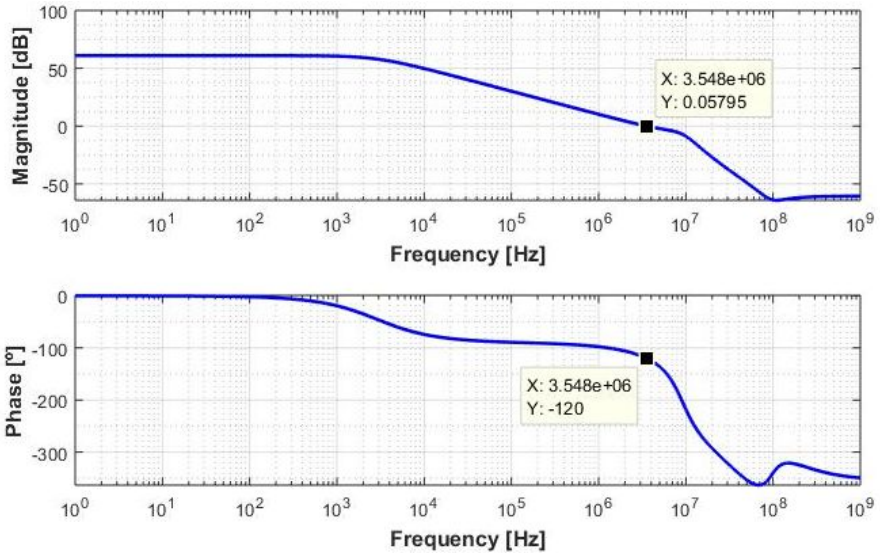
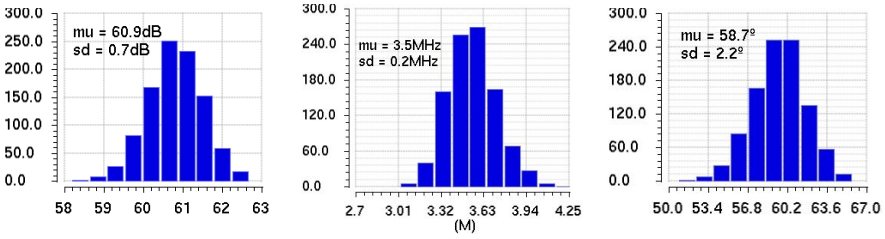


Figure 22: Nominal simulated frequency response of the Three-Stage Class-AB OTA.



(a) (b) (c)

Figure 23: MonteCarlo results for (a) DC gain, UGBW (b) and (c) phase margin of the Three-Stage Class-AB OTA.

These results show the robustness of the solution. A mean DC gain of 61 dB, with standard deviation (σ) of 0.7 dB is obtained. The mean UGBW is equal to 3.5 MHz, with a deviation of 0.2 MHz, while the phase margin mean value results to be 59°, with a standard deviation of 2.2°. That means, considering the 3-σ rule[4], that even in the worst case the phase margin is above 45° (actually, 52°) so the system should remain stable. These three parameters were also experimentally tested: Figure 24 shows a measurement of the UGBW and phase margin, carried out using a vector network analyzer (Rohde&Schwarz ZVRL). A UGBW of 3 MHz and a phase margin of 60° were measured.

[4] 3-σ rule states that 99.7% of the outcomes lie within three standard deviations of the mean.

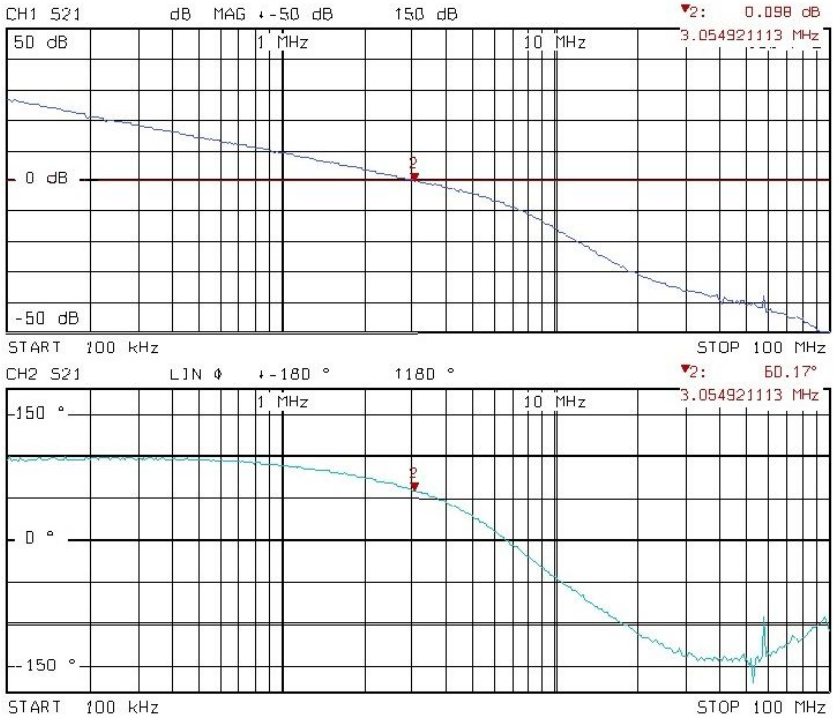


Figure 24: UGBW and phase margin measurement of the Three-stage Class-AB OTA.

For this OTA, despite being fabricated in a different option of the technology, measurements properly fit expected results.

DC gain.

Regarding the DC gain, as the first pole is placed at a frequency lower than the vector analyzer's minimum frequency of operation (9 kHz), it was measured using an oscilloscope (Agilent MS08104A),like proposed on [43] and depicted in Figure 25, obtaining a value of 57.5 dB.

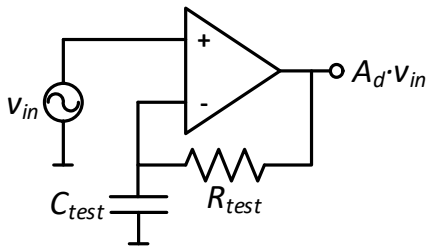


Figure 25: Low-frequency differential gain test circuit.

Resistor R_{test} and capacitor C_{test} are chosen large enough (3 MΩ, 1 μF) for properly set the DC and, as they act as a high pass filter, the pole is set below the first pole of the OTA introduce so at certain frequencies the low frequency A_d can be

measured.

Thereby, a value of 57.5 dB was measured. This value is lower than expected by MonteCarlo simulation, but easily explained if the fabricated technology presents lower $g_m \cdot r_o$ product.

Common Mode Rejection Ratio.

The CMRR obtained via simulation is depicted on the histogram of Figure 26, corresponding to a MonteCarlo simulation of 1000 iterations for process and mismatch. A mean CMRR of 14.7 dB with a standard deviation of 2.6 dB is obtained.

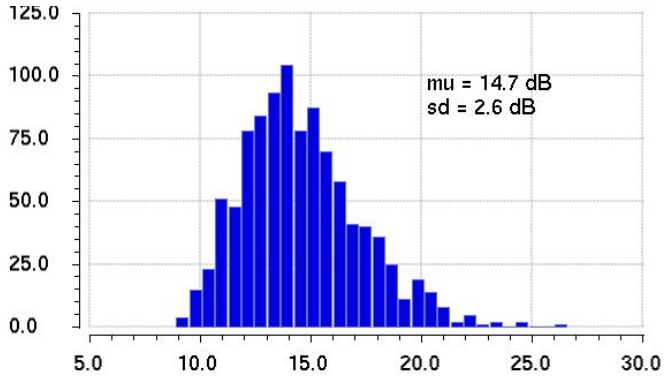


Figure 26: Histogram of the CMRR of the Three-stage Class-AB OTA.

Experimental validation was fulfilled using and oscilloscope and the test circuit of Figure 27 [43], similarly as done for the differential gain. In this case, C_{test} ensures that at proper frequency values both OTA inputs are driven by the same input V_{in}, thus A_{cm} can be measured, obtaining a value of 38.5 dB.

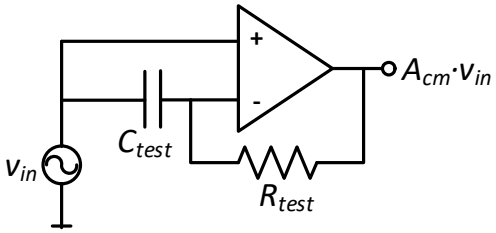


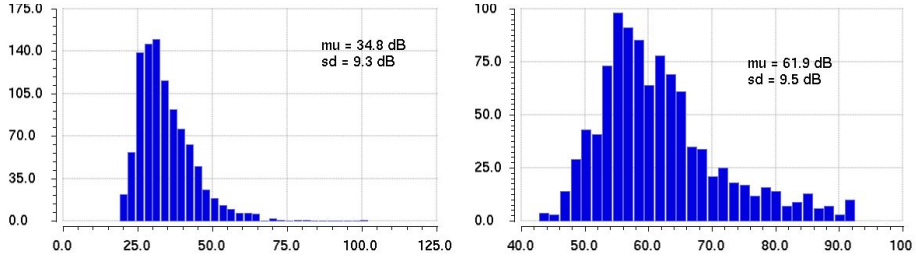
Figure 27: Low-frequency common-mode gain test circuit.

Hence, the CMRR can be obtained by simply:

$$CMRR[dB] = A_d[dB] - A_{cm}[dB] = 57.5dB - 38.5dB = 19dB \qquad (2\text{–}29)$$

Power Supply Rejection Ratio.

Statistical simulations of the positive and negative PSRR of the proposed OTA have been performed, assuming process and mismatch variations, and its histograms are depicted in Figure 28.



(a) (b)

Figure 28: Histogram of the (a) PSRR+ and (b) PSRR- of the Three-stage Class-AB OTA @DC.

Huge variability is observed in the results, what evidences a strong dependency with the variability of the technology process and mismatch.

Measurements of five samples show mean results of 45 dB and 57 dB for the positive and negative PSRR, respectively. As the OTA was fabricated in a different technology and PSRR variability is high, it is expectable to obtain results that does not properly fit with the simulated results.

Input Referred Noise.

The input referred noise was also experimentally validated. In Figure 29 the measured noise is plotted altogether with the noise simulated in the technology option in which the OTA was designed (Option 1). It can be observed that the measured results are below the simulations, with around 100 nV/√Hz at 1 MHz of input referred noise density.

As the main contributor to noise is flicker noise, it makes sense that the simulations in the technology option where the OTA was fabricated are above the measured results, provided that the measured circuit is fabricated in other technology and that the flicker noise is strongly variable with process and mismatch[5].

[5] Moreover, the model provided by the foundry for the flicker noise of Option 1 tends to overestimate it.

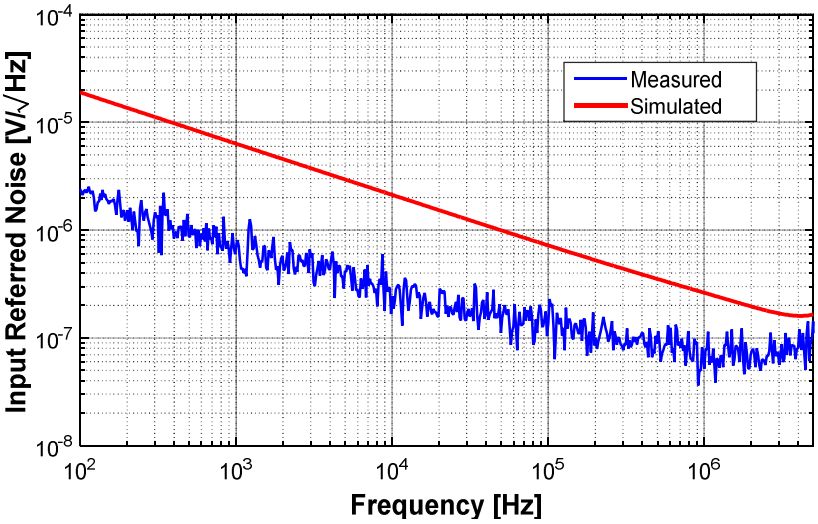


Figure 29: Simulated and measured input referred noise spectral density of the Three-stage Class-AB OTA.

Transient Response.

The simulation of the transient response for the voltage-follower configuration of Figure 30 is shown in Figure 31 for the nominal corner and an input of 500 mV_{pp}.

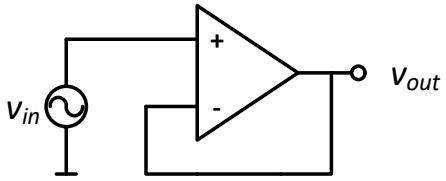


Figure 30: Voltage-follower configuration.

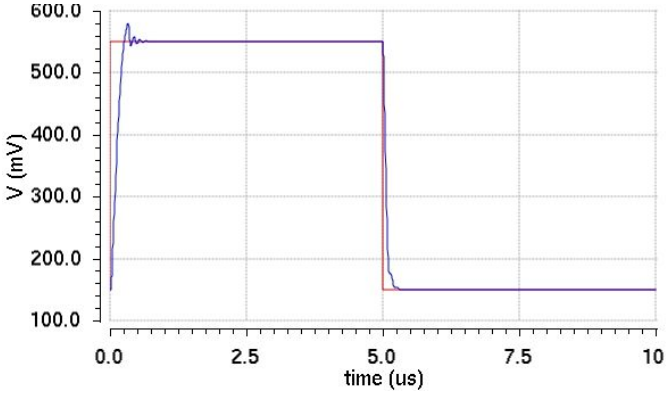


Figure 31: Simulated voltage-follower step response to a 500 mV_{pp} input of the Three-stage Class-AB OTA.

In Table 5 the slew rate and 1% settling time (ST), obtained for different corners, are summarized. The asymmetry between the values for the positive and negative slope that was explained on section 2.3.2.2 can be observed.

Corner	*SR+/SR- [V/µs]*	*ST+/ST- [ns]*
Nominal	2.16/4.42	498/270
FF	2.92/5.90	437/237
SS	1.59/3.22	544/253
FS	2.15/5.57	497/253
SF	2.00/3.44	489/240

Table 5: Simulated slew rate (SR) and settling time (ST) for different corners of the Three-Stage Class-AB OTA.

The measured step response is shown in Figure 32 where a positive SR of 1.8 V/µs and a negative SR of 3.8 V/µs were obtained. Although SR results are in agreement with simulations the positive settling time is found to be doubled, obtaining around 0.9 µs. Negative settling time is around 0.2 µs.

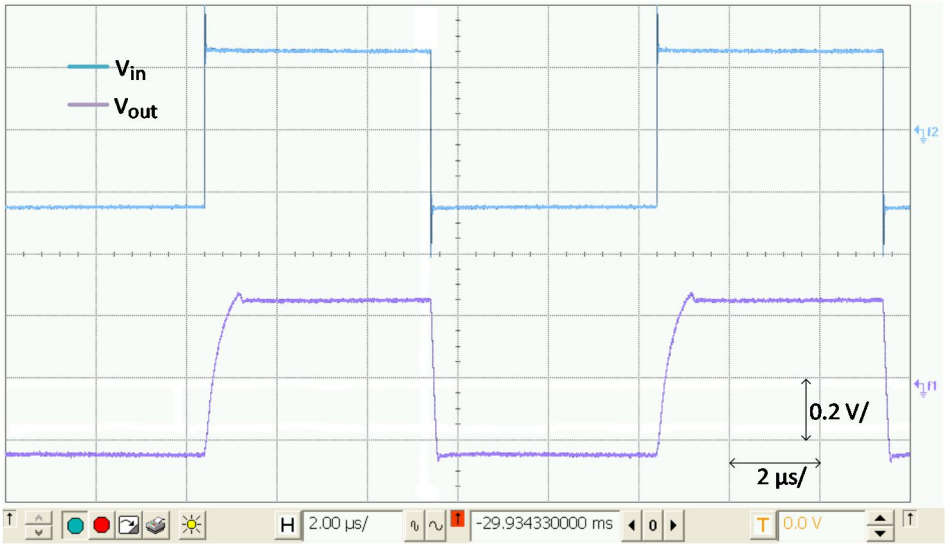


Figure 32: Measured voltage-follower step response to a 500 mV_{pp} input of the Three-stage Class-AB OTA.

Performance Summary.

Table 6 shows a summary of the measured parameters of the proposed Three-Stage OTA.

Parameter	*Value*
Supply voltage (VDD-VSS) [V]	0.7
Power dissipation [µW]	25.4
Area [mm²]	0.019.8
Offset (maximum) [mV]	11
ICMR [mV]	550 (from 150 mV to 700 mV)
Max Input Current [nA] @ 20°C	1.3
Open-Loop DC Gain [dB]	57.5
UGBW [MHz]	3
Phase Margin [°]	60
*SR+/SR- [V/µs]**	1.8/3.8
*1% ST (+/-) [µs]**	0.9/0.2
CMRR@DC [dB]	19
PSRR@DC (+/-) [dB]	45/57
Input Ref. Noise @1MHz [nV/√Hz]	100
*THD @100kHz, 400mV$_{p-p}$ input [%]***	0.20
*THD@250kHz, 400mV$_{p-p}$ input [%]***	0.99

*Voltage follower configuration
**Inverting configuration

Table 6: Measured performance parameters of the Three-Stage Class-AB OTA under 20 pF loading.

At the end of this chapter the performance of this OTA is discussed altogether with the other two proposed OTAs and compared with other State-Of-Art Amplifiers.

2.3.3. Low-Voltage Bulk-Driven Three-Stage Class-AB OTA with Bulk-Driven Slew-Rate Boosting.

2.3.4. Low-Voltage Bulk-Driven Four-Stage Class-AB OTA with Bulk-Driven Slew-Rate Boosting

2.4. Conclusions.

In this chapter, a Non-Tailed Bulk-Driven Differential Input Stage, suitable for very low-voltage design is presented and analysed. Three different multistage Class-AB OTAs have been implemented, all of them sharing the same proposed input stage, as a proof of concept: two three-stage, one of them with an additional technique to enhance the SR. Finally a four-stage OTA is presented.

The three OTAs were analysed, designed and fabricated. However, due to

foundry imposition, they were finally fabricated in a different technology option (details provided in Appendix B) with smaller transistor g_m, higher transistor r_o and, higher parasitics. Due to the robustness of the design and compensation, this has barely affected the performances of the Three-Stages OTAs

Table 16 shows a comparison of the performances of the proposed OTAs altogether with the Sub-1V amplifiers found in the State-Of-Art that were commented in section 2.2. In order to carry out a quantitative comparison, the two traditional Figures of Merit (FoMs and FoML) are evaluated and, for convenience, shown again in equation (2-55).

$$FoM_S = \frac{UGBW \cdot C_L}{Power}$$
$$FoM_L = \frac{SR \cdot C_L}{Power} \qquad (2\text{–}30)$$

Figure 33 and Figure 34 show the comparison in a graphical way. It is apparent that the proposed amplifiers outperform almost all other previously reported bulk-driven OTAs. In particular, as far as parameter FoML is concerned, the proposed OTAs display the maximum values by far. Regarding the FoMs parameter, Contribution 3 performs the best result, followed by [30] and [6] and then Contributions 1 and 2.

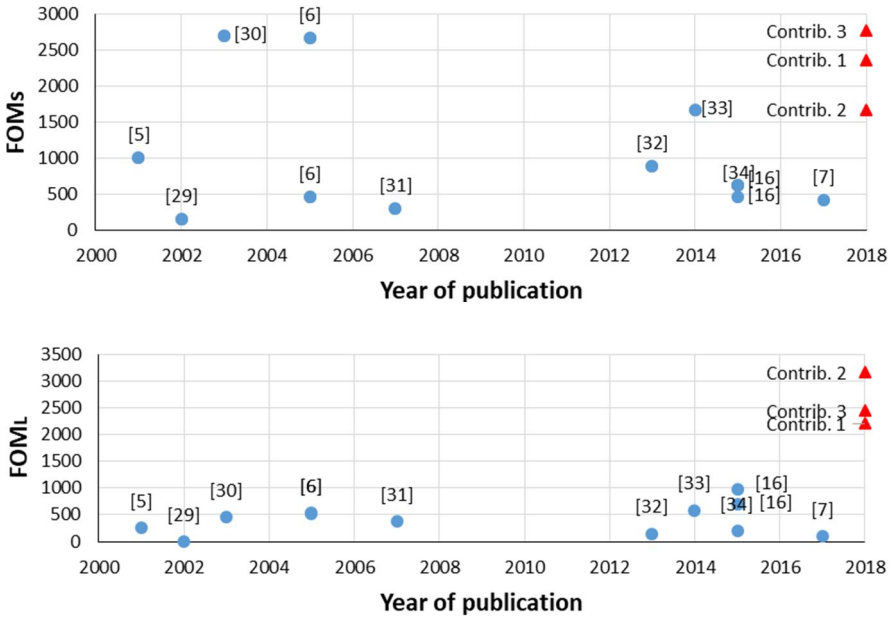


Figure 33: FOMs and FOML Vs Year of Publication of Sub-1V OTAs.

In Figure 34 FOMs and FOML are depicted together for further comparison.

As the proposed OTAs are the only ones placed in the upper-right quadrant it is apparent that their overall performance outstand the other solutions proposed in literature.

However, they perform the worst CMRR among all the other solutions found in the comparison, thus, an effort to overcome this issue should be accomplished in future research.

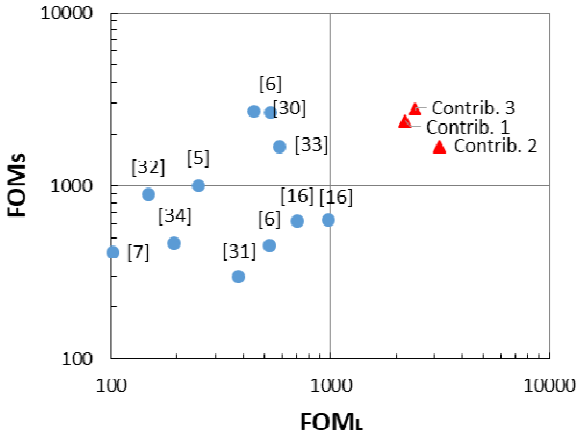


Figure 34: FOMs Vs FOML of Sub-1V OTAs.

The achieved performances have been possible thanks to the combination of all the discussed techniques. Summarizing, the bulk-driven input, applied in a non-tailed differential pair, allows a very low-voltage supply while maintaining a wide input common-mode range. Gain is provided by multiple stages, and quiescent currents properly set structurally. Large signal performances are achieved through Class-AB stages, and, in the last two contributions, making use of the bulk to further enhance the Class-AB behavior. Nonetheless, the bulk-driven non-tailed structure means poor CMRR and PSRR and the noise worsening related to bulk-driven inputs.

Year, Ref.	Tech. [µm]	Supply [V]	DC Current [µA]	C_L [pF]	DC Gain [dB]	UGBW [MHz]	PM [°]	Average SR [V/µs]	CMRR [dB]	PSRR [dB]	Noise [nV/√Hz]	FoM_S [MHz·pF /mW]	FoM_L [V·pF/ (µs·mW)]
2001 [5]	0.5	1	40	20	69	2	57	0.5	-	-	-	1000	250
2002 [29]	2.5	0.9	0.5	12	70	0.0056	62	-	26	-	-	149	-
2003 [30]	0.25	0.8	10	18	50	1.2	60	0.2	-	-	-	2700	450
2005 [6]	0.18	0.5	220	20	52	2.5	-	2.89	78	76	80 @ 1MHz	455	525
	0.18	0.5	150	20	62	10	-	2.0	74	81	70 @ 1MHz	2666	533
2007 [31]	0.35	0.6	0.916	15	69	0.011	65	0.014	74	53	290 @1kHz	300	382
2013 [32]	0.35	1	197	15	88	11.67	66	1.95	40	40/46	60@ 1MHz	889	148
2014 [33]	0.13	0.25	0.072	15	40	0.002	52	0.0007	-	-	3300 @-	1667	583
2015 [16]	0.065	0.5	366	3	46	38	57	43	35	37	-	623	705
	0.065	0.35	49	3	43	3.6	56	5.6	46	35	-	630	980
2015 [34]	0.18	0.9	290	17	76	7.11	72	2.98	55	48	800 @ 10kHz	463	194
2017 [7]	0.35	0.9	27	10	65	1	60	0.25	45	55	65 @ 100KHz	411	102
Contr. 1	**0.18**	**0.7**	**36.3**	**20**	**57.5**	**3**	**60**	**2.8**	**19**	**45/57**	**100 @ 1MHz**	**2361**	**2204**
Contr. 2	**0.18**	**0.7**	**76.2**	**33**	**57.7**	**2.6**	**50**	**4.6**	**14**	**43/47**	**100 @ 1MHz**	**1674**	**3155**
Contr. 3	**0.18**	**0.7**	**50.16**	**33**	**91**	**2.9**	**11**	**2.6**	**13**	**35/44**	**100 @ 1MHz**	**3155**	**2443**

Table 7: Performance comparison of Sub-1V OTAs.

3. AMPLIFIER-LESS SWITCHED CAPACITOR CIRCUITS

Switched Capacitor (SC) Circuits are one of the most commonly used type of circuits. Their versatility and suitability for being integrated have made them widely used since the early days of integrated electronics [46]. They are based on a charge transfer carried out by a charge conveyor (CC), switches and capacitors.

In traditional SC design, the CC is implemented by an OpAmp, but, as stated before, achieving proper performances in OpAmp design has become more challenging with the technological downscaling. Thus, recently, researchers try to substitute the OpAmp by other CC that do not suffer the OpAmp limitations: the so called amplifier-less techniques.

In this chapter the second line of this thesis is explored: a new differential structure for switched capacitor circuits, specially suitable for reducing low frequency noise and distortion and, thus, enhancing the dynamic range (DR) is presented.

3.1. Amplifier-less techniques.

3.1.1. Charge-Coupled devices.

One amplifier-less alternative for SC circuits is the use of charge-coupled devices (CCD) in standard CMOS technologies [47]. They were proposed by Boyle and Smith in 1970 [48] and are mainly used in imaging applications.

CCD are metal-oxide-semiconductor (MOS) structures, similar to MOS transistors, in which adjacent gates are close enough to allow channel overlapping. In Figure 35 the transversal view of a CCD structure is shown.

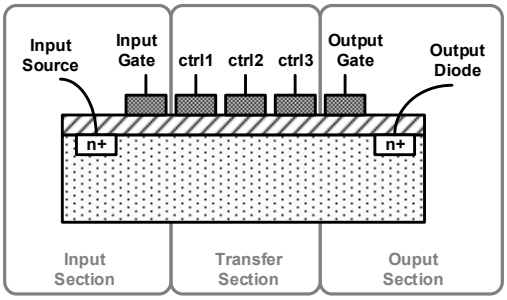


Figure 35: Transversal view of a CCD structure.

In consists of three different sections: input, transfer and output.

- *Input section*. It consist on a diffusion, and the input gate. The diffusion provides minority carriers and its potential can be controlled. The input gate potential can be turned on or off in order to allow the carriers pass from the diffusion to the input gate potential well.
- *Transfer section*. It consists on some control gates whose potential is controlled to allow the charge to pass through the structure.
- *Output section.* Consists on a reverse-biased junction capacitance. Its voltage changes depending on the amount on charge that receives. A switch resets the diode voltage after each charge transference.

Figure 36 depicts an example of how a charge transfer is carried out.

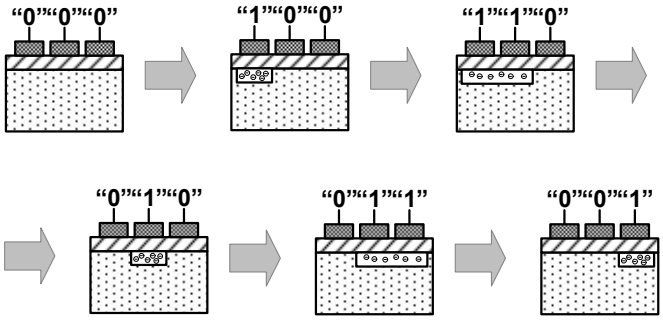


Figure 36: Charge transfer example.

CCD are used in SC circuits as they are based on charge transfer and its efficiency can be really high [47]. The main advantage of CCD structures is that they are not affected by thermal noise, charge injection or coupling from the substrate or clock but they need special process to be implemented and, usually, a high supply voltage is required for the clock signals.

3.1.2. Dynamic Amplifiers.

Another OpAmp-less technique for SC circuits substitutes the OpAmp by a group of switches that act as a dynamic amplifier [39], [49]. In charge transfer circuits, where the operation is based on a virtual ground condition, the implementation of dynamic amplifiers is straight-forward.

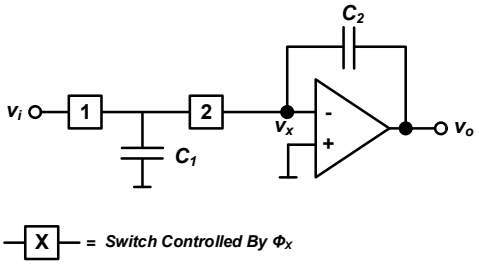


Figure 37: Classic OpAmp-based SC integrator.

In Figure 37 the classical OpAmp-based SC integrator is depicted. It is well know that the high gain and virtual ground condition of node v_x is only needed during the charge transfer phase to fully complete the charge transfer from C_1 to C_2. Thus, the OpAmp can be substituted by a dynamic amplifier as shown in Figure 38.

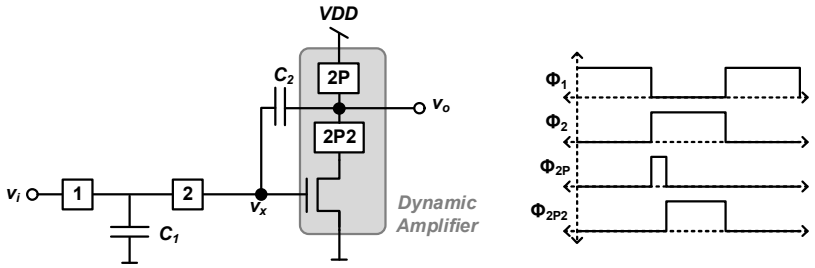


Figure 38: SC integrator with dynamic amplifier implementation.

This structure recreates the virtual ground condition on node v_x by the feedback provided by C_2 as follows: during the sampling phase, Φ_1, the capacitor C_1 receives the charge from the input, then, at the beginning of the charge transfer phase, Φ_2, the switch controlled by Φ_{2P} closes. This precharges the output node, v_o to the positive bias voltage, and, consequently, sets node v_x to a voltage higher than the M_1 threshold voltage, V_{th}. After this preset phase, the switch opens and the switch controlled by Φ_{2P2} closes, beginning the amplification phase: node v_o starts to discharge from the positive bias and, due to the capacitive coupling, the voltage at node v_x also starts to diminish. When v_x is under V_{th}, transistor M_1 is turned off and the virtual ground condition is achieved.

Even though dynamic amplifiers considerably reduce the power consumption that a OpAmp may require, there is still an analog feedback and, in fact, the output will never settle completely [50].

3.1.3. Parametric Amplifier.

In a parametric amplifier, the amplification is achieved though the variation of one circuit parameter or element [51]. For instance, in a capacitor, the voltage drop between its terminals is given by $V_{out}=Q/C$ where Q is the stored charge and C its capacitance. If it is charged to a certain value V_{in} and then the capacitance C is lowered, the voltage drop, V_{out}, increases achieving the amplification as shown in Figure 39.

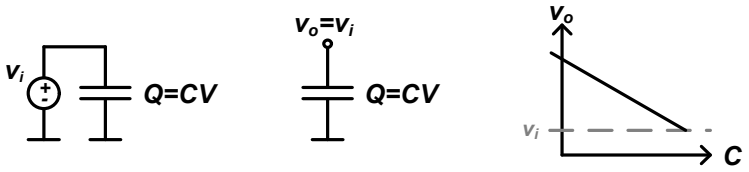


Figure 39: Parametric amplification.

A varactor can be used instead of a traditional capacitor in order to electrically control the capacitance value and apply the amplification to sampled systems such as SC [51].

3.1.4. Inverter-Based Switched Capacitors Circuits.

In SC circuits the OpAmp can also be replaced by a logic inverter [52]. Figure 40 shows the implementation of an inverter-based single-ended integrator.

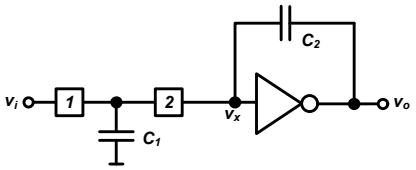


Figure 40: Inverter-Based SC integrator.

Its main advantage is that it can work under very low supply voltages. However, as the inverter only has one input terminal it is not able to provide an inherent virtual ground, instead, the node v_x is kept close to the offset voltage of the inverter. As this offset is unknown and sensitive to any process, size, supply variation, offset cancellation techniques must be implemented. Figure 41 shows an integrator with offset cancellation [52].

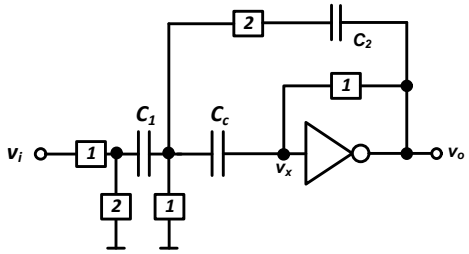


Figure 41: Inverter-Based SC integrator with offset cancellation.

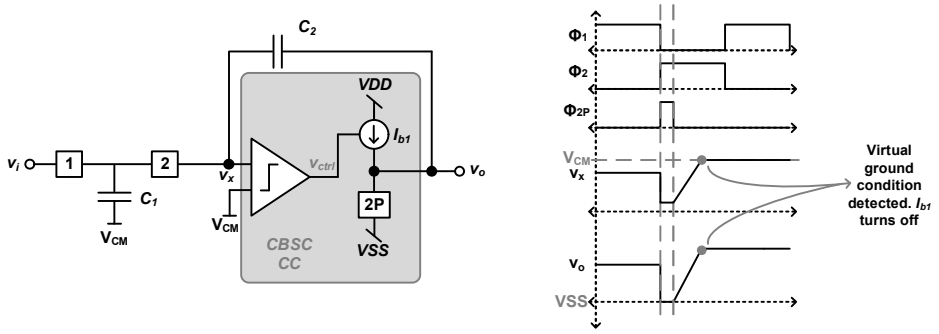
3.1.5. Comparator-Based Switched Capacitor Circuits.

In Comparator-Based SC (CBSC) circuits [53] the OpAmp is replaced by a comparator and a current source, as depicted in Figure 42 (a). As the comparator operates in open loop configuration, the requirements of gain and power consumption are substantially relaxed, but speed and accuracy are strongly related to the comparator and current source implementation.

The contribution of this chapter is based on the CBSC technique so it is explained in detail in next section.

3.2. Comparator-Based Switched Capacitors

A CBSC integrator is depicted again for reference in Figure 42 (a), as mentioned before, this technique substitutes the amplifier by a comparator and a current source. The main idea of this technique is that, for properly transfer the charge from C_1 to C_2, the CC needs to stablish a virtual ground condition on node v_x.



(a) (b)

Figure 42: (a) CBSC integrator (a) structure (b) clock phases and operation.

Hence, the comparator controls the activation of the current source, I_{b1}, responsible for the charge of the output node, v_o. At the beginning of the charge transfer phase, Φ_2, during a brief time, called preset phase, signal Φ_{P2}, Figure 42 (b), is activated so that node v_o is short-circuited to the negative bias voltage, VSS, ensuring that node v_x always starts below V_{CM}. At the end of Φ_{P2} the comparator activates the current source I_{b1}, which starts the charge of v_o. As a consequence, as v_x and v_o are capacitively coupled in an integrator, v_x increases until it equals V_{CM}. At this moment the virtual ground condition is achieved so the charge transfer is completed and the comparator turns I_{b1} off.

Let us now consider a non-ideal integrator, where the comparator has some delay and the current source is not perfectly linear. Under these realistic conditions an error in the output appears: the overshoot error, which is explained in next section.

3.2.1. Overshoot Error.

In a CBSC integrator, as the one depicted in Figure 42, due to comparator time delay, t_d, the current source, I_{b1}, will not turn off exactly when the ground condition is achieved but later. This causes the so-called overshoot error, v_{OS}, represented in Figure 43.

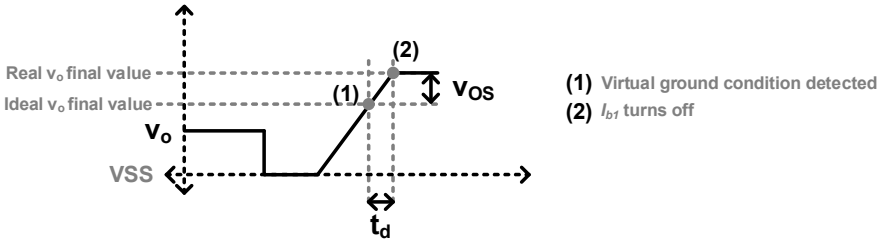


Figure 43: Overshoot Error.

The overshoot error is proportional to the current I_{b1}, as it is responsible of the slope of v_o. Thus, for a given t_d, small currents minimize v_{OS}, but it needs to be large enough to assure node v_x reaches v_{cm} during Φ_2. This implies that a compromise between speed and accuracy needs to be stablished. Moreover, since the current source is not completely lineal, the overshoot is going to introduce distortion.

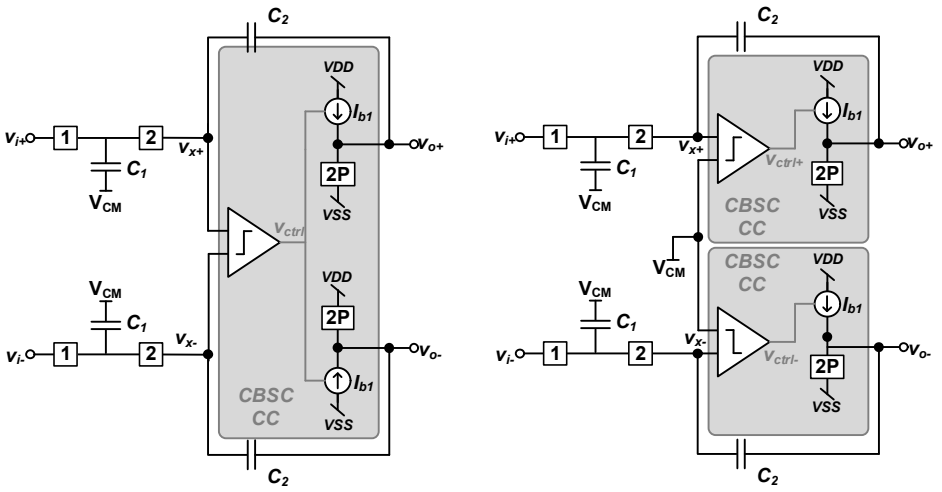
In order to overcome this error, in [53] authors propose the use of two current sources: the first one, larger, provides the speed but implies large overshoot error, and the other one, smaller, is activated later to reduce the overshoot. In [54] and [55] authors make use of variable current sources to improve speed while maintaining accuracy. Other contributions, such as modifying the charging algorithm [56], [57], using hybrid schemes [58] or dynamic comparators [59] have been proposed to further improve the performances and overcome the speed-accuracy compromise.

In addition, some works present differential implementations, [60]–[63], as they have the advantages of double signal swing, extrinsic noise and common mode rejection and linearity enhancement among others. Moreover, in SC circuits, charge injection issues are greatly reduced [64].

In the next section, differential CBSC implementations are discussed.

3.2.2. Differential CBSC Implementation.

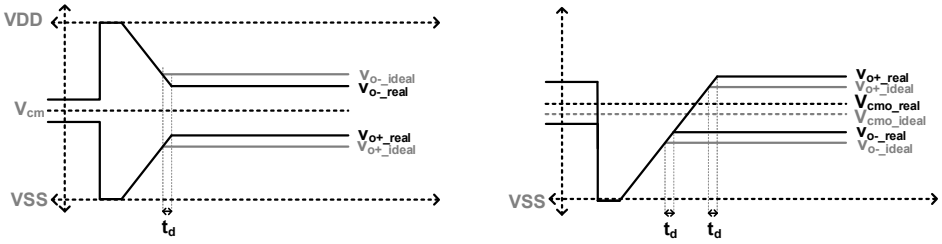
As in the traditional OpAmp-based SC circuits, a differential implementation can be carried out in different ways: Fully-Differential (F-D) and Pseudo-Differential (P-D). In Figure 44 the differential CBSC integrators are depicted.



(a) (b)

Figure 44: (a) F-D and (b) P-D CBSC integrators.

The F-D implementation of Figure 44(a) uses a SE comparator to generate both outputs, v_{o+} and v_{o-}. At the beginning of the charge transfer phase, Φ_2, the outputs v_{o+} and v_{o-} are pushed to the supply rails, *VSS* and *VDD*, respectively, during the preset phase, Φ_{2P}. Then, both current sources are turned on and when v_{x+} crosses v_{x-} they are turned off. Due to the comparator time delay, the current sources are not closed immediately and some overshoot error happens. This overshoot error is a differential error in F-D CBSC structures, as it can be observed in Figure 45(a).



(a) (b)

Figure 45: Output signals evolution in (a) F-D and (b) P-D CBSC integrators.

On the contrary, in P-D structures (Figure 44(b)), during the present phase, v_{o+} and v_{o-} are both pushed to the same voltage value, *VSS*, and, when the current sources are turned on they both charge the output nodes in the same direction until v_{x+} and v_{x-} reach v_{cm}, as it can be observed in Figure 45(b). In this case, the overshoot error leads to a common mode error, than can be easily removed by a common mode control circuit. As it is easier to eliminate common mode errors than differential errors, the pseudo-differential implementation is usually preferred [63].

3.3. Contribution.

3.4. Conclusions.

4. CONCLUSIONS AND FUTURE WORK

Throughout this thesis two different design philosophies that have arisen in the context of deeply scaled analog integrated electronics have been undertaken.

First, on Chapter 2, three multistage bulk-driven OTA that share the same proposed low-voltage non-tailed differential input stage were proposed. When compared with other sub-1V amplifiers, the proposed OTAs outstand the state of the art.

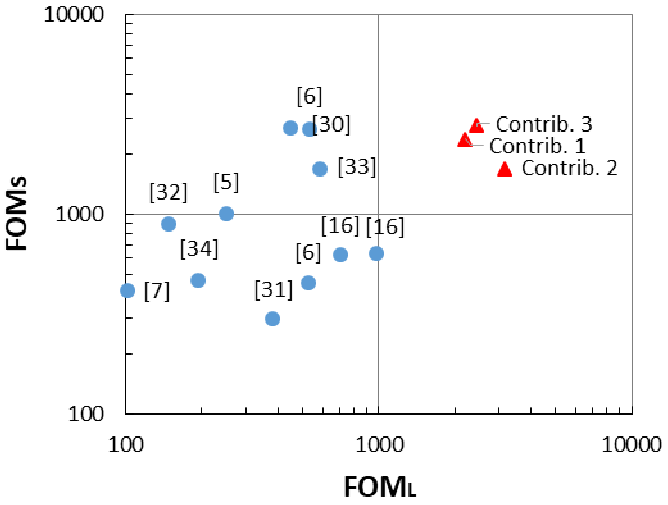


Figure 46: FOMs Vs FOML of Sub-1V OTAs.

Despite the competitive results, there is still place for further improvement. Firstly, the amplifiers may be refabricated in order to overcome the limitation of a non-controlled fabrication. Secondly, the design of a fully-differential version. But, among all the future work, enhancing the parameters that have obtained less satisfactory results may be a priority. In this line, a new input stage with CMRR

improvement shall be developed.

On Chapter 3, amplifier-less switched-capacitor circuits were studied and a new differential technique that intrinsically reduces noise and distortion is proposed.

REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits (Reprinted from Electronics, pg 114-117, April 19, 1965)," *Proc. Ieee*, vol. 86, no. 1, pp. 82–85, Sep. 1965.

[2] A. J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, 2005.

[3] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proc. IEEE*, vol. 97, no. 10, pp. 1687–1714, Oct. 2009.

[4] P. E. Allen, D. R. Holberg, and Allen, *CMOS Analog Circuit Design*. Oxford University Press, 2002.

[5] T. Lehmann and M. Cassia, "1-V power supply CMOS cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1082–1086, Jul. 2001.

[6] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, 2005.

[7] A. D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "0.9-V Class-AB Miller OTA in 0.35-μm CMOS With Threshold-Lowered Non-Tailed Differential Pair," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 64, no. 7, pp. 1740–1747, 2017.

[8] P. Monsurro, G. Scotti, A. Trifiletti, and S. Pennisi, "Biasing technique via bulk terminal for minimum supply CMOS amplifiers," *Electron. Lett.*, vol. 41, no. 14, pp. 779–780, 2005.

[9] A. D. Grasso, P. Monsurro, S. Pennisi, G. Scotti, and A. Trifiletti, "Analysis and Implementation of a Minimum-Supply Body-Biased CMOS Differential Amplifier Cell," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 17, no. 2, pp. 172–180, Feb. 2009.

[10] P. Monsurro, S. Pennisi, G. Scotti, and A. Trifiletti, "Exploiting the Body of MOS Devices for High Performance Analog Design," *IEEE Circuits Syst. Mag.*, vol. 11, no. 4, pp. 8–23, 2011.

[11] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE J. Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, Jun. 1977.

[12] T. M. Hollis, D. J. Comer, and D. T. Comer, "Optimization of MOS amplifier performance through channel length and inversion level selection," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 52, no. 9, pp. 545–549, Sep. 2005.

[13] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 6, pp. 1453–1462, 2015.

[14] Y. Tsividis, *Operation and Modeling of the Mos Transistor (The Oxford Series in Electrical and Computer Engineering)*. Oxford University Press, 2004.

[15] Y. Li, C. C. Y. Poon, and Y. T. Zhang, "Analog Integrated Circuits Design for Processing Physiological Signals," *IEEE Rev. Biomed. Eng.*, vol. 3, pp. 93–105, 2010.

[16] O. Abdelfattah, G. W. Roberts, I. Shih, and Y. C. Shih, "An Ultra-Low-Voltage CMOS Process-Insensitive Self-Biased OTA With Rail-to-Rail Input Range," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 10, pp. 2380–2390, Oct. 2015.

[17] G. Di Cataldo, A. D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "CMOS Non-tailed differential pair," *Int. J. Circuit Theory Appl.*, vol. 44, no. 7, pp. 1468–1477, 2016.

[18] F. Centurelli, P. Monsurro, S. Pennisi, G. Scotti, and A. Trifiletti, "Design Solutions for Sample-

and-Hold Circuits in CMOS Nanometer Technologies," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 56, no. 6, pp. 459–463, 2009.

[19] J. Ramirez-Angulo, S. C. Choi, and G. Gonzalez-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 42, no. 11, pp. 971–974, Nov. 1995.

[20] J. Ramirez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "Low-voltage CMOS op-amp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple-input floating-gate transistors," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 48, no. 1, pp. 111–116, 2001.

[21] J. Ramirez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, and F. M. Chavero, "Very low-voltage analog signal processing based on quasi-floating gate transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 434–442, 2004.

[22] E. Cabrera-Bernal, C. Lujan-Martinez, R. G. Carvajal, and J. Ramirez-Angulo, "Limitations of CAD Tools for Modeling Transistors that Implement Large Resistors," in *2012 XXVII Conference On Design of Circuits and Integrated Systems(DCIS)*, 2012.

[23] M. Wang, T. L. Mayhugh, S. H. K. Embabi, and E. Sanchez-Sinencio, "Constant-gm rail-to-rail CMOS op-amp input stage with overlapped transition regions," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 148–156, Feb. 1999.

[24] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, 1994.

[25] L. Moldovan and H. H. Li, "A rail-to-rail, constant gain, buffered op-amp for real time video applications," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 169–176, Feb. 1997.

[26] G. Ferri and W. Sansen, "A rail-to-rail constant-g/sub m/ low-voltage CMOS operational transconductance amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 10, pp. 1563–1567, Oct. 1997.

[27] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1364–1372, 2003.

[28] J. M. Carrillo, G. Torelli, M. A. Dominguez, and J. F. Duque-Carrillo, "On the input common-mode voltage range of CMOS bulk-driven input stages," *Int. J. Circuit Theory Appl.*, vol. 39, no. 6, pp. 649–664, 2011.

[29] T. Stockstad and H. Yoshizawa, "A 0.9-V 0.5-μA rail-to-rail CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 286–292, Mar. 2002.

[30] L. Yao, M. Steyaert, and W. Sansen, "A 0.8-V, 8-μW, CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load," in *ESSCIRC 2004 - 29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705)*, 2003, pp. 297–300.

[31] L. H. C. Ferreira, T. C. Pimenta, and R. L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, no. 10, pp. 843–847, Oct. 2007.

[32] L. Zuo and S. K. Islam, "Low-Voltage Bulk-Driven Operational Amplifier With Improved Transconductance," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 60, no. 8, pp. 2084–2091, 2013.

[33] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 61, no. 6, pp. 1609–1617, 2014.

[34] N. Tang, W. Hong, J. H. Kim, Y. Yang, and D. Heo, "A Sub-1-V Bulk-Driven Opamp With an Effective Transconductance-Stabilizing Technique," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 62, no. 11, pp. 1018–1022, Nov. 2015.

[35] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2074–2079, Nov. 2004.

[36] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1514–1520, 2005.

[37] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in Reversed Nested Miller Compensation," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 7, pp. 1459–1470, 2007.

[38] J. Lemus-LóPez, A. DíAz-Sánchez, C. Muniz-Montero, J. RamíRez-Angulo, J. M. Rocha-PéRez, and L. A. SáNchez-Gaspariano, "High gain amplifier with enhanced cascoded compensation," *Radioengineering*, vol. 23, no. 1, pp. 504–511, 2014.

[39] B. J. Hosticka, "Dynamic CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 15, no. 5, pp. 881–886, Oct. 1980.

[40] A. D. Grasso, G. Palumbo, and S. Pennisi, "High-Performance Four-Stage CMOS OTA Suitable for Large Capacitive Loads," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 10, pp. 2476–2484, Oct. 2015.

[41] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 45, no. 7, pp. 769–780, Jul. 1998.

[42] W. Aloisi, G. Palumbo, and S. Pennisi, "Design methodology of Miller frequency compensation with current buffer/amplifier," *IET Circuits, Devices Syst.*, vol. 2, no. 2, pp. 227–233, 2008.

[43] J. Zhou and J. Liu, "On the measurement of common-mode rejection ratio," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 52, no. 1, pp. 49–53, 2005.

[44] M. K. Gill and A. Agarwal, "A Test Methodology to Measure the Open-Loop Voltage Gain of an Operational Amplifier," *Int. J. Electr. Comput. Energ. Electron. Commun. Eng.*, vol. 11, no. 2, pp. 167–170, 2017.

[45] A. Devices, "Op Amp Common-Mode Rejection Ratio (CMRR)," (*Tutorial)*. pp. 1–4.

[46] K. R. Stafford, P. R. Gray, and R. A. Blanchard, "A Complete Monolithic Sample/Hold Amplifier," *IEEE J. Solid-State Circuits*, vol. 9, no. 6, pp. 381–387, 1974.

[47] S. A. Paul, H. S. Lee, J. Goodrich, T. F. Alailima, and D. D. Santiago, "Nyquist-rate pipelined oversampling A/D converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1777–1787, 1999.

[48] W. S. Boyle and G. E. Smith, "Charge Coupled Semiconductor Devices," *Bell Syst. Tech. J.*, vol. 49, no. 4, pp. 587–593, 1970.

[49] M. A. Copeland and J. M. Rabaey, "Dynamic amplifier for m.o.s. technology," *Electron. Lett.*, vol. 15, no. 10, pp. 301–302, May 1979.

[50] H. S. Lee, L. Brooks, and C. G. Sodini, "Zero-Crossing-Based Ultra-Low-Power A/D Converters," *Proc. IEEE*, vol. 98, no. 2, pp. 315–332, Feb. 2010.

[51] S. Ranganathan and Y. Tsividis, "Discrete-time parametric amplification based on a three-terminal MOS varactor: analysis and experimental results," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2087–2093, 2003.

[52] Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.

[53] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, 2006.

[54] K. F. Wong, S. W. Sin, U. Seng-Pan, and R. P. Martins, "Level-shifting variable current charging technique for high-speed Comparator-Based Switched-Capacitor circuits," in *Midwest Symposium on Circuits and Systems*, 2010, pp. 566–569.

[55] M. Zamani, M. Dousti, and A. H. A. Nohoji, "A10-bit, 20-MS/s, fully differential single transfer phase CBSC pipelined ADC in 0.18 μm CMOS," in *2011 International Conference on Electronic Devices, Systems and Applications (ICEDSA)*, 2011, pp. 77–82.

[56] J. K. Woo, T. H. Kim, H. Lee, S. Kim, H. Lee, and S. Kim, "A comparator-based cyclic analog-to-digital converter with boosted preset voltage," in *IEEE/ACM International Symposium on Low Power Electronics and Design*, 2011, pp. 199–204.

[57] K. F. Wong, S. W. Sin, S. P. U, and R. P. Martins, "A modified charging algorithm for comparator-based switched-capacitor circuits," in *2009 52nd IEEE International Midwest Symposium on Circuits and Systems*, 2009, pp. 86–89.

[58] M. A. Martins, K. F. Un, P. I. Mak, and R. P. Martins, "SC biquad filter with hybrid utilization of OpAmp and comparator-based circuit," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, 2010, pp. 1276–1279.

[59] K. Yamamoto and A. Carusone, "A 1-1-1-1 MASH delta-sigma modulator with dynamic comparator-based OTAs," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1866–1883, 2012.

[60] D. Prelog, M. Momeni, B. Horvat, and M. Glesner, "Cascade delta-sigma modulator with pseudo-differential comparator-based switched-capacitor gain stage," *Analog Integr. Circuits Signal Process.*, vol. 51, no. 3, pp. 201–206, Jun. 2007.

[61] L. Brooks and H. S. Lee, "A 12b, 50 MS/s, Fully Differential Zero-Crossing Based Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3329–3343, 2009.

[62] M. C. Huang and S. I. Liu, "A fully differential comparator-based switched-capacitor ΔΣ modulator," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 56, no. 5, pp. 369–373, May 2009.

[63] K. Cornelissens and M. Steyaert, "Comparator-Based Switched-Capacitor Delta-Sigma A/D Converters," in *Analog Circuit Design: Robust Design, Sigma Delta Converters, RFID*, H. Casier, M. Steyaert, and A. H. M. van Roermund, Eds. Dordrecht: Springer Netherlands, 2011, pp. 157–176.

[64] B.Razavi, *Design of analog CMOS integrated circuits*, 1st ed. New York, NY, USA: McGraw-Hill, Inc., 2001.

[65] K. R. Laker, "Equivalent Circuits for the Analysis and Synthesis of Switched Capacitor Networks," *Bell Syst. Tech. J.*, vol. 58, no. 3, pp. 729–769, 1979.

[66] R. Schreier and G. C. Temes, *Understanding delta-sigma data converters*. New York, NY: Wiley, 2005.

[67] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.

[68] M.-H. Tsai and T.-P. Ma, "The impact of device scaling on the current fluctuations in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2061–2068, Nov. 1994.

[69] E. Simoen and C. Claeys, "On the flicker noise in submicron silicon MOSFETs," *Solid. State. Electron.*, vol. 43, no. 5, pp. 865–882, 1999.

[70] T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Noise Analysis for Comparator-Based

Circuits," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 56, no. 3, pp. 541–553, 2009.

[71] K. L. Lee and R. G. Mayer, "Low-distortion switched-capacitor filter design techniques," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1103–1113, 1985.

[72] K. Yamamoto, "A 1-1-1-1Mash Delta-Sigma ADC Using Dynamic Comparator-Based OTAs," University of Toronto, 2012.

[73] E. López-Morillo, R. G. Carvajal, F. Munoz, H. El Gmili, A. Lopez-Martin, J. Ramirez-Angulo, and E. Rodríguez-Villegas, "A 1.2-V 140-nW 10-bit sigma-delta modulator for electroencephalogram applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 223–230, Sep. 2008.

[74] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 50, no. 3, pp. 352–364, Mar. 2003.

[75] J. M. de la Rosa and R. Rio, *CMOS Sigma-Delta Converters: Practical Design Guide*. Wiley, 2013.

[76] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, 1999.

[77] H. Tian and A. El Gamal, "Analysis of 1/f noise in switched MOSFET circuits," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 48, no. 2, pp. 151–157, Feb. 2001.

APPENDIX A

APPENDIX B

APPENDIX C

APPENDIX D

In this appendix the publications of the author of this thesis are attached for reference.

1. E. Cabrera-Bernal, C. Lujan-Martinez, R. G. Carvajal, and J. Ramirez-Angulo, "Limitations of CAD Tools for Modeling Transistors that Implement Large Resistors," in *2012 XXVII Conference On Design of Circuits and Integrated Systems(DCIS)*, 2012.
2. E. Cabrera-Bernal, S. Pennisi, and A. D. Grasso, "Bulk-Driven Three-Stage Class-AB CMOS OTA," in *2014 XXIX Conference On Design of Circuits and Integrated Systems(DCIS)*, 2014.
3. E. Cabrera-Bernal, S. Pennisi, and A. D. Grasso, "0.7-V bulk-driven three-stage class-AB OTA," in *2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS)*, 2015, pp. 1–4
4. E. Cabrera-Bernal, S. Pennisi, A. D. Grasso, A. Torralba, and R. G. Carvajal, "0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 63, no. 11, pp. 1807–1815, Nov. 2016.

Limitations of CAD Tools for Modeling Transistors that Implement Large Resistors

E. Cabrera-Bernal, C. Lujan-Martinez
and R.G. Carvajal
Electronic Engineering Department
University of Seville
Seville, Spain
{elena.cabrera, clara.lujan, carvajal}@gie.esi.us.es

J. Ramirez-Angulo
Klipsch School of Electrical Engineering
New Mexico State University
Las Cruces (New Mexico) USA
jramirez@nmsu.edu

Abstract— **The QFG technique has proven to be very effective for low power and low voltage analog design with a moderate increase in the circuit area thanks to the implementation of pseudo-resistors by means of MOS transistors in the cut-off region. However, the implementation of these pseudoresistors introduces some parasitic effects whose study is required to prevent undesired dynamics, or to take profit of these structures in some other applications with extremely slow time behavior. In this paper, a study of the accuracy of the CAD tools to model certain structures based on transistors in the cutoff region is presented. A comparison between simulations and measurements shows the need of a simple but reliable model for this kind of structures.**

Keywords- Low power; low voltage; biomedical applications; Quasi-floating gate (QFG) transistors; CAD tools

I. INTRODUCTION.

Nowadays, handheld electronic devices have acquired huge importance in modern lifestyle. From mobile phones to personal laptops, the requirement of low power and low voltage is compulsory to extend the battery lifetime.[1]

In biomedical applications, the need of ambulatory monitoring is undisputable as it allows long-term patient monitoring, reduces their hospitalization costs and provides trustable data as they are acquired during their normal daily activity. However, these devices have been traditionally rather uncomfortable and aesthetic leading patients to stay at home during the tests. As a consequence, the accuracy of diagnosis is crippled by the unrealistic conditions of the data acquisition.

Thus, the design of truly miniaturized wearable devices is a current challenge for this kind of applications where the stringent requirements of size, weight, battery lifetime and performance imply a great effort on low power and low voltage electronic design. The interest of the scientific community is clearly reflected in recent literature [1], [2].

The first stage of biomedical signal acquisition is the sensor; hence, the sensor interface is a critical block, as it has to provide to the next processing stages a clear input signal.

This work was financed by the Spanish Ministry of Economy and Competitiveness under project TEC2011-28724-C03-01 and the Andalousian "Consejería de Economía, Innovación y Ciencia" under project TIC-6323

Biomedical signals are usually characterized by extremely low frequency and generally very low amplitude. Nevertheless, they usually introduce an unknown and appreciable dc offset, due to some electrochemical effects that takes place between sensor and organic tissues. These facts pose a complex problem, as it is indispensable to filter the large dc offset (as it can lead to severe problems in the signal processing) while maintaining the low-frequency signals unfiltered. This results in the use of extremely low cut-off frequency high pass filters. Moreover, integrating large passive resistors or capacitors to implement those low cut off frequency filters in existing MOS technologies is not feasible.

Recently, the high pass filtering capability of the Quasi-Floating Gate (QFG) technique has been highlighted in [3], where an extremely low cutoff frequency was achieved by means of an extremely high resistor implemented by a MOSFET transistor working in subthreshold or cutoff region. In addition, QFG transistors have been successfully used in a number of different, not only biomedical, applications as stated in [4], [5]. In the field of biomedical sensor interfacing, some contributions based on these pseudo-resistors have been also proposed [6], [7].

However, in [8] a time dependency of the DC voltage on some structures, that used these pseudo-resistors, was reported. From the results published in the literature these problems seem to be related to the implementation of the pseudoresistors.

Although this voltage drift is not a serious problem, as it can be easily overcome, a detailed study of this drift highlights the lack of fair modeling present CAD simulators when working with transistors in cutoff region. With a proper model this voltage drift could be anticipated and corrected. Even in certain cases some profit could be taken from it for some applications that require extremely slow time dynamics.

This deficiency in transistor modeling makes the design work quite complicated, as simulation results are unreliable.

In this paper a thorough study of different ways to use circuit simulators with transistors working in cutoff region is presented. In section II, the QFG transistor technique is reviewed. In section III, two selected implementations of pseudo-resistors for a test circuit used in this study are presented. In section IV, some simulation techniques and their

results are presented. Later, in section V, measurement results are compared to simulation ones. Finally, in section VI, some conclusions are drawn.

II. QFG TRANSISTORS.

Theoretical foundation and practical aspects of the QFG transistors are presented in [3]. They are MOSFET transistors whose gates are capacitively coupled to the inputs as shown in Figure 1. Moreover, a very large resistor connects the gate to a dc bias voltage. Hence, as the gate is not really floating, they are called quasi-floating gate transistors (Fig. 1).

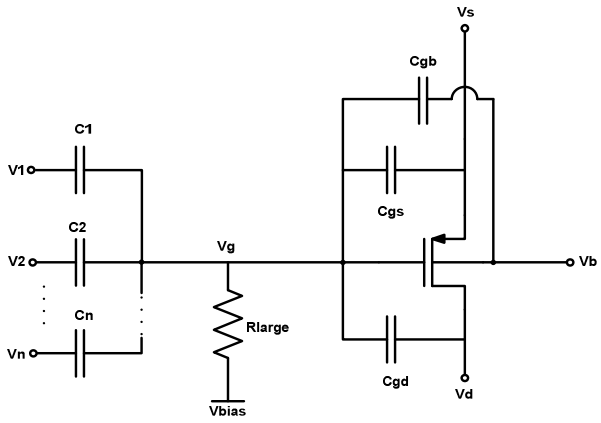


Figure 1. QGF transistor.

This simple structure allows gate biasing while filtering the inputs dc level. Thus, in the gate of the transistor we have the weighted sum of the ac component of the inputs plus the desired bias voltage established through the large resistor. This is important for sensor interface, as it filters out the non-desired dc offset of the input signals.

III. TEST CIRCUIT AND PSEUDORESISTORS

A. Test circuit.

For testing purposes two pseudoresistors will be used in the simple voltage follower depicted in Fig. 2, where Rlarge is replaced by the selected pseudoresistor implementation. This circuit has been chosen because the voltage drift in the pseudoresistor can be easily measured in the circuit output.

The circuit shown in Figure 2 consists of two simple and identical voltage followers. The first one has a QFG transistor with a pseudoresistor at the input terminal, while the latter do not. The principle of operation is quite simple: the outputs v_{o1} and v_{o2} will follow *M1* and *M*2 gate voltage respectively, with an ideal voltage gain of 1. In this circuit v_1 is the bias voltage while v_2 is a sinusoidal input signal. Consequently, the circuit allows the differences between the QFG follower dc output (v_{o1}) and the classical follower dc output (v_{o2}) to be easily observed.

Concerning the pseudoresistor implementation many different structures can be found in the literature [6], [7]. In this paper two simple pseudo-resistor implementations have beenchosen, as their simplicity will facilitate the development of basic circuit models. Comparing simulated to experimental results obtained with the proposed structure will provide an in-depth understanding of the physical phenomena that occur in the devices components and in their implementation. From these results new powerful models could be developed for more complex structures.

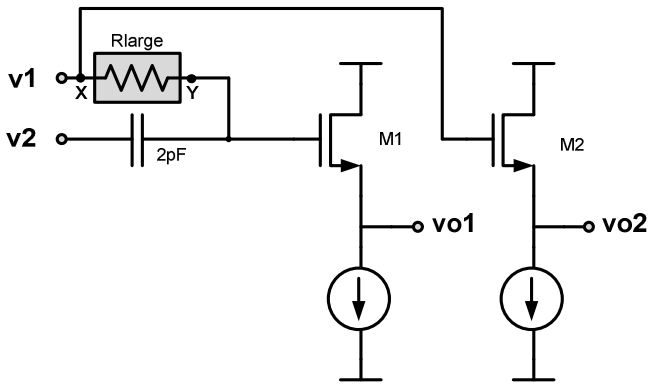
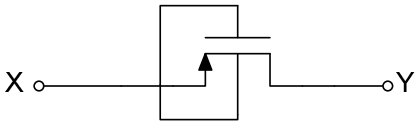


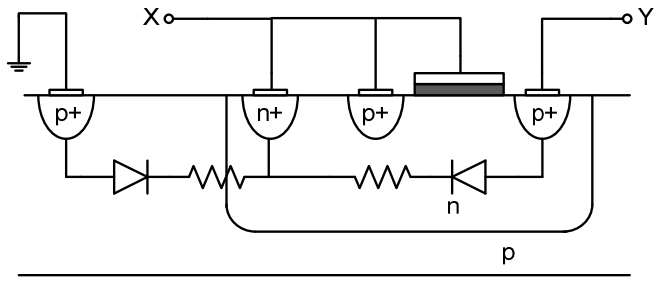
Figure 2. Test circuit, voltage follower.

B. Pseudoresistor 1

In Fig. 3, the first pseudoresistor implementation is shown. As the gate node is connected to the source node, no transistor channel is created. In addition, in our test circuit (Fig. 2), the PN junction between source and drain is always reverse biased, as node *X* always has a voltage higheror equal than node *Y*, so the current flowing through the structure is expected to be quite small. For all these reasons, pseudo-resistor 1 is expected to present a huge ohmic value.



(a)



(b)

Figure 3. Pseudoresistor 1. (a) Symbol. (b) Physical structure.

C. Pseudoresistor 2

In Fig. 4, the second pseudoresistor structure considered in this paper is shown. Just like in Pseudoresistor 1, no channel

can be created, as gate and source nodes are connected together, so a very small current flow is expected through the transistor channel. However, as in our test circuit (Fig. 2) the PN junction between node *X* and node *Y* will always be forward biased, a higher value of the current through this structure is now expected in comparison to Pseudoresistor 1 implementation.

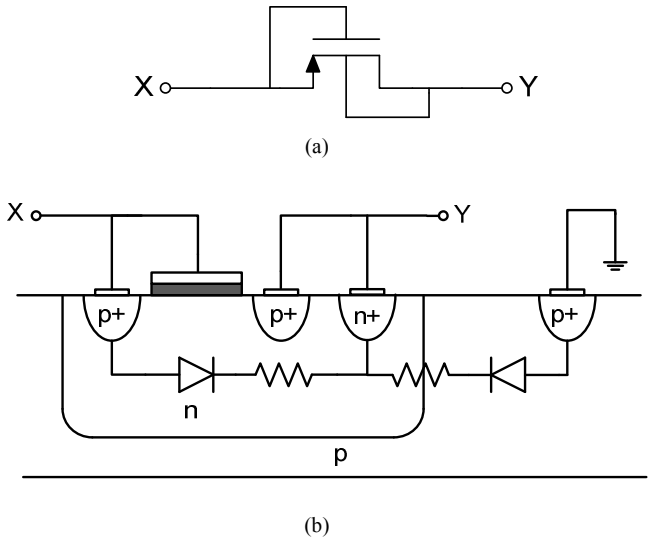


Figure 4. Pseudoresistor 2. (a) Symbol. (b) Physical structure.

IV. SIMULATION TECHNIQUE AND RESULTS

In this section some particularities, difficulties and solutions encountered while simulating this kind of circuits are detailed. All the simulations have been done in Cadence and for a standard 0.5µm CMOS technology.

A. High precision simulation technique.

Considering that we are trying to simulate structures that deal with extremely low current values, standard simulation precision parameters must be modified, as high precision is required to compute those current values. In our study, relative convergence criterion (reltol) is set to 1e-6, voltage and current absolute tolerance convergence criterion (vabstol, iabstol) are set to 1e-9 and 1e-15, respectively, and minimum conductance across all semiconductor junctions (gmin) is set to 1e-18.

These parameter values will usually lead to convergence problems that could be solved by relaxing the simulation precision, at the cost of imprecise simulations. However, these convergence problems have been solved by facilitating the computation of the operating point to the simulator by means of ramp-up simulation.

B. Ramp-up simulation technique.

As it was described above, the simulator will present convergence problems when changing the convergence parameters. Furthermore, as we are trying to simulate transient phenomena, we must emulate, as far as possible, the real circuit behavior.

For all this, every independent current and voltage source were simulated using Piece Wise Linear (pwl) sources. Using these sources we are able to set all circuit excitation to zero at the beginning of the simulation and, after a brief period of time, set them to their final values following an rising ramp, in a way similar to what it is expected when the power source of a real circuit is switched on.

In addition, pwl sources facilitate the operating point computation as, at the beginning of the simulation, all voltages and currents are equal to zero.

Although Cadence offers the possibility of running an automatic ramp-up simulation, using pwl sources have the advantage of providing more controllable simulation parameters.

C. Simulation time.

First of all, note that the circuits to be simulated have very large time constants. As a consequence, in order to see the full transient behavior, a long period of time must be simulated. It leads to large simulation files that could run computers out of memory. Fortunately, in Cadence, just a limited amount of data can be managed when plotting simulation result. Then, to avoid these problems, neither circuit node voltage nor branch currents must be saved. Instead of that, AHDL code have been used to save into a text file the average voltage of the signals of interest in the test circuit shown in Fig. 2, which are v_{o1} and v_{o2} in this case. Later, these text files are processed using MatLab.

D. Simulation results.

Simulation results are now presented. As we are only interested in the dc voltage drift, for these simulations, v_1 is the bias voltage while v_2 is also a dc source. In the following graphs the dc voltage of the outputs v_{o1} and v_{o2} are represented.

1) Pseudoresistor 1.

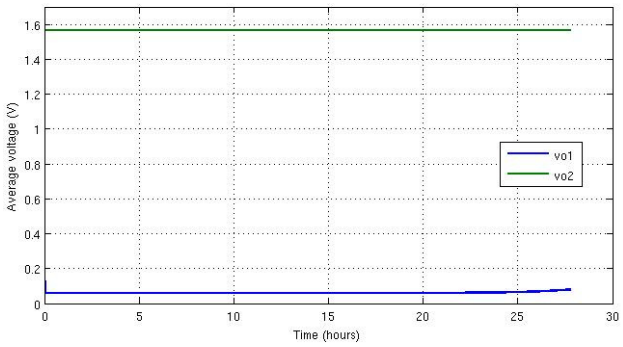


Figure 5. Pseudoresistor 1 simulation results.

2) Pseudoresistor 2.

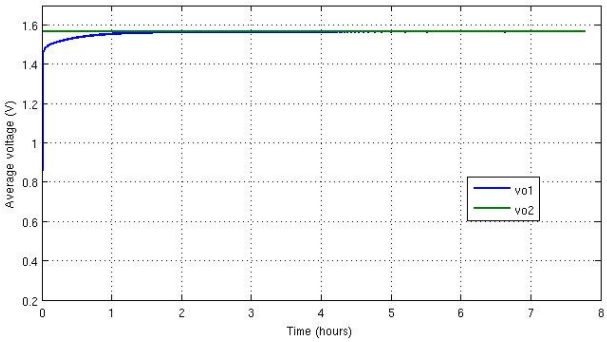


Figure 6. Pseudoresistor 2 simulation results.

Unfortunately these simulations require such an amount of time to be completed that it is not usually handy. As we are only interested in the dc voltage and the transient dynamic is slow enough, one way to accelerate the simulations is to increase the transient simulation step. Simulation results obtained this way are shown below, where the simulation transient time step was artificially set to 0.02s.

3) *Pseudoresistor 1*

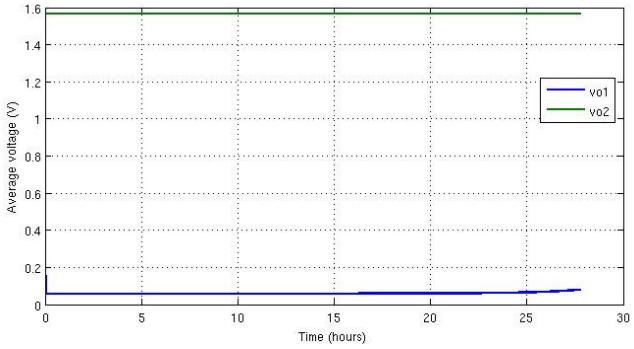


Figure 7. Pseudoresistor 1 simulation results using a large transienttime step.

4) *Pseudoresistor 2.*

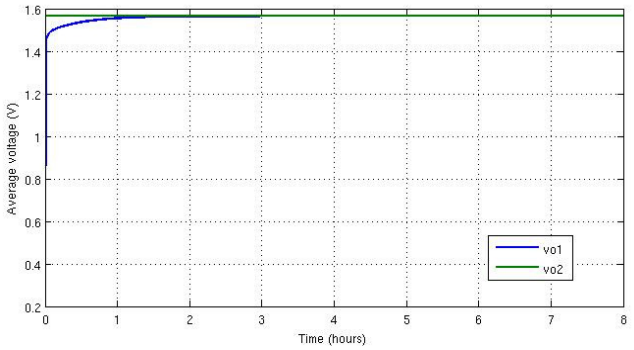


Figure 8. Pseudoresistor 2 simulation results using a large transient time step.

It can be observed that both simulations with standard, self-adjusted, and with large, fixed transient timesteps, approximately provide the same results. Then, whenever it is possible, selecting a time step as big as possible is the first solution to be tried for faster simulation of the dc voltage drift. How big? This question is no easy to answer. In our case we obtained a proper value by a trial and error procedure.

V. MEASUREMENT TECHNIQUE AND RESULTS

In order to test the accuracy of the simulations, the test circuit was laid out and sent for fabrication and some measurement results are presented here.

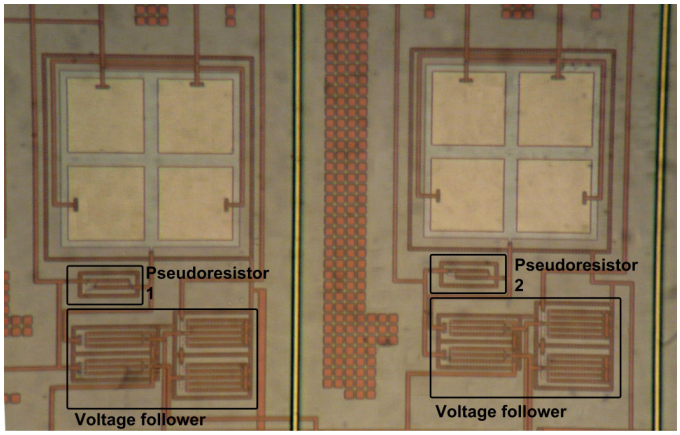


Figure 9. Microphotograph of the chip..

As the measurement of these circuits takes a long period of time, an automated measurement technique has been used. The circuit outputs are taken to an oscilloscope, which is connected to a computer with LabView programmed to take periodic measurements and to save them to a text file. Later, these files are processed using MatLab.

Measurements results are shown below.

1) *Pseudoresistor 1.*

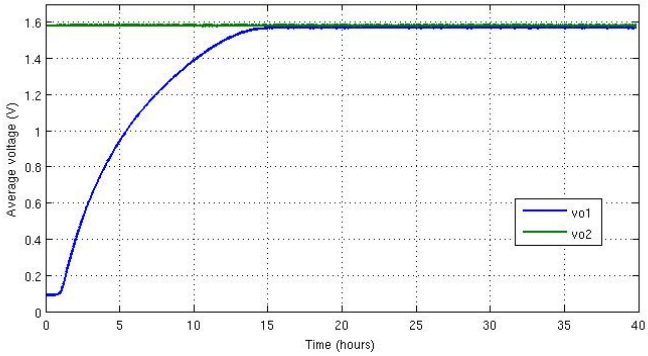


Figure 10. Pseudoresistor 1 experimental results.

It can be observed that the experimental results do not match with simulation results, as the experimentally measured time constant is rather lower than that obtained by simulation. This fact highlights that simulators are not able to reproduce real circuit behavior, as MOS transistors working in cut-off are not properlymodeled.

2) Pseudoresistor 2.

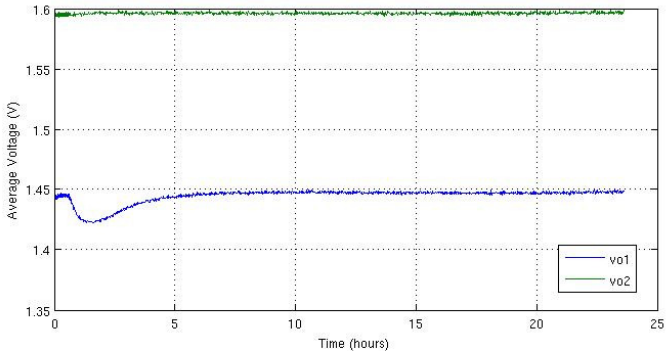


Figure 11. Pseudoresistor 2 experimental results.

Once again, it can be observed that the experimental results do not match with those obtained by simulation. In this pseudoresistor, not only the time constant is different, there are also certain transient dynamic effects clearly visible in the experimental measurements which do not appear in the simulations. Once again, it can be concluded that the simulation model for the MOSFET working in the cutoff region is not accurate.

VI. CONCLUSIONS

Circuits containing pseudoresistors implemented by transistors working in the cutoff region have shown to be extremely useful and versatile in many low power and low voltage applications. As a consequence, a thorough study of the transient behavior of different implementations of pseudoresistor implementations is required.

It has been revealed that many effects that are usually ignored when the transistors are working in active regions cannot be neglected when working in cutoff region. The study presented in this paper reveals the lack of a reliable model provided by standard simulators and highlights the need of developing a trustable model in order to gain an in-depth understanding of its behavior, in order to be able to control and exploit it. This is especially important for deep submicron technologies where additional effects such as drain and gate leakage could change the dynamic behavior of these pseudoresistors.

The study presented here also addresses the problem associated to the long simulation times required by these structures, due to their extremely large time constants.

Presently, from the results presented here, an accurate and simple model for the transient behavior of these circuits is being developed, and new algorithms and methods to control them in a predictable way are being devised.

REFERENCES

[1] A. J. Casson, S. Smith, J. S. Duncan, and E. Rodriguez-Villegas, "Wearable EEG: what is it, why is it needed and what does it entail?,"in *Proc. of the 30th Annual International IEEE EMBS Conference,* Vancouver, British Columbia, Canada, Aug. 20-24, 2008.

[2] P. Corbishley and E.Rodriguez-Villegas, "A Nanopower Bandpass Filter for Detection of an Acoustic Signal in a Wearable Breathing Detector,"*IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no.3, Sep.2007.

[3] J. Ramirez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, and F. Muñoz-Chavero, "Very low voltage analog signal processing based on quasi floating gate transistors," *IEEE J. Solid State Circuits,* vol. 39, no. 3,pp. 434–442, Mar. 2004

[4] A. Torralba Silgado, C. I. Luján Martínez, R.Gonzalez Carvajal, Juan Antonio Gómez Galán, J. Galán, et. al."Tunable Linear MOS Resistors Uusing Quasi-Floating-Gate Techniques". *IEEE Transactions on Circuits and Systems II-Express*, vol. 56,no. 1, pp. 41-45, 2009.

[5] E. López Morillo, R.Gonzalez Carvajal, J.A. Gómez Galán, Hakim Elgmili, Jaime Ramírez Angulo, et. al. "A Very Low-Voltage Low-Power QFG-Based Sigma-Delta Modulator for Electroencephalogram Applications," in *Proc. of the XXI Conference on Design of Circuits and Integrated Systems. Conference on Design of Circuits and Integrated Systems*, no. 21. Barcelona. Departamento de Electrónica. 2006. Pag. 210-215

[6] R.R. Harrison and C. Charles "A low-Power, Low-Noise CMOS amplifier for neural Recording Application," *IEEE J. Solid State Circuits,* vol. 38, no. 6, 2003.

[7] X. Zou, X. Xu, L. Yao, Y. Lian "A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip,"*IEEE Journal of Solid-State Circuits*, vol. 44, no.4, Apr. 2009.

[8] I. Seo, R. M. Fox "Comparison of Quasi-/Pseudo-Floating Gate Techniques and Low-Voltage Applications," *Analog Integrated circuits and signal processing*, 47, pp. 183-192, 2006.

Bulk-Driven Three-stage Class-AB CMOS OTA

E. Cabrera-Bernal
Electronic Engineering Department
University of Seville
Seville, Spain
ecabrera@gie.us.es

S. Pennisi, A. D. Grasso
DIEEI
University of Catania
Catania, Italy
salvatore.pennisi@dieei.unict.it

***Abstract*—In this paper a bulk-driven three-stage class-AB operational transconductance amplifier (OTA) is presented. The design is suitable for very low voltage design and, concretely, a 0.7 V supply voltage is applied. The OTA is designed in 180-nm standard CMOS technology and achieves a 61 dB open loop gain and a unity gain bandwidth of 3.71 MHz while driving a capacitive load of 20 pF.**

Keywords—Bulk-driven; Low-Voltage; OTA; class-AB; CMOS

I. INTRODUCTION

The continuous downscaling of transistor size in CMOS technologies implies, unavoidably, the decrease of the supply voltage in order to ensure circuit reliability and lifespan. Moreover, electronic industry is continuously demanding for portable devices with increasingly operation time in order to satisfy modern lifestyle, where portable devices have become ubiquitous.

However, while supply voltages decrease, threshold voltages (V_T) do not decrease in the same proportion. This is a main concern in analog design, where transistors operating in saturation are usually preferred to achieve higher transconductances, lower noise and overall better performance.

Therefore, in order to maintain good circuit performances in low voltage conditions, new topologies and design techniques must be developed to deal with low power supply and large V_T, while maintaining acceptable signal swing. Techniques such as floating gate transistors [1][1], level shifting techniques [2] or special low V_T devices are some examples of low voltage techniques. Bulk-driven techniques have also been extensively used for low voltage design ([3]-[8]). In this approach, the bulk terminal of the MOS transistor is driven by the signal while the transistor is properly biased from its gate terminal. Applying the signal through the bulk allows modifying the V_T, thus modifying the current through the device and obtaining a bulk transconductance, g_{mb}.

In this paper, a bulk-driven three-stage class-AB amplifier, which works under 0.7-V supply, is presented. A brief review of bulk driven technique is provided in Section II. The proposed bulk-driven three-stage class-AB amplifier topology is presented in Sec. III. The main simulation results of the proposed amplifier, as well as a comparison with other sub 1-V amplifiers, are carried out in Sec. IV. Conclusions are drawn in Sec. V.

II. BULK DRIVEN TECHNIQUE

In traditional gate-driven transistors, the conductivity of the channel and, thus, the drain current, I_D, is usually controlled by the gate-source voltage V_{GS}, but, as already stated, the drain current can also be controlled by the bulk-source voltage V_{BS}. This is, normally, an unwanted parasitic effect but in a bulk driven transistor, the idea is to use that g_{mb} instead of the source transconductance g_m. The bulk terminal has no threshold voltage associated and, as a result, the V_T drawback is eliminated. This makes the technique especially suitable for low voltage design.

One of the main disadvantages of bulk driven technique is the fact that g_{mb} is smaller than g_m, as shown in (1)

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2\varphi_F + V_{BS}}} = \eta g_m \tag{1}$$

where η is usually between 0.2 and 0.4. When designing amplifiers, this leads to poor DC gain performance, larger noise and offset. In the proposed structure a third stage is added in order to counteract the drawback of low DC gain.

Another issue that must be considered is the fact that the bulk-driven technique requires each bulk to be accessible, hence, in standard CMOS technologies, only *p*-channel transistors can be driven from the bulk.

III. PROPOSED BULK-DRIVEN CLASS-AB AMPLIFIER

The schematic of the proposed solution is shown in Fig.1. It is made up of three gain stages, namely the differential stage M_1-M_4, the second common-source stage M_5-M_6 and the third common-source stage M_7-M_8.

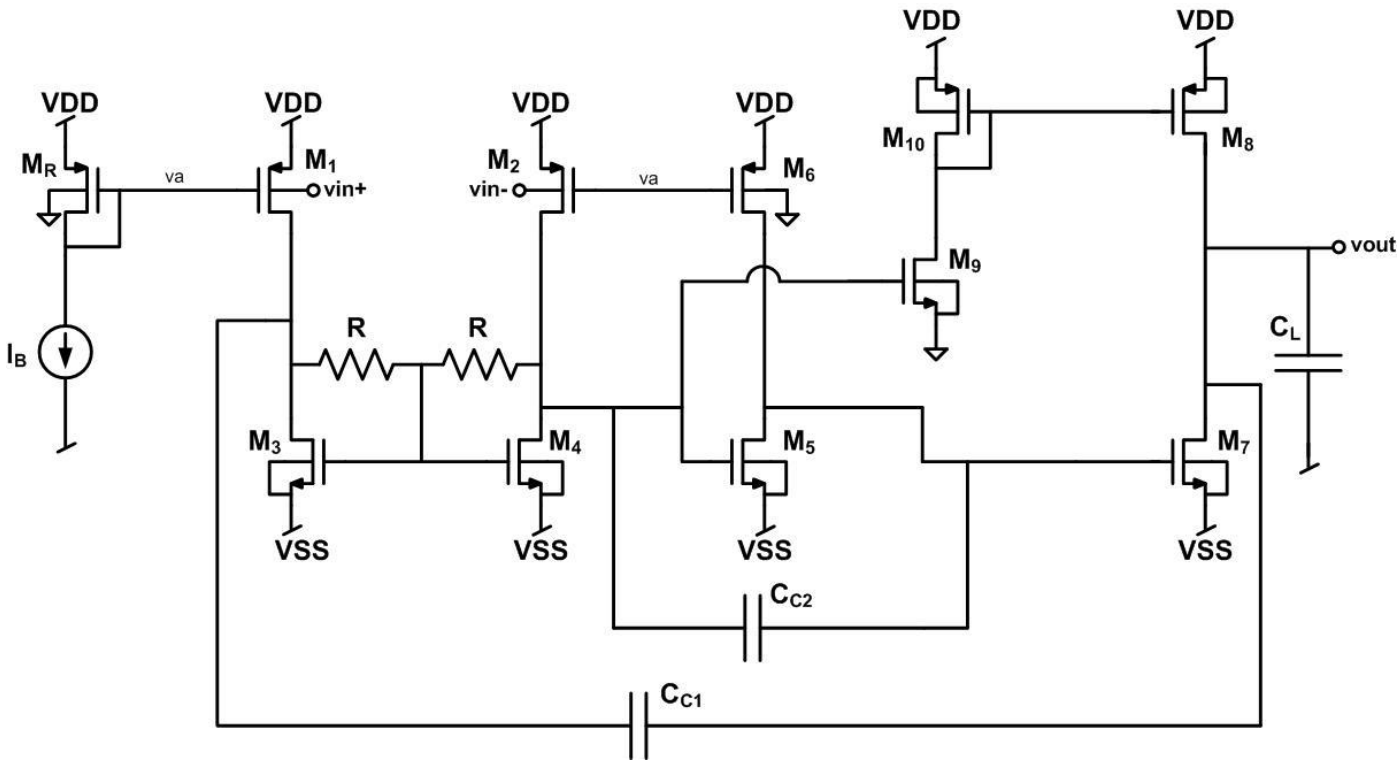


Fig. 1. Proposed bulk-driven three-stage class-AB amplifier.

The differential stage is made up of the bulk-driven differential pair, M_1-M_2, biased by diode-connected transistor, M_R, whose body is tied to the analog ground, i.e., (VDD+VSS)/2. In this way, M_R-M_1 and M_R-M_2 form two current mirrors that accurately set the DC current, provided that also the body of M_1-M_2 is connected to the analog ground. The active load of the first stage is realized with transistors M_3-M_4. The use of resistors R enables true differential mode operation from pair M_1-M_2 that is otherwise intrinsically pseudo differential. Indeed, the small-signal voltage at the drain of M_4 (output of the first stage) depends on both *Vin+* and *Vin-*. The first stage DC gain can be approximated by $g_{mb} \cdot R$.

Resistors R set also the common-mode voltage at the drain of M_3-M_4 to be equal to their gate voltage. The DC current in the second stage is set through current generator M_6, and thanks to the mirroring action between M_4 and M_5 (they have the same V_{GS}), M_5 can be dimensioned so as to minimize systematic offset (by setting equal nominal DC current in M_5 and M_6). The last stage is biased by current generator M_8, whose current is set by the pseudo current mirror formed by M_4 and M_9. Note that this current is signal dependent and that increases when *Vin+* increases. In other words, both M_7 and M_8 can deliver a large-signal current greater than the standby value, and therefore the third stage works in class AB.

Frequency compensation is obtained through Miller capacitors C_{C1} and C_{C2} and a current buffer implemented by M_3-M_4, with a technique similar to that developed in [9] for a nested Miller compensated OTA. Dominant pole is hence achieved through C_{C1}, and the unity-gain bandwidth (GBW) is equal to $g_{mb1,2}/C_{C1}$.

Transistors aspect ratios, as well as the main circuit devices values are summarized in Table I.

TABLE I. TRANSISTORS DIMENSIONS AND DEVICES VALUES.

Device	Value	Device	Value
M_1, M_2	12µm/540nm	I_B	4µA
M_3, M_4	2µm/540nm	C_{C1}	500fF
M_5, M_6	5µm/540nm	C_{C2}	50fF
M_7, M_8	30µm/540nm	R	250kΩ
M_9	2µm/540nm	C_L	20pF
M_{10}	12µm/540nm	V_{DD}	0.7v
M_R	12µm/540nm		

IV. RESULTS

In this section, the main simulation results of the proposed amplifier are shown. At the end of the section, a brief comparison of performances among this amplifier and other low voltage amplifiers is also carried out.

Fig. 2 illustrates the frequency response of the proposed amplifier. The open loop gain is 61dB and the unity-gain

bandwidth is 3.7 MHz. The phase margin resulted to be around 62º. The common mode rejection ratio, CMRR, and the power supply rejection ratio, PSRR, have also been simulated. Their DC values are 46.8dB for the CMRR and 61.2dB and 72.4dB for the positive and negative PSRR, respectively.

The amplifier was connected in inverting unity gain configuration as shown in Fig. 3 (Ra=Rb=100 kΩ). The response to an input step of 600 mV is illustrated in Fig. 4. The positive (negative) slew rate was 2.2V/µs (4.9V/µs) besides, 1% settling time was 594 ns (positive step) and 379 ns (negative step), respectively. It is seen that an almost rail-to-rail output swing is achieved. The input common mode range (ICMR) is also in principle rail to rail but is, actually, set by the maximum allowed input current that flows into the bulk. Thus, it should be limited to 400mV in order to maintain the input current below 3nA.

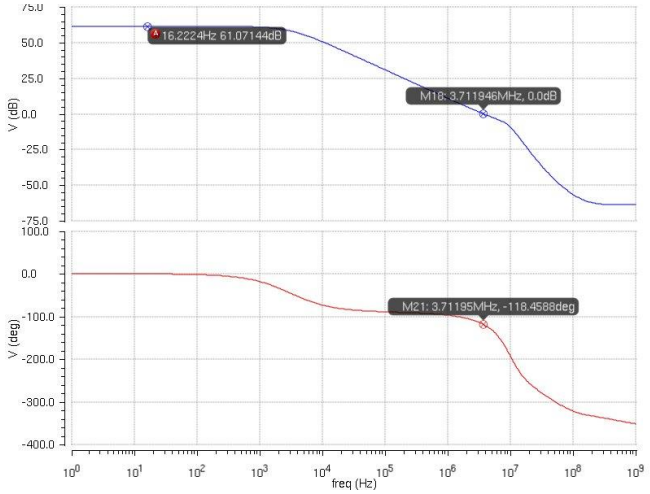


Fig. 2. Frequency respose of the proposed amplifier.

Main performance parameters of the proposed OTA are summarized in Table II. A comparison with other sub-1V amplifiers is also presented in Table III where a figure of merit (FOM) is included in order to make the comparison easier. The FOM is defined in (2), where I is the standby current consumption and C_L is the load capacitance [12]. High-performance amplifiers are characterized by a larger FOM.

$$FOM = 100 \cdot \frac{GBW \cdot C_L}{I} \qquad (2)$$

It is apparent from TABLE III. that the proposed solution exhibits the best FOM among the considered sub-1V amplifiers. The FOM value versus the year of publication for the amplifiers appearing in TABLE III. is also plotted in Fig. 5.

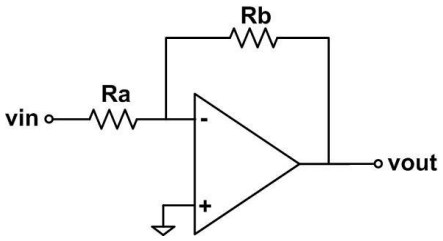


Fig. 3. Amplifier in inverting closed loop configuration.

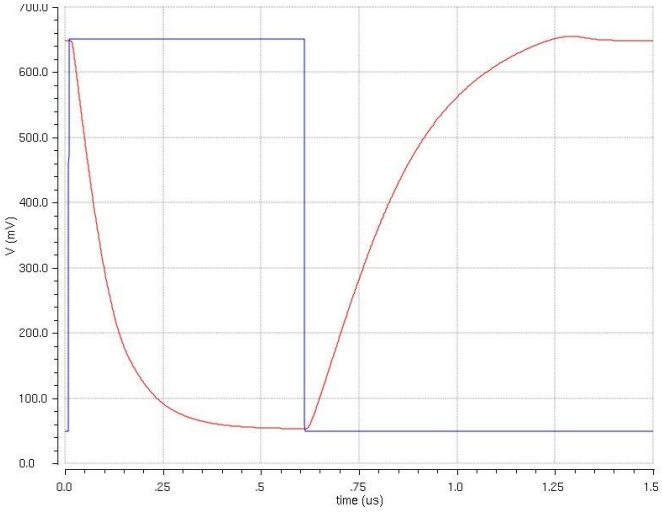


Fig. 4. Step response of the proposed OTA in unty gain configuration.

TABLE II. RESULTS SUMMARY.

Parameter	Value
Supply voltage [V]	0.7
Power dissipation [uW]	22.4
ICMR [mV]	400
Max Input current [nA]	2.96
Open Loop Gain [dB]	61.07
Open Loop Unity Gain BW [MHz]	3.7
Phase Margin [º]	62
SR+/SR- [V/us]	2.2/4.9
1% Settling time (+/-) [ns]	594/379
CMRR@DC [dB]	46.8
PSRR+@DC [dB]	61.2
PSRR-@DC [dB]	72.4
Input Ref. Noise @1MHz [nV/√Hz]	273
THD @100kHz (250mV input) [%]	0.058
THD @250kHz (250mV input) [%]	0.460

V. CONCLUSIONS

In this paper, a bulk-driven three-stage class-AB CMOS OTA, suitable for very low voltage supplies has been presented. Operation under 0.7 V was simulated using the models of a 180-nm standard CMOS technology and results compared with the state-of-the-art sub-1V amplifiers. The proposed solution exhibits the best FOM. Future work will be aimed to balance the positive and negative slew rate in order to reduce the settling time and drive even larger load capacitors.

TABLE III. PERFORMANCE COMPARISON OF SUB-1V AMPLIFIERS.

Works	Technology [µm]	C_L [pF]	UGBW [MHz]	PM [º]	SR+/- [V/us]	Supply [V]	Power [µW]	FOM
1998 [3]	2	22	1.3	57	0.7/1.6	1	287	10
2001[4]	0.5	-	2	57	0.5	1	40	50
2002[5]	2.5	-	0.56	62	-	0.9	0.45	13.4
2005[6] Bulk Driven (BD)	0.18	20	2.5	-	2.89	0.5	110	22.7
2005[6] Gate Driven (GD)	0.18	20	10	-	2	0.5	75	133.4
2009[7]	0.35	2.5	0.54	52	-	0.9	9.9	12.3
2013[8]	0.35	15	11.67	66	2.53/1.37	1	197	88.9
2000[10]	1.2	15	1.9	61	0.8/1	1	410	13.7
2003[11]	0.25	18	1.2	60	0.2	0.8	8	218
This work	0.18	20	3.7	62	2.2/4.9	0.7	22.4	231.8

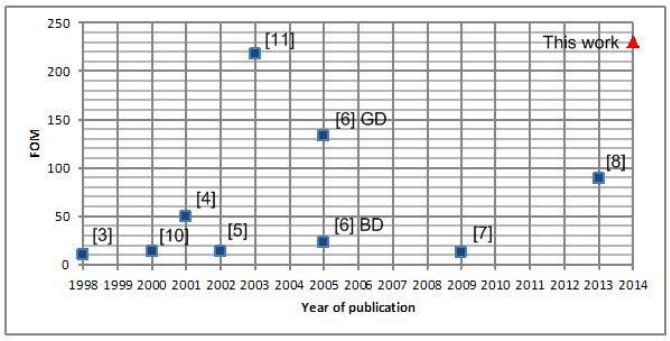


Fig. 5. FOM vs Year of Publication for the amplifiers appearing in the comparison of TABLE III.

ACKNOWLEDGMENT

This work was partially supported by the Spanish Ministry of Economy and Competitiveness under the project TEC2011-28724-C03-01 and the Andalousian "Consejería de Economía, Innovación y Ciencia" under the project TIC-6323.

REFERENCES

[1] Ramirez-Angulo, J., Choi, S.C. & Gonzalez-Altamirano, G. 1995, "Low-voltage circuits building blocks using multiple-input floating-gate transistors", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 11, pp. 971-974.

[2] Rajput, S.S. & Jamuar, S.S. 2001, "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications", *IEE Proceedings: Circuits, Devices and Systems*, vol. 148, no. 5, pp. 273-278.

[3] Blalock, B. J. , Allen, P. E., & Rincon-Mora, G. A., 1988, "Designing 1-V Op Amps using standard digital CMOS technology" *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process*., vol.45, no. 7, pp. 769-780.

[4] Lehmann, T. & Cassia, M., 2001, "1-V power supply CMOS cascode amplifier" *IEEE J. Solid-State Circu*its, vol 36, no.7, pp. 1082-1086.

[5] Stockstad, T. & Yoshizawa, H., 2002, "A 0.9-V 0.5 µm rail-to-rail CMOS operational amplifier", *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp.286-292.

[6] Chatter, S., Tsividis, Y. & Kinget, P., 2005, "0.5-V analog circuit techniques and their application in OTA and filter design", *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373-2387

[7] Pan, S. W., Chuang, C. C.,Yang, C. H. & Lai, Y. S., 2009, "A novel OTA with dual bulk-driven input stage", *Proc. IEEE Int. Symp. Circuits Syst*., pp. 21-24.

[8] Zuo L. & Islam S.K. 2013, "Low-Voltage Bulk-Driven Operational Amplifier With Improved

[9] Grasso, A. D., Palumbo, G., Pennisi, S., 2007"Advances in Reversed Nested Miller Compensation" IEEE Transactions on Circuits and Systems—I, vol. 54, no. 7.

[10] Duque-Carrillo, J. F., Ausin, J. L., Torelli, G. Valverde, J. M. & Dominguez, M. A. 2000, "1-V rail-to-rail operational amplifiers in standard CMOS technology*", IEEE J. Solid-State Circuits*, vol.35, no. 1, pp. 33-44.

[11] Libin, Y., Steayert, M. & Sansen, W., 2003, "A 0.8 V, 8 µm, CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load", *Proc. Eur. Solid-State Circuits Conf*., pp.297-300

[12] Peng, X & Sansen, W., 2004 "AC boosting compensation scheme for low-power multistage amplifiers". *IEEE Journal of Solid-state Circuits*; 39:2074–2077.

0.7-V Bulk-Driven Three-Stage Class-AB OTA

E. Cabrera-Bernal
Electronic Engineering Department
University of Seville
Seville, Spain
ecabrera@gie.us.es

S. Pennisi, A. D. Grasso
DIEEI
University of Catania
Catania, Italy
[spennisi, agrasso]@dieei.unict.it

***Abstract*—A high-performance architecture for bulk-driven operational transconductance amplifiers (OTAs) is presented. The solution exploits a three-gain-stage topology and, as a distinctive behavior, provides an inherent class-AB performance with simple and robust standby current control. A 0.7-V supply OTA is designed using a 180-nm standard CMOS technology. Post layout simulations show a 61-dB open loop gain and a unity gain bandwidth of 3.6 MHz, under a capacitive load of 20 pF. Significant performance improvement when compared to prior art is achieved, so that the best figure of merit is found.**

Keywords—Bulk-driven; Low-Voltage; OTA; class-AB; CMOS

I. INTRODUCTION

The continuous downscaling of transistor size in CMOS technologies implies, unavoidably, the decrease of the supply voltage in order to ensure circuit reliability and lifespan. Moreover, electronic industry is continuously demanding for portable devices with increasingly operation time in order to satisfy modern lifestyle, where portable devices have become ubiquitous.

However, while supply voltages decrease, threshold voltages (V_T) do not decrease in the same proportion. This is a main concern in analog design, where transistors operating in saturation are usually preferred to achieve higher transconductances, lower noise and overall better performance.

Consequently, in order to preserve circuit performances in low voltage conditions, new topologies and design techniques must be developed to deal with low power supply and large V_T, while maintaining acceptable signal swing. Techniques such as floating gate transistors [1], level shifting [2] or employing special low V_T devices are some examples of low voltage design approaches. Bulk-driven techniques have also been extensively exploited ([3]-[8]). In this approach, the bulk terminal of the MOS transistor is driven by the signal, while the transistor is properly biased from its gate terminal. Applying the signal through the bulk allows modifying the V_T, thus modifying the current through the device and obtaining a bulk transconductance, g_{mb}. The main drawback of this method is the low achievable transconductance that, especially in the design of amplifiers, implies low gain, low bandwidth and high noise.

In this paper, a bulk-driven class-AB operational transconductance amplifier (OTA) in 0.18-µm CMOS, which works under 0.7-V supply, is presented. The OTA provides more than 60-dB DC gain thanks to a three-stage architecture that is used to compensate for the transconductance reduction. The added stage, however, does not sacrifice the gain-bandwidth product, which resulted larger than 3 MHz under a load capacitance of 20 pF, a value comparable with three-stage gate-driven OTAs under the same load and current consumption [9]. After a brief review of bulk driven technique in Section II, the proposed OTA topology is presented in Sec. III. The main post layout simulation results along with a comparison with other sub 1-V solutions are carried out in Sec. IV. Conclusions are drawn in Sec. V.

II. BULK DRIVEN TECHNIQUE

In traditional gate-driven transistors, the conductivity of the channel and, thus, the drain current, I_D, is controlled by the gate-source voltage V_{GS}, but, as already stated, the drain current can also be controlled by the bulk-source voltage V_{BS}. This is normally an unwanted parasitic effect, but in a bulk driven transistor the idea is to use that g_{mb} instead of the source transconductance g_m. The bulk terminal has no threshold voltage associated and, as a result, the V_T drawback is eliminated. This makes the technique especially suitable for low voltage design.

One of the main disadvantages of bulk driven technique is the fact that g_{mb} is smaller than g_m, as quantified in (1)

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{2\varphi_F + V_{BS}}} = \eta g_m \quad (1)$$

where η is usually between 0.2 and 0.4. When designing amplifiers, this leads to poor DC gain performance, larger noise and offset. In the proposed structure a third stage is added in order to counteract the drawback of low DC gain.

Another issue that must be considered is the fact that the bulk-driven technique requires each bulk to be accessible, hence, in standard CMOS technologies, only *p*-channel transistors can be driven from the bulk.

III. PROPOSED BULK-DRIVEN CLASS-AB AMPLIFIER

The schematic of the proposed solution is shown in Fig.1. It is made up of three gain stages, namely the differential stage M_1-M_4, the second common-source stage M_5-M_6 and the third common-source stage M_7-M_8.

The differential stage is made up of the bulk-driven differential pair, M_1-M_2, biased by diode-connected transistor, M_R, whose body is tied to the virtual ground, i.e., $(V_{DD}+V_{SS})/2$

978-1-4799-8893-8/15/$31.00 ©2015 IEEE

(it should be noted that the proposed structure can work under double or single supply). In this way, M_R-M_1 and M_R-M_2 form two current mirrors that accurately set the DC current, provided that also the body of M_1-M_2 is connected to the analog ground. The active load of the first stage is realized with transistors M_3-M_4. The use of resistors R enables true differential mode operation from pair M_1-M_2 that is otherwise intrinsically pseudo differential. Indeed, the small-signal voltage at the drain of M_4 (output of the first stage) depends on both V_{in+} and V_{in-}. The first stage DC gain can be approximated by g_{mb}·R.

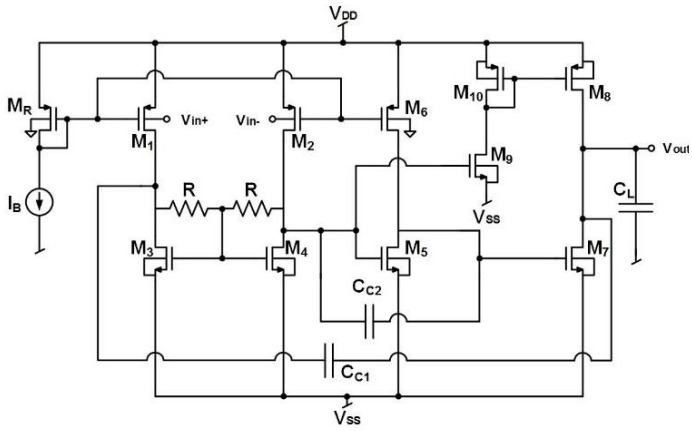


Fig. 1. Schematic diagram of the proposed OTA.

TABLE I. TRANSISTORS DIMENSIONS AND DEVICES VALUES.

Device	Value	Parameter	Value
M_R , M_1, M_2, M_{10}	12µm/540nm	I_B	4 µA
M_3, M_4, M_9	2µm/540nm	C_{C1}	550 fF
M_5, M_7	5µm/540nm	C_{C2}	30 fF
M_6, M_8	30µm/540nm	R	250 kΩ
C_L	20 pF	V_{DD} -V_{SS}	0.7 V

Resistors R set also the common-mode voltage at the drain of M_3-M_4 to be equal to their gate voltage. The DC current in the second stage is set through current generator M_6, and thanks to the mirroring action between M_4 and M_5 (they have the same V_{GS}), M_5 can be dimensioned so as to minimize systematic offset (by setting equal nominal DC current in M_5 and M_6). The last stage is biased by current generator M_8, whose current is set by the pseudo current mirror formed by M_4 and M_9. Note that this current is signal dependent and that increases when $Vin+$ increases. In other words, both M_7 and M_8 can deliver a large-signal current greater than the standby value, and therefore the third stage works in class AB.

Frequency compensation is obtained through Miller capacitors C_{C1} and C_{C2} and a current buffer implemented by M_3-M_4, with a technique similar to that developed in [10] for a nested Miller compensated OTA. Dominant pole is hence achieved through C_{C1}, and the unity-gain bandwidth (GBW) is equal to $g_{mb1,2}/C_{C1}$.

Transistors aspect ratios, as well as the main circuit devices values are summarized in Tab. I.

IV. POST LAYOUT SIMULATION RESULTS

The OTA shown in fig. 1 was designed in a 180-nm standard CMOS technology. The layout of the amplifier is shown in fig. 2. The occupied area is 120 ×165µm^2.

Figure 3 illustrates the frequency response of the proposed amplifier. The open loop gain is 61 dB and the unity-gain bandwidth is 3.6 MHz. The phase margin resulted to be around 60º. The common mode rejection ratio, CMRR, and the power supply rejection ratio, PSRR, have also been simulated. Their DC values are 46.7 dB for the CMRR and 60.2 dB/72.6 dB for the positive/negative PSRR, respectively.

The amplifier was connected in inverting unity gain configuration as shown in Fig. 4 (R_a=R_b=100 kΩ). The response to an input step of 600 mV is illustrated in Fig. 5. The positive (negative) slew rate was 2 V/µs (4.4 V/µs) besides, 1% settling time was 733 ns (positive step) and 380 ns (negative step), respectively. It is seen that an almost rail-to-rail output swing is achieved. The input common mode range (ICMR) is also in principle rail to rail but is actually set by the maximum allowed input current that flows into the bulk. Thus, it should be limited to 400 mV in order to maintain the input current below 4 nA.

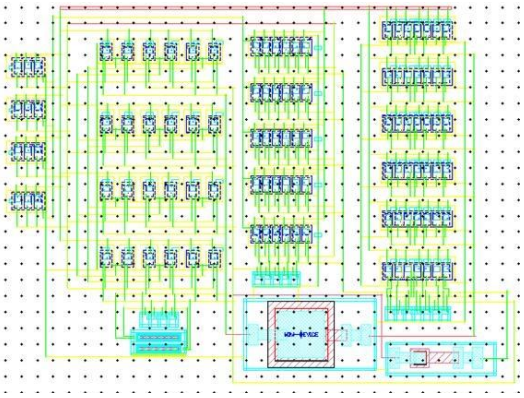


Fig. 2. Layout of the proposed amplifier, area is 120 ×165µm^2.

Main performance parameters of the proposed OTA are summarized in Tab. II.

The effect of temperature and process variations on the amplifier's performance has been investigated via corner simulations at 27°C, -40°C, 125°C. Results are summarized in Tab. III. The proposed amplifier remains stable across the extreme temperature and process corners.

A comparison with other sub-1V amplifiers is also presented in Tab. IV where a figure of merit (FOM) is included in order to make the comparison easier. The FOM is defined as [9]

$$FOM = 100 \cdot \frac{GBW \cdot C_L}{I_{DD}} \qquad (2)$$

where I_{DD} is the standby current consumption and C_L is the load capacitance. High-performance amplifiers are characterized by a larger FOM.

The FOM value versus the year of publication for the amplifiers appearing in TABLE IV. is also plotted in Fig. 6. It is apparent from TABLE IV. that the proposed solution exhibits the best FOM. Besides, it provides one of the highest GBW values with reduced DC current consumption.

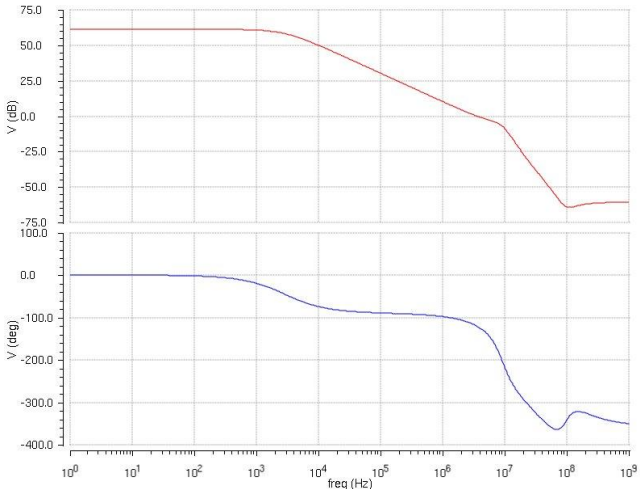


Fig. 3. Frequency response of the proposed amplifier (magnitude and phase).

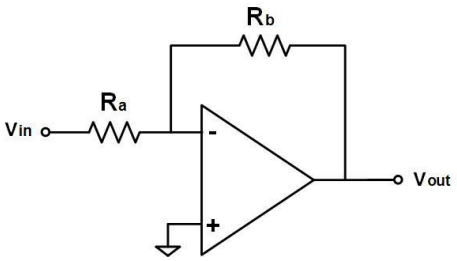


Fig. 4. Amplifier in inverting closed loop configuration.

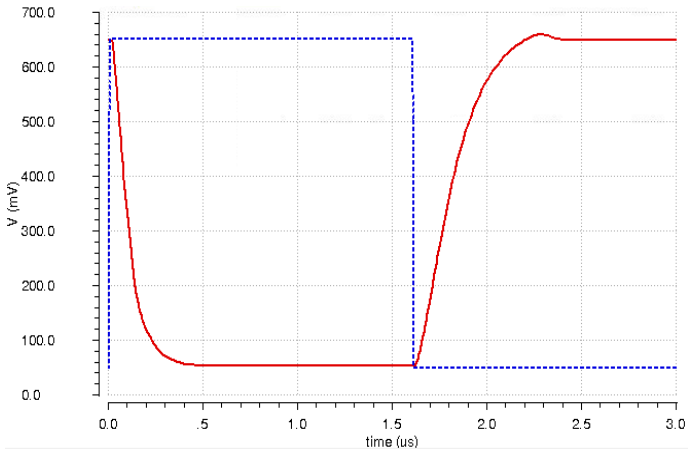


Fig. 5. Step response of the proposed OTA in inverting unity gain configuration.

TABLE II. SIMULATION RESULTS SUMMARY (C_L=20 PF).

Parameter	Value
Supply voltage (V_{DD}-V_{SS}) [V]	0.7
Power dissipation [µW]	22.4
ICMR [mV]	400
Max Input current [nA]	3.5
Open Loop Gain [dB]	61
GBW [MHz]	3.6
Phase Margin [deg]	60
Gain Margin	5.08
SR+/SR- [V/µs]	2/4.4
1% Settling time (+/-) [ns]	733/380
CMRR@DC [dB]	46.7
PSRR+@DC [dB]	60.2
PSRR-@DC [dB]	72.6
Input Ref. Noise @1MHz [nV/ √ Hz]	273
THD @100kHz, 250mV input [%]	0.061
THD @250kHz, 250mV input [%]	0.509

TABLE III. MAIN PERFORMANCE PARAMETERS OVER PROCESS AND TEMPERATURE VARIATIONS.

T= 27°C

Corner	TT	FF	SS	SF	FS
DC Gain [dB]	60.9	61.3	60.2	61.1	60.6
GBW [MHz]	3.57	3.70	3.41	3.54	3.57
PM [°]	59.74	61.2	58.90	60.57	59.28
GM [dB]	5.08	5.06	5.32	5.16	5.15
SR+/SR- [V/µs]	1.9/4.5	2.4/6.2	1.5/3.3	1.9/5.7	1.8/3.5
1% Ts+/Ts- [ns]	733/380	655/366	843/408	729/378	761/391

T= 125°C

Corner	TT	FF	SS	SF	FS
DC Gain [dB]	58.4	58.4	58.1	58.2	58.4
GBW [MHz]	3.15	3.24	3.04	3.10	3.18
PM [°]	56.81	58.45	55.90	57.87	56.20
GM [dB]	5.10	5.20	5.16	5.28	5.03
SR+/SR- [V/µs]	1.4/4.3	1.5/5.7	1.2/3.3	1.4/5.3	1.3/3.5
1% Ts+/Ts- [ns]	803/418	643/403	896/442	698/414	837/426

T= -40°C

Corner	TT	FF	SS	SF	FS
DC Gain [dB]	62.0	62.6	60.7	62.3	61.1
GBW [MHz]	4.01	4.17	3.77	3.99	3.96
PM [°]	60.59	61.90	59.72	61.11	60.22
GM [dB]	5.27	5.13	5.74	5.28	5.53
SR+/SR- [V/µs]	1.9/4.4	2.6/6.5	1.4/3.1	1.9/5.9	1.7/3.2
1% Ts+/Ts- [ns]	706/340	603/329	871/357	705/339	755/346

TABLE IV. PERFORMANCE COMPARISON OF SUB-1V AMPLIFIERS.

Works [b]		Technology [µm]	Supply [V]	DC Current [µA]	C_L [pF]	DC Gain [dB]	GBW [MHz]	PM [°]	SR+/- [V/µs]	FOM [MHz • pF/µA]
1998 [3]	GD	2	1	287	22	48.8	1.3	57	0.7/1.6	10
2001 [4]	BD	0.5	1	40	20	62-69	2	57	0.5	100
2002 [5]	BD	2.5	0.9	0.5	12	79	0.56	62	-	13.4
2005 [6]	BD	0.18	0.5	220	20	52	2.5	-	2.89	22.7
	GD	0.18	0.5	150	20	62	10	-	2	133.4
2009 [7]	BD	0.35	0.9	11	2.5	62	0.54	52	-	12.3
2013 [8]	BD	0.35	1	197	15	88.3	11.67	66	2.53/1.37	88.9
2000 [11]	GD	1.2	1	410	15	87	1.9	61	0.8/1	6.9
2014 [12]	BD	0.13	0.25	0.072	15	40	0.002	52	0.71	42
2013 [13] [a]	BD	0.05	0.5	200	20	74	4.8	49°	3.4	0.48
This work [a]	BD	**0.18**	**0.7**	**32**	**20**	**61**	**3.6**	**60**	**2/4.4**	**225**

[a] Simulations.
[b] BD: Bulk Driven. GD: Gate Driven.

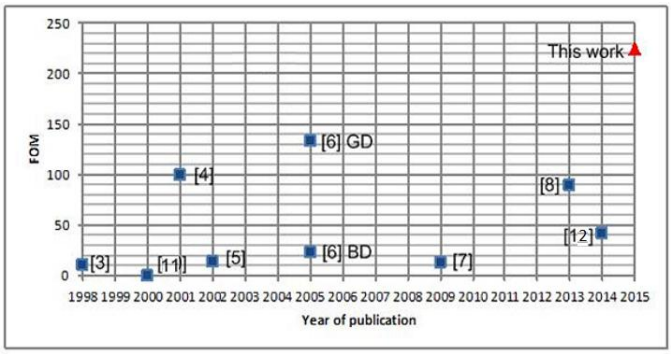


Fig. 6. FOM vs Year of publication for the amplifiers appearing in TABLE IV.

IV. CONCLUSIONS

In this paper, a bulk-driven three-stage class-AB CMOS OTA, suitable for very low voltage supplies has been presented. Operation under 0.7 V was demonstrated through simulations using the models of a 180-nm standard CMOS technology. Compared to the state-of-the-art sub-1V amplifiers, the proposed solution exhibits a significant improvement in small-signal and large-signal performance thanks to an efficient class AB configuration, as a result, it presents the best FOM. Future work will be aimed to balance the positive and negative slew rate in order to reduce the settling time and drive even larger load capacitors. Besides, fully-differential solutions to increase signal swing and CMRR should be developed.

REFERENCES

[1] J. Ramirez-Angulo, S.C. Choi, and G. Gonzalez-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors", *IEEE Trans. Circ. Syst.-I: Fund. Theor. App.*, vol. 42, no. 11, pp. 971-974, 1995.

[2] S. S. Rajput, and S. S. Jamuar, "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications", *IEE Proceedings: Circ. Dev. Syst.*, vol. 148, no. 5, pp. 273-278, 2001

[3] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V Op Amps using standard digital CMOS technology" *IEEE Trans. Circ. Syst. II Analog Dig. Sig. Proc.*, vol.45, no. 7, pp. 769-780, 1998

[4] T. Lehmann, and M. Cassia, "1-V power supply CMOS cascode amplifier" *IEEE J. Solid-State Circ.*, vol 36, no.7, pp. 1082-1086, 2001.

[5] T. Stockstad, and H. Yoshizawa, "A 0.9-V 0.5 µm rail-to-rail CMOS operational amplifier", *IEEE J. Solid-State Circ.*, vol. 37, no. 3, pp.286-292, 2002.

[6] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design", *IEEE J. Solid-State Circ.*, vol. 40, no. 12, pp. 2373-2387, 2005.

[7] S. W. Pan, C. C. Chuang, C. H. Yang, and Y. S. Lai, "A novel OTA with dual bulk-driven input stage", *Proc. IEEE Int. Symp. Circ. Syst.*, pp. 21-24, 2009.

[8] L. Zuo and S. K. Islam, "Low-Voltage Bulk-Driven Operational Amplifier With Improved Transconductance", *IEEE Trans. Circ. Syst.-I: Regul. Pap.,* vol. 60, no. 8, pp. 2084-2091, 2013.

[9] P. Monsurrò, S. Pennisi, G. Scotti and Trifiletti, "0.9-V CMOS cascode amplifier with body-driven gain boosting," Int. J. Circ. Theor. Appl., vol. 37, pp. 193–202, 2009.

[10] A.D. Grasso, G. Palumbo and S. Pennisi, "Advances in Reversed Nested Miller Compensation" *IEEE Trans. Circ. Syst.I: Regul. Pap.*, vol. 54, no. 7, pp. 1459-1470, 2007.

[11] J. F. Duque-Carrillo, J. L. Ausin, G. Torelli, J. M. Valverde and M. A. Dominguez, "1-V rail-to-rail operational amplifiers in standard CMOS technology*", IEEE J. Solid-State Circ.*, vol.35, no. 1, pp. 33-44, 2000.

[12] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB Gain OTA Operating at 0.25-V Power Supply in 130-nm Digital CMOS Process," *IEEE Trans. Circ. Syst.I: Regul. Pap.*, vol. 61, no. 6, pp. 1609–1617, 2014.

[13] T. Kulej, "0.5-V bulk-driven CMOS operational amplifier," *IET Circ. Dev. Syst.,* vol.7, no. 6, pp. 352-360, 2013.

0.7-V Three-Stage Class-AB CMOS Operational Transconductance Amplifier

Elena Cabrera-Bernal, *Student Member, IEEE*, Salvatore Pennisi, *Senior Member, IEEE*, Alfio Dario Grasso, *Senior Member, IEEE*, Antonio Torralba, *Senior Member, IEEE*, and Ramón Gonzalez Carvajal, *Senior Member, IEEE*

***Abstract*—A simple high-performance architecture for bulk-driven operational transconductance amplifiers (OTAs) is presented. The solution, suitable for operation under sub 1-V single supply, is made up of three gain stages and, as an additional feature, provides inherent class-AB behavior with accurate and robust standby current control. The OTA is fabricated in a 180-nm standard CMOS technology, occupies an area of $19.8 \cdot 10^{-3}$ mm^2 and is powered from 0.7 V with a standby current consumption of around 36 μA. DC gain and unity gain frequency are 57 dB and 3 MHz, respectively, under a capacitive load of 20 pF. Overall good large-signal and small-signal performances are achieved, making the solution extremely competitive in comparison to the state of the art.**

***Index Terms*—Bulk-driven, class-AB, CMOS analog integrated circuits, low-voltage, operational transconductance amplifier.**

I. Introduction

ONE of the main trends of modern consumer electronics industry is towards the extension of portable devices autonomy through the adoption of low power design techniques [1]–[5]. This has reinforced the interest in the development of low-voltage design approaches and techniques for the limitation of power consumption. Considering the CMOS technology, the most straightforward methodologies to enable operation below 1-V supplies are subthreshold biasing and bulk driving (or body driving) and even a combination of both [6]–[20].

Subthreshold transistors can be biased with currents in the range of a few nanoamperes, but this also implies low unity-gain frequency and low achievable slew rate values. Therefore, subthreshold operation is particularly suitable in wireless sensor networks, biomedical applications and in all those applications where speed is not a concern, e.g., for bandwidth specifications in the range of a few kilohertz [21].

Manuscript received June 6, 2016; revised July 27, 2016; accepted July 28, 2016. Date of publication August 30, 2016; date of current version October 25, 2016. This work was partially supported by the Spanish Ministry of Economy and Competitiveness under the project TEC2013-47286-C3-1-R and the Andalousian "Consejería de Economía, Innovación y Ciencia" under the project P12-TIC-1862. This paper was recommended by Associate Editor A. Demosthenous.

E. Cabrera-Bernal, A. Torralba, and R. G. Carvajal are with the Ingenieria Electronica, University of Seville, Escuela Técnica Superior de Ingenieria, 41012 Seville, Spain (e-mail: ecabrera3@us.es; torralba@us.es; carvajal@us.es).

S. Pennisi and A. D. Grasso are with the Dipartamento de Ingegneria Elettrica Elettronica e Informatica, University of Catania, Catania I-95125, Italy (e-mail: salvatore.pennisi@dieei.unict.it; alfio.grasso@dieei.unict.it).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2016.2597440

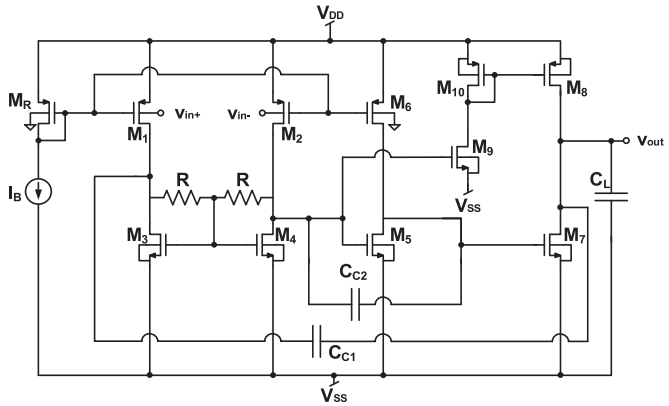


Fig. 1. Schematic diagram of the proposed OTA.

As said, bulk-driven has also been exploited extensively for low voltage applications. While in traditional gate-driven transistors, the conductivity of the channel and, hence, the drain current, I_D, is controlled by the gate-source voltage V_{GS}, in bulk driven transistors the drain current is controlled by the bulk-source voltage V_{BS}. The main idea is to use the bulk transconductance, g_{mb}, instead of the gate transconductance, g_m, since the bulk terminal has no threshold voltage associated and, as a result, the V_T limitation is eliminated. Note that the bulk-driven technique requires the MOS bulk terminal to be accessible, hence, in standard n-well CMOS technologies, only p-channel transistors can be utilized. One of the main disadvantages of the bulk driven technique is the fact that $g_{mb} = \gamma g_m / 2\sqrt{2\varphi_F + V_{BS}} = \eta g_m$, with $0.1 < \eta < 0.4$. This means that g_{mb} is smaller than g_m and, specifically for amplifiers design, this leads to poor DC gain and gain-bandwidth performance with larger noise and offset.

In this paper, a high performance bulk-driven three-stage class-AB amplifier topology able to work under sub-1 V supply is presented. To provide adequate DC gain, the solution adopts a three-gain stage architecture, as also recently proposed in [22]–[24] for a subthreshold OTA. The proposed topology will be thoroughly explained and analyzed with the derivation of useful design equations in Sections II and III. Implementation and experimental results are presented in Sections IV as well as a comparison with other similar amplifiers. Some conclusions are drawn in Section V.

II. Circuit Description

The schematic of the proposed OTA is shown in Fig. 1. As already mentioned, it is made up of three gain stages,

namely the differential stage $M_1 - M_4$, the second common-source stage $M_5 - M_6$ and the third common-source stage $M_7 - M_{10}$.

Transistor M_R, whose body is tied to the virtual ground, i.e., $(V_{DD} + V_{SS})/2$, sets through mirror ratios the quiescent current of the differential pair $M_1 - M_2$ and of its load $M_3 - M_4$, as well as of transistor M_6 acting as a load of the second stage. Indeed, $M_R - M_1$ and $M_R - M_2$ form two current mirrors that accurately set the DC current in the pair, provided that also the body of $M_1 - M_2$ is connected to the analog ground. The active load of the first stage is realized with transistors $M_3 - M_4$ and two resistors, R. Due to the fact that no DC current flows through resistors, the drains of $M_3 - M_4$ are at the same potential of their gates and, consequently, the DC current of M5 is also accurately set by (pseudo) current-mirror ratios

$$I_{D5} = \frac{I_{D4}\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}. \tag{1}$$

The excellent matching between the DC currents of M_5 and M_6, causes the drain of M_5 to be theoretically at the same potential of the drain of M_4, ultimately defining the current of M_7, again through a mirror ratio

$$I_{D7} = \frac{I_{D4}\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4}. \tag{2}$$

Note that current I_{D8} is set through current mirror $M_8 - M_{10}$ and pseudo-current mirror $M_9 - M_4$. Therefore, to theoretically nullify systematic offset, I_{D8} must be equal to I_{D7} leading to

$$\frac{\left(\frac{W}{L}\right)_8\left(\frac{W}{L}\right)_9}{\left[\left(\frac{W}{L}\right)_{10}\left(\frac{W}{L}\right)_4\right]} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4}. \tag{3}$$

In our design $(W/L)_9 = (W/L)_4$ was assumed for simplicity, but $(W/L)_9 < (W/L)_4$ could be used to slightly reduce current consumption. The minimum supply voltage $(V_{DD} - V_{SS})$ can be as low as $V_{DS1,2} + V_{GS3,4}$.

A final comment regards the class AB behavior of the third stage. Both transistors M_7 and M_8 can deliver a maximum signal current that is not limited by any DC value. Indeed, M_7 is in common source configuration, whereas the current in M_8 increases when $V_{\text{in}+}$ increases because v_{GS9} also increases.

III. Analysis and Design

In this section the main behavior of the proposed amplifier will be analyzed and design equations derived.

A. Differential Gain

The use of resistors R in the active load of the input stage enables fully differential operation of an otherwise pseudo-differential pair $M_1 - M_2$. To understand this fact, let us apply a single-ended small-signal voltage, v_d, at one input (e.g., the body of M_1), while grounding the second input. Referring to Fig. 3, voltage v_d is converted into a current, $g_{mb1}v_d$, one half

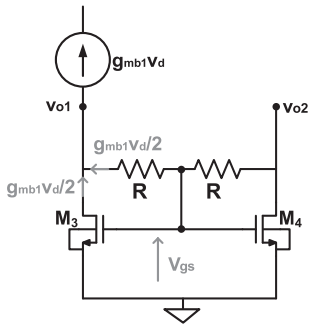


Fig. 2. Equivalent circuit used for demonstrating the differential behavior of the adopted solution.

of which will flow through the resistor series and the other half through transistor M_3, because M_3 and M_4 have the same v_{gs}, have the same transconductance and must consequently carry the same current. Fig. 2 shows then that a differential output voltage, $v_{o1} - v_{o2}$, is generated. The expression of the individual output voltages is approximated by[1]:

$$v_{o1} = v_{gs} - g_{mb1}R\frac{v_d}{2} = g_{mb1}\left(\frac{1}{g_{m3}} - R\right)\frac{v_d}{2} \tag{4a}$$

$$v_{o2} = v_{gs} + g_{mb1}R\frac{v_d}{2} = g_{mb1}\left(\frac{1}{g_{m3}} + R\right)\frac{v_d}{2} \tag{4b}$$

where in the second equality we used the following result: $g_{mb1}(v_d/2) = g_{m3}v_{gs}$. Given that $g_{mb1} = g_{mb2} = g_{mb1,2}$ and $g_{m3} = g_{m4} = g_{m3,4}$. Assuming that $g_{m3,4}R \gg 1$, then (4a), (4b) yield $v_{o1} = -v_{o2} \cong g_{mb1,2}R(v_d/2)$, demonstrating differential operation, since the application of v_d from only one input terminal produces a differential output, as opposed to a pseudo-differential topology.

For the symmetry of the circuit, the same result holds also if we apply the input signal from the body of M_2. As a conclusion, the (single ended) gain of this first stage, v_{o2}/v_d can be approximated by $g_{mb1,2}R/2$. This outcome can be easily understood by referring to the fact that under small-signal differential input the gate of $M_3 - M_4$ is at virtual ground and therefore the load seen by the couple $M_1 - M_2$ is R (or, more accurately, $R//r_{ds1}//r_{ds3}$, as explained in footnote 1).

From the above considerations, it follows that the proposed solution is well suited to implement a fully differential OTA. In this paper, for the sake of simplicity, we will limit the design to a single-ended topology to focus our attention on the operating principles and to determine basic design equations.

B. Common Mode Rejection Ratio

Resistors R have the additional role of setting the common-mode voltage at the drain of $M_3 - M_4$ to be equal to their gate voltage (because no current flows in the resistors under common-mode input). Referring to Fig. 3, under common mode

[1]We are neglecting for simplicity the output resistance of M_1 (M_2) and M_3 (M_4). If this is not the case, a more accurate expression of the output voltage should include the parallel of R, r_{ds1}, and r_{ds3}, instead of R alone.

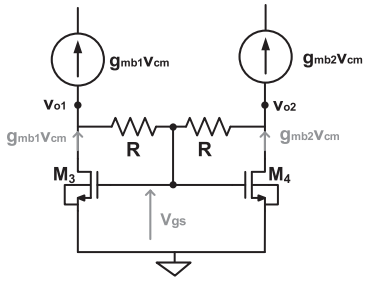


Fig. 3. Differential input stage CMRR analysis.

input no current flows onto resistors R and $g_{mb2}v_{cm}$ must equal $g_{m3}v_{gs}$. Therefore, the common mode gain is

$$A_{cm} = \frac{v_{o2}}{v_{cm}} = -\frac{g_{mb1,2}}{g_{m3,4}}. \tag{5}$$

This outcome can be easily understood by considering that if no current flows through the resistors then M_3 and M_4 operate as they are connected in diode and offer an equivalent resistance equal to $1/g_{m3,4}$.

The (single ended) common mode rejection ratio, defined as $|A_d/A_{cm}|$, is hence

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = \frac{1}{2}\frac{g_{mb1,2}R}{\frac{g_{mb1,2}}{g_{m3,4}}} = \frac{1}{2}g_{m3,4}R. \tag{6}$$

From (6) we see that $R \gg 1/g_{m3,4}$ must be chosen to obtain adequate CMRR values.

C. Frequency Compensation

Frequency compensation of the differential (open loop) gain is obtained through Miller capacitors C_{C1} and C_{C2} and a current buffer [25] implemented by $M_3 - M_4$, with a technique similar to that developed in [26] for a nested-Miller-compensated OTA. Dominant pole is hence achieved through C_{C1}. Assuming both $g_{mi}r_{oi}$, $g_{mi}R \gg 1$, where g_{mi} is the gate transconductance of transistor i and r_{oj} is the resistance of the output node of the amplifier jth stage, the OTA loop gain transfer function can be approximated as

$$A(s) \approx A_0 \frac{1 + \frac{s}{z_1}}{\left(1 + \frac{s}{p_1}\right)(as^2 + bs + 1)} \tag{7}$$

where the DC gain, A_0, the dominant pole, p_1, and the zero, z_1, are given by[2]

$$A_0 = \frac{g_{mb1,2}g_{m5}g_{m7}(R//r_{o1})r_{o2}r_{o3}}{2} \tag{8a}$$

$$p_1 = \frac{2}{g_{m5}g_{m7}(R//r_{o1})r_{o2}r_{o3}C_{C1}} \tag{8b}$$

$$z_1 = \frac{g_{m5}g_{m3}}{2C_{C1}g_{m5} - C_{C2}g_{m3}}. \tag{8c}$$

[2]In this accurate computation of the DC gain, the MOS transistors output resistances are included.

And for the remaining non-dominant complex conjugate poles, the coefficients of the polynomial in (7) are

$$a = \frac{C_{C2}C_L(2g_{m5} + g_{m3})}{g_{m3}g_{m5}g_{m7}} \tag{9a}$$

$$b = \frac{C_{C1}C_L + C_{C2}C_Lg_{m5}r_{o2}}{C_{C1}g_{m5}g_{m7}r_{o2}}. \tag{9b}$$

The damping coefficient of this pair of complex poles is given by

$$\xi = \frac{b}{2\sqrt{a}} = \frac{C_{C1} + C_{C2}g_{m5}r_{o2}}{2C_{C1}r_{o2}}\sqrt{\frac{C_Lg_{m3}}{g_{m5}g_{m7}C_{C2}(2g_{m5} + g_{m3})}}. \tag{10}$$

Given $g_{mb1,2}$, C_L, and C_{C1}, one can derive from (10) a suitable value of C_{C2} in order to avoid peaking in the frequency response and to obtain a phase margin in the range of 60 to 70°. Besides, $g_{m5}/g_{m3} > C_{C2}/(2C_{C1})$ can be chosen in order to obtain a negative zero from (8c) useful to increase the phase margin.

From (8a) and (8b) the gain-bandwidth product, ω_{GBW}, is

$$\omega_{GBW} = \frac{g_{mb1,2}}{C_{C1}}. \tag{11}$$

D. Noise

Noise in multistage amplifiers is usually dominated by the first stage provided that this first stage has a voltage gain considerably larger than the unity. Considering only white noise for simplicity, the equivalent input-referred noise voltage power spectral density (PSD) of the proposed amplifier can be approximated as (see the Appendix for the calculation of the input-referred equivalent noise contribution of resistors, $S_{VR,\text{in}}$)

$$\begin{aligned} S_{V,in} &\approx 2S_{V1,2}\left(\frac{g_{m1,2}}{g_{mb1,2}}\right)^2 + 2S_{V3,4}\left(\frac{g_{m3,4}}{g_{mb1,2}}\right)^2 + S_{VR,in} \\ &= 2\frac{2}{3}4kT\frac{1}{g_{mb1,2}}\left(\frac{g_{m1,2}}{g_{mb1,2}} + \frac{g_{m3,4}}{g_{mb1,2}}\right) \\ &\quad + 4kTR\left(\frac{1}{g_{mb1,2}r_{o1}}\right)^2\left[1 + \left(1 + \frac{2r_{o1}}{R}\right)^2\right] \\ &\approx \frac{16}{3}kT\frac{1}{g_{mb1,2}}\frac{g_{m1,2} + g_{m3,4}}{g_{mb1,2}} \end{aligned} \tag{12}$$

where S_{Vi} is the gate-referred noise voltage PSD of the i-th transistor and k and T are the Boltzmann's constant and the absolute temperature.

In the above expression noise from M_R was neglected since it is seen as a common-mode signal and rejected. Besides, also the noise from R results to be negligible provided that $(g_{m1,2} + g_{m3,4})r_{o1} \gg (3/4)(R/r_{o1})[1 + (1 + (2r_{o1}/R))^2]$. This condition is usually met.

Finally, it is also seen from (12) that to make noise of $M_{3,4}$ negligible, $g_{m3,4} \ll g_{m1,2}$ must be selected, yielding

$$S_{V,\text{in}} \approx \frac{16}{3}kT\frac{1}{g_{mb1,2}}\frac{1}{\eta} = \frac{16}{3}kT\frac{1}{g_{m1,2}}\left(\frac{1}{\eta}\right)^2. \tag{13}$$

However, $g_{m3,4} \ll g_{m1,2}$ cannot be easily set since large $g_{m3,4}$ values are needed from (6) to achieve sufficient $CMRR$ without requiring excessive R values.

TABLE I
TRANSISTORS DIMENSIONS AND DEVICE VALUES

Device	Value	Parameter	Value
M_R, M_1, M_2, M_{10}	12µm/540nm	I_B	4 µA
M_3, M_4, M_9	2µm/540nm	C_{C1}	550 fF
M_5, M_7	5µm/540nm	C_{C2}	30 fF
M_6, M_8	30µm/540nm	R_1, R_2	250 kΩ
C_L	20 pF	V_{DD}-V_{SS}	0.7 V

TABLE II
TRANSCONDUCTANCES (SIMULATED)

Transconductance	Value [µA/V]
$g_{mb1,2}$	12
$g_{m1,2}$	65
$g_{m3,4}$	65
g_{m5}	162
g_{m7}	150

E. Slew Rate

In multi-stage amplifiers, the slew rate, SR, is dictated by the slowest stage, i.e., $SR = \min[I_x/C_x]$, where I_x is the maximum charging or discharging current and C_x the load capacitor of x-th stage. If, as usual, the load capacitor is the largest one, then the output node is the most critical regarding the slew rate performance. This problem is alleviated if the last stage operates in class AB, leaving SR essentially determined by the first stage that drives the largest of the two compensation capacitors. Assuming $C_{C1} \gg C_{C2}$, slew rate can be expressed as

$$SR \approx \frac{(I_{D1} - I_{D1,\max})}{C_{C1}} \tag{14}$$

where $I_{D1} - I_{D1,\max}$ is the minimum current charging capacitor C_{C1} as I_{D1} is the quiescent current of M_1 and $I_{D1,\max}$ is the maximum instantaneous value. Current driving C_{C1} under large signals can be considerably different from the quiescent $I_{D1,2}$ value. Indeed, assuming a buffer configuration, for positive-going input voltage steps the current available from M_1 decreases as V_{TH1} increases, whereas for negative-going steps the current available from M_1 increases. This yields to an unbalanced SR performance with $SR^+ < SR^-$.

IV. IMPLEMENTATION AND EXPERIMENTAL VALIDATION

In order to validate the proposed OTA topology and associated design criteria, the amplifier in Fig. 1 was implemented in a 180-nm standard CMOS technology (thresholds around 0.4 V) under a 0.7-V single supply. Aspect ratios and standby currents were set in order to achieve a unity gain-bandwidth of 3.5 MHz with a load capacitor of 20 pF and a damping factor of the complex conjugated poles equal to 0.5.

The transistors aspect ratios together with the main circuit design parameters are summarized in Table I. The transconductances are summarized in Table II. Observe that $g_{m3,4} = g_{m1,2} = 65$ µA/V was chosen and that the two resistors R were set to 250 kΩ in order to find a trade-off between acceptable noise performance from (12) and sufficient CMRR from (6). Resistors are implemented with 1792 Ω/□ high resistive poly. Each resistor occupies 13.47 μm × 1.67 μm.

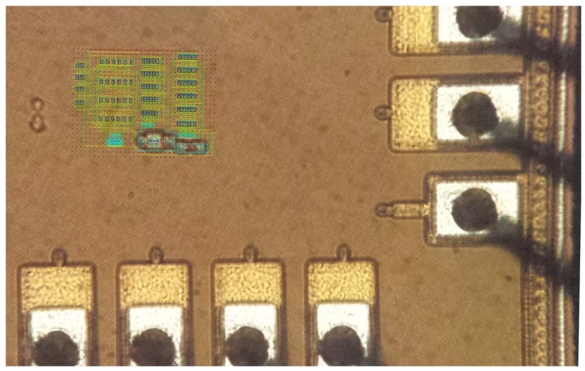


Fig. 4. Layout over microphotograph of the fabricated amplifier.

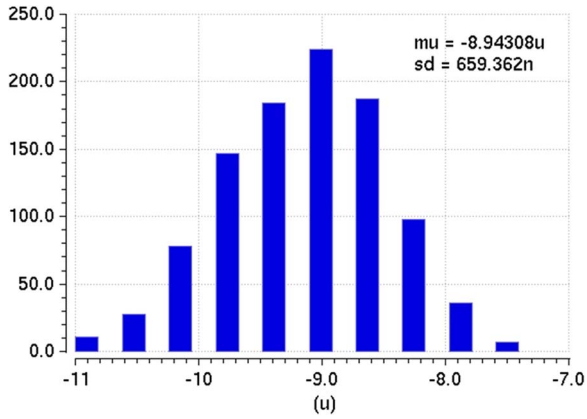


Fig. 5. Monte Carlo results for the standby current of the third stage.

Fig. 4 shows the layout of the amplifier superimposed to the microphotograph of the chip. The OTA occupies a silicon area of $19.8 \cdot 10^{-3}$ mm^2.

To check the robustness of the standby current control in the last stage of the OTA we performed 1000 Monte Carlo iterations (process and mismatch). Fig. 5 summarizes the simulated results. The mean of the standby current of the last stage is 8.94 μA and the standard deviation is only 0.66 μA (the nominal designed value is 10 μA). Of course, any output mismatch current, $i_{o,os}$, when referred the input produces an offset voltage $v_{i,os} = i_{o,os}/(g_{mb1,2}R//r_{o1}g_{m5}r_{o2}g_{m7})$. For instance, with the circuit parameters 2 μA of $i_{o,os}$ produces about 0.24 mV of input offset.

Fig. 6 illustrates the postlayout simulation of the Bode plot (magnitude and phase) of the loop gain, as well as process and mismatch Monte Carlo results for DC gain, GBW and phase margin for 1000 iterations. For the nominal case, the DC gain is 61 dB and GBW is 3.5 MHz, with phase margin of 59°. Standard deviations are respectively, 0.7 dB, 200 kHz, and 2.2°, showing that the proposed solution is robust against process mismatches.

The measured frequency response of the loop gain is shown in Fig. 7. GBW and phase margin are around 3 MHz and 60°, respectively. The slight difference of GBW from simulation is attributed to process tolerances. The DC gain has been measured using an oscilloscope, obtaining a value of 57.5 dB. The measured CMRR at DC was 19 dB, in close agreement

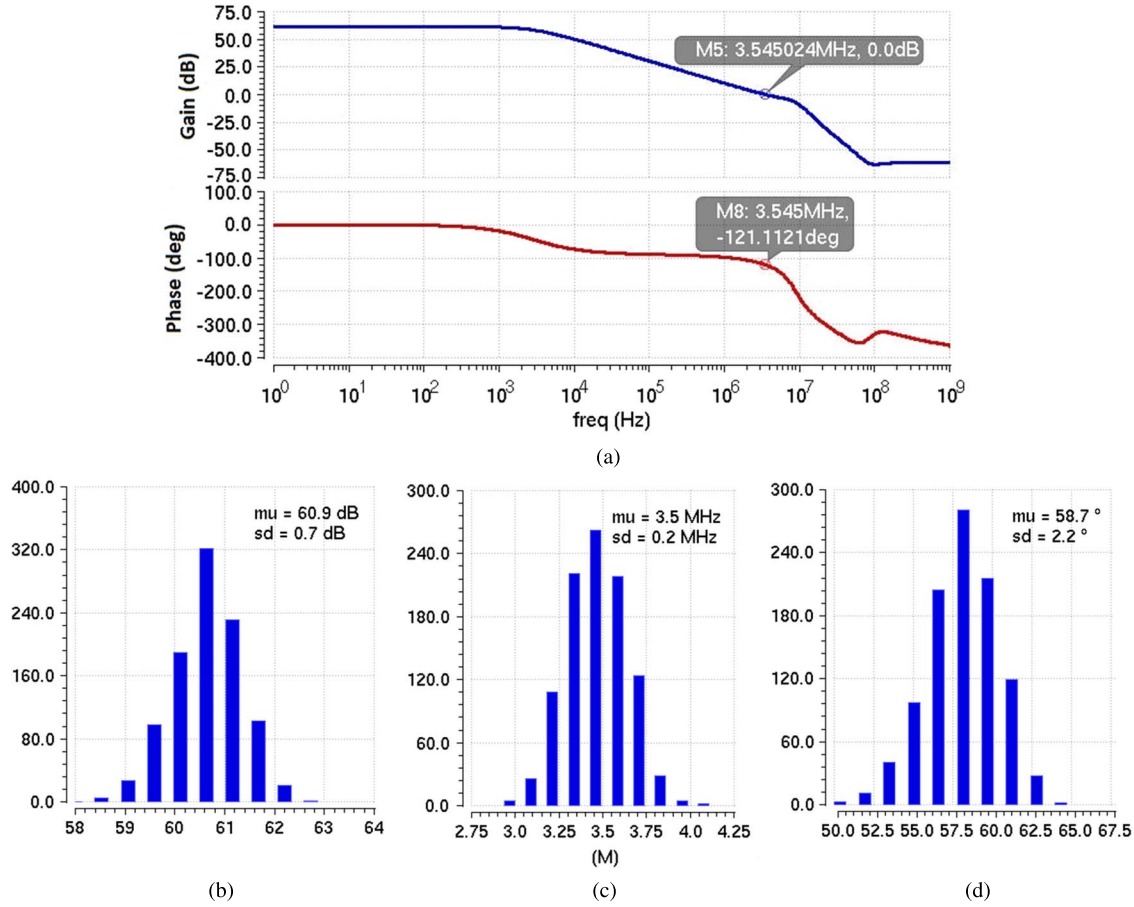


Fig. 6. Postlayout simulations. (a) Nominal open loop frequency response (magnitude and phase) and Monte Carlo results for (b) DC gain, (c) GBW, and (d) phase margin.

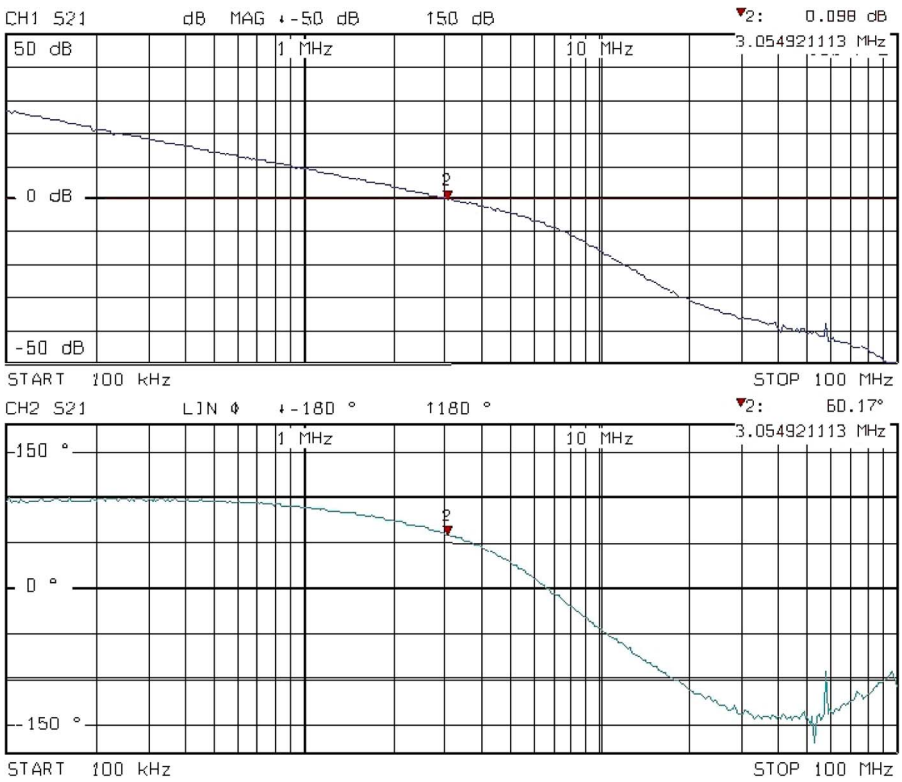


Fig. 7. Measured open loop frequency response (magnitude and phase).

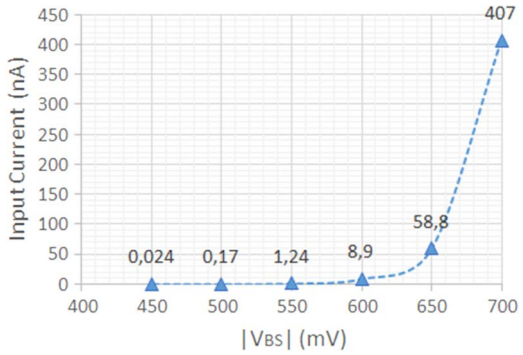


Fig. 8. Measured input current versus bulk-source voltage @ 20 °C.

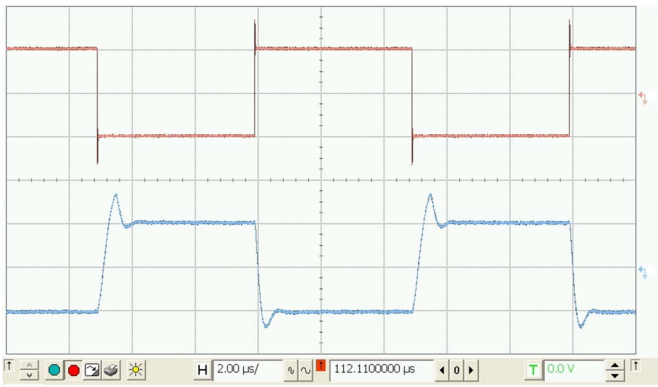


Fig. 9. Measured time response of the OTA in inverting unity gain to an input step of 400 mV.

with (6). The power supply rejection ratio, PSRR, at DC was 52.1 dB/66.4 dB for the positive/negative-supply PSRR, respectively. Regarding gain, CMRR and PSRR, classical measurement schemes have been used. Configurations shown in [27], setup I, were used for the gain and CMRR measurement. PSRR measurement set up is also well known [28].

The input common mode range (ICMR) is, in principle, rail to rail but it is actually limited by the maximum allowed input current that flows into the bulk. Indeed, the maximum input current occurs when V_{BS} is maximum. That means that the ICMR should be restricted in its lower bound and simulations show that ICMR should then be limited to 550 mV (from 150 mV to 700 mV) in order to maintain the input current below 4 nA at 27 °C. Measurements of the input current versus bulk-source voltage, performed at 20 °C are shown in Fig. 8. It can be seen that when $V_{BS} = V_{BS\,\max} = 550$ mV the input current results to be around 1.3 nA. Since bulk current approximately doubles each 10 °C [29], it can be inferred that input current will remain below 100 nA up to 80 °C. It is worth noting that to avoid any latch-up problem conventional layout strategies such as double guard rings have been implemented and that extensive experimental measurements show that latch-up did not occur.

The measured time response to a 400 mV_{pp} input step with the OTA in inverting unity gain configuration is plotted in Fig. 9 (100 kΩ resistors used). The positive and negative slew rate values were 1.8 $V/\mu s$ and 3.8 $V/\mu s$, respectively. Besides, 1% settling time was 1.3 μs (positive step) and 1.0 μs (negative step).

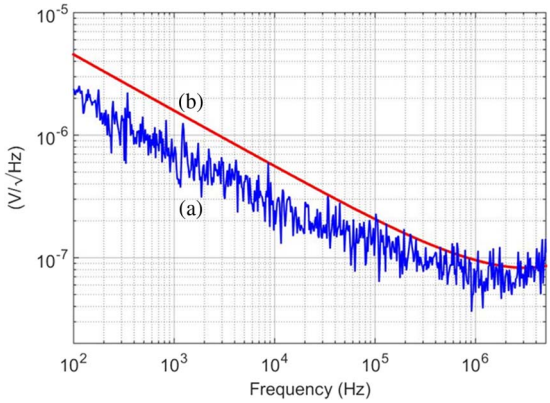


Fig. 10. Measured (a) and simulated (b) input referred noise spectral density versus frequency.

Noise measurements and simulation are shown in Fig. 10. The input referred noise density measured at 1 MHz is around 100 nV/$\sqrt{}$Hz.

In order to carry out a quantitative comparison of the performance achieved through the implemented solution against other sub-1 V amplifiers, the two traditional figures of merit (FoM) [26], [30], [31] shown in (15) have been also evaluated in Table III. FoM_S and FoM_L allow a comparison of small signal and large signal performance, respectively

$$\text{FoM}_S = \frac{\text{GBW} \cdot C_L}{\text{Power}} \tag{15a}$$

$$\text{FoM}_L = \frac{SR \cdot C_L}{\text{Power}}. \tag{15b}$$

It is apparent that the proposed amplifier outperforms almost all other previously reported body-driven OTAs. In particular, as far as parameter FoM_L is concerned, the proposed OTA displays the maximum value, 2204, that is around 2.25 times greater than the best result previously reported [23]. Regarding the FoM_S parameter, the proposed OTA displays the second best result (2361) that is close to the maximum value obtained by [10] i.e., 2700. Fig. 11 shows the comparison in a graphical way.

The OTA main performance is summarized in Table IV. In addition to the parameters discussed before, Table IV includes offset (the maximum value measured from the available samples) and the total harmonic distortion (THD) of the output voltage with the OTA in inverting unity gain for 400-mV_{p-p} input and two different frequencies.

V. Conclusion

The bulk terminal of MOS transistors and its exploitation for low-voltage applications have recently received a renewed interest from analog and digital designers [33]–[38]. In this paper, a high-performance architecture for sub-1 V bulk-driven OTAs has been presented. The proposed solution exploits a three-gain-stage topology and uses a class AB output stage to improve DC gain and drive capability, respectively. A single-ended OTA using the proposed topology and derived design equations was fabricated in a 180-nm standard CMOS technology and experimentally tested. Measurements were found in

TABLE III
PERFORMANCE COMPARISON OF SUB-1 V AMPLIFIERS

Year, reference	Tech. [μm]	Supply [V]	DC Current [μA]	C_L [pF]	DC Gain [dB]	GBW [MHz]	PM [°]	Average SR [V/μs]	FoM_S [MHz·pF/mW]	FoM_L [V·pF/(μs·mW)]
2001 [8]	0.5	1	40	20	69	2	57	0.5	1000	250
2002 [9]	2.5	0.9	0.5	12	70	0.0056	62	-	149	-
2003 [10]	0.25	0.8	10	18	50	1.2	60	0.2	2700	450
2005 [12]	0.18	0.5	220	20	52	2.5	-	2.89	455	525
2007 [13]	0.35	0.6	0.916	15	69	0.011	65	0.014	300	382
2009 [14]	0.35	0.9	11	2.5	62	0.54	52	-	136	-
2013 [15]	0.35	1	197	15	88	11.67	66	1.95	889	148
2014 [17]	0.13	0.25	0.072	15	40	0.002	52	0.0007	1667	583
2015 [23]	0.065	0.5	366	3	46	38	57	43	623	705
		0.35	49	3	43	3.6	56	5.6	630	980
This work	**0.18**	**0.7**	**36.3**	**20**	**57.5**	**3**	**60**	**2.8**	**2361**	**2204**

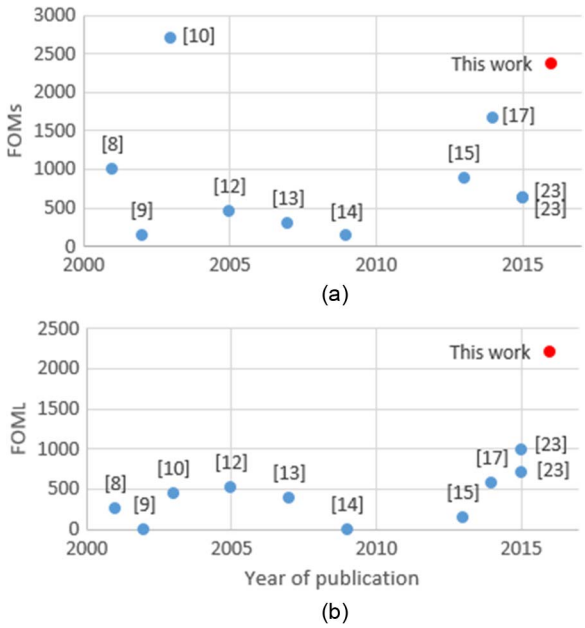


Fig. 11. Figures of merit for: (a) small signal performance and (b) large signal performance.

TABLE IV
MEASURED PERFORMANCE PARAMETERS

Parameter	Value
Supply voltage (V_{DD}-V_{SS}) [V]	0.7
Power dissipation [μW]	25.4
Area [mm²]	$19.8 \cdot 10^{-3}$
Offset (maximum) [mV]	11
ICMR [mV]	550 (from 150 mV to 700 mV)
Max Input Current [nA] @ 20ºC	1.3
Open-Loop DC Gain [dB]	57.5
GBW [MHz]	3
Phase Margin [deg]	60
Gain Margin [dB]	8
SR+/SR- [V/μs]	1.8/3.8
1% Settling Time (+/-) [μs]	1.3/1.0
CMRR@DC [dB]	19
PSRR+@DC [dB]	52.1
PSRR-@DC [dB]	66.4
Input Ref. Noise @1MHz [nV/√Hz]	100
THD @100kHz, 400mV_{p-p} input [%]	0.20
THD@250kHz, 400mV_{p-p} input [%]	0.99

close agreement with the expected results and comparison with other bulk-driven amplifiers demonstrated the excellent small-signal and large-signal performance achieved by the proposed solution. Future work will be aimed to improve CMRR and to balance the positive and negative SR in order to reduce the settling time and drive even larger load capacitors.

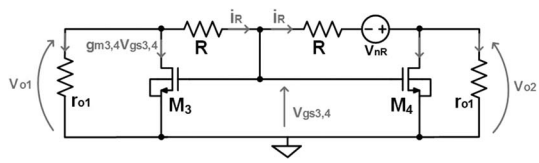


Fig. 12. Simplified schematic for resistors R noise analysis.

APPENDIX

Let us consider the noise generated by the right-side resistor R, which is connected between the gate and drain of M_4 in Fig. 1. The simplified small signal model illustrated in Fig. 12 is utilized to find the voltage gain between v_{nR} and the outputs of the first stage, v_{o1} and v_{o2}.

From inspection of the figure we write the expr essions of i_R, v_{o1}, and v_{o2}

$$i_R = g_{m3,4} v_{gs3,4} + \frac{v_{o2}}{r_{o1}} = -g_{m3,4} v_{gs3,4} - \frac{v_{o1}}{r_{o1}} \tag{A1}$$

$$v_{o1} = v_{gs3,4} + R i_R \tag{A2}$$

$$v_{o2} = v_{gs3,4} - R i_R + v_{nR}. \tag{A3}$$

From (A1)–(A3) we get the transfer functions

$$\frac{v_{o1}}{v_{nR}} = \frac{g_{m3,4}R - 1}{2(1 + g_{m3,4} r_{o1})\left(1 + \frac{R}{r_{o1}}\right)} \approx \frac{1}{2}\frac{R}{R + r_{o1}} \tag{A4}$$

$$\frac{v_{o2}}{v_{nR}} = \frac{1 + g_{m3,4}(R + 2r_{o1})}{2(1 + g_{m3,4} r_{o1})\left(1 + \frac{R}{r_{o1}}\right)} \approx \frac{1}{2}\frac{R + 2r_{o1}}{R + r_{o1}}$$

$$= \frac{1}{2}\left(1 + \frac{r_{o1}}{R + r_{o1}}\right) \tag{A5}$$

where the approximations hold for $g_{m3,4}R \gg 1$ and $g_{m3,4} r_{o1} \gg 1$.

Observe that for the symmetry of the circuit, v_{o1}/v_{nR} represents also the transfer function from the noise source of the left-side resistor to v_{o2}. This noise contribution of the left-side resistor is lower than that of the right-side resistor as can be seen by comparing (A4) and (A5) which imply the product of 0.5 by a quantity lower than the unity and greater than the unity, respectively.

The resistors noise referred to the input is evaluated by considering that the gain from the inverting input to the output of the first stage is $-(1/2)g_{mb1,2}R//r_{o1}$. Therefore we get

$$S_{VR,\text{in}} = S_{VR}\frac{1}{4}\left[\left(\frac{R}{R+r_{o1}}\right)^2+\left(\frac{R+2r_{o1}}{R+r_{o1}}\right)^2\right]\left(\frac{2}{g_{mb1,2}r_{o1}//R}\right)^2$$
$$= 4kTR\left(\frac{1}{g_{mb1,2}r_{o1}}\right)^2\left[1+\left(1+\frac{2r_{o1}}{R}\right)^2\right]. \quad \text{(A6)}$$

The above input-referred resistor noise is used in (12).

REFERENCES

[1] B. H. Calhoun, D. C. Daly, N. Verma, D. F. Finchelstein, D. D. Wentzloff, A. Wang, S. Cho, and A. P. Chandrakasan, "Design considerations for ultra-low energy wireless microsensor nodes," *IEEE Trans. Comput.*, vol. 54, no. 6, pp. 727–740, Jun. 2005.

[2] A. Tabesh and L. G. Fréchette, "A low-power stand-alone adaptive circuit for harvesting energy from a piezoelectric micropower generator," *IEEE Trans. Ind. Electron.*, vol. 27, no. 3, pp. 740–749, Mar. 2010.

[3] A. Romani, M. Filippi, and M. Tartagni, "Micropower design of a fully autonomous energy harvesting circuit for arrays of piezoelectric transducers," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 729–739, Feb. 2014.

[4] R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[5] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," *Annu. Rev. Biomed. Eng.*, vol. 10, no. 1, pp. 247–274, 2008.

[6] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *IEEE J. Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, Jun. 1977.

[7] B. J. Blalock, P. E. Allen, and G. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 7, pp. 769–780, Jul. 1998.

[8] T. Lehmann and M. Cassia, "1-V power supply CMOS cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1082–1086, Jul. 2001.

[9] T. Stockstad and H. Yoshizawa, "A 0.9-V 0.5-μm rail-to-rail CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 286–292, Mar. 2002.

[10] Y. Libin, M. Steayert, and W. Sansen, "A 0.8 V, 8 μm, CMOS OTA with 50-dB gain and 1.2-MHz GBW in 18-pF load," in *Proc. Eur. Solid-State Circuits Conf.*, 2003, pp.297–300.

[11] T. M. Hollis, D. J. Comer, and D. T. Comer, "Optimization of MOS amplifier performance through channel length and inversion level selection," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 52, no. 9, pp. 545–549, Sep. 2005.

[12] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, 2005.

[13] L. H. C. Ferreira, T. C. Pimenta, and R. L. Moreno, "An ultra-low-voltage ultra-low-power CMOS miller OTA with rail-to-rail input/output swing," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 54, no. 10, pp. 843–847, Oct. 2007.

[14] S. W. Pan, C. C. Chuang, C. H. Yang, and Y. S. Lai, "A novel OTA with dual bulk-driven input stage," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2009, pp. 21–24.

[15] L. Zuo and S. K. Islam, "Low-voltage bulk-driven operational amplifier with improved transconductance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 8, pp. 2084–2091, Aug. 2013.

[16] T. Kulej, "0.5-V bulk-driven CMOS operational amplifier," *IET Circuits Dev. Syst.*, vol. 7, no. 6, pp. 352–360, 2013.

[17] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS process," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, Jun. 2014.

[18] P. Monsurrò, S. Pennisi, G. Scotti, and A. Trifiletti, "0.9-V MOS cascode amplifier with body-driven gain boosting," *Int. J. Circuits Theory Appl.*, vol. 37, no. 2, pp. 193–202, 2009.

[19] G. Raikos and S. Vlassis, "0.8-V bulk driven operational amplifier," *Analog Integr. Circuits Signal Process.*, vol. 63, pp. 425–432, Jun. 2010.

[20] G. Raikos and S. Vlassis, "Low-voltage bulk-driven input stage with improved transconductance," *Int. J. Circuits Theor. Appl.*, vol. 39, no. 3, pp. 327–339, Mar. 2011.

[21] Y. Li, C. C. Y. Poon, and Y.-T. Zhang, "Analog integrated circuits design for processing physiological signals," *IEEE Rev. Biomed. Eng.*, vol. 3, pp. 93–105, 2010.

[22] E. Cabrera-Bernal, A. D. Grasso, and S. Pennisi, "0.7-V bulk-driven three-stage class-AB CMOS OTA," in *Proc. NEWCAS 2015*, Grenoble, France, Jun. 2015, pp. 1–4.

[23] O. Abdelfattah, G. W. Roberts, I. Shih, and Y.-C. Shih, "An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail-to-rail input range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2380–2390, Oct. 2015.

[24] A. D. Grasso, D. Marano, G. Palumbo, and S. Pennisi, "Design methodology of subthreshold three-stage CMOS OTAs suitable for ultra-low-power low-area and high driving capability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1453–1462, Jun. 2015.

[25] W. Aloisi, G. Palumbo, and S. Pennisi, "Design methodology of miller frequency compensation with current buffer/amplifier," *IET Circuits Devices Syst.*, vol. 2, no. 2, pp. 227–233, Jan. 2008.

[26] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in reversed nested miller compensation" *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1459–1470, 2007.

[27] J. Zhou and J. Liu, "On the measurement of common-mode rejection ratio" *IEEE Trans. Circuits Syst. II, Express Briefs* vol. 52, no. 1, pp. 49–53, Jan. 2005.

[28] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. Oxford, U.K.: Oxford Univ. Press, 2002.

[29] K. R. Laker and W. M. Sansen, *Design of Analog Integrated Circuits and Systems*. New York, NY, USA: McGraw-Hill, 1994.

[30] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2074–2077, Nov. 2004.

[31] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1515–1520, Jul. 2005.

[32] J. F. Duque-Carrillo, J. L. Ausin, G. Torelli, J. M. Valverde, and M. A. Dominguez, "1-V rail-to-rail operational amplifiers in standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 33–44, 2000.

[33] A. D. Grasso, P. Monsurrò, S. Pennisi, G. Scotti, and A. Trifiletti, "Analysis and implementation of a minimum-supply body-biased CMOS differential amplifier cell," *IEEE Trans. VLSI Syst.*, vol. 17, no. 2, pp. 172–180, 2009.

[34] P. Monsurrò, G. Scotti, A. Trifiletti, and S. Pennisi, "Biasing technique via bulk terminal for minimum supply CMOS amplifiers," *Electron. Lett.*, vol. 41, no. 14, pp. 779–780, Jul. 2005.

[35] P. Monsurrò, S. Pennisi, G. Scotti, and A. Trifiletti, "Linearization technique for source-degenerated CMOS differential transconductors," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 54, no. 10, pp. 848–852, Oct. 2007.

[36] J. Kim, P. M. Solomon, and S. Tiwari, "Adaptive circuit design using independently biased back-gated double-gate MOSFETS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 806–819, Apr. 2012.

[37] M. Meijer and J. P. de Gyvez, "Body-bias-driven design strategy for area- and performance-efficient CMOS circuits," *IEEE Trans. VLSI Syst.*, vol. 20, no. 1, pp. 42–51, 2012.

[38] G. Di Cataldo, A. D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "CMOS non-tailed differential pair," *Int. J. Cir. Theor. Appl.*, vol. 44, no. 7, pp. 1468–1477, Jul. 2016.

Elena Cabrera-Bernal (S'15) was born in Seville, Spain. She received the telecommunication engineering degree and the electronics, signal processing and communications M.Sc degree from the University of Seville, Seville, Spain, in 2011 and 2013, respectively.

Since 2013 she has been with the Department of Electronic Engineering, School of Engineering, University of Seville, where she is currently working towards the Ph.D. degree, granted by the Spanish Government. She was a Visiting Researcher at University of Catania in 2014 and at Imperial College of London in 2015. Her research interests are related to low-voltage low-power analog circuit design and analog and mixed signal microelectronics.

Salvatore Pennisi (M'00–SM'04) received the Laurea degree in electronic engineering and the Ph.D. degree in electrical engineering, both from the University of Catania, Italy, in 1992 and 1997, respectively.

In 1996, he became a Researcher (Assistant Professor) and in 2002 he was appointed an Associate Professor. In 2014 he received the Italian National Scientific Qualification for the position of Full Professor. He teaches undergraduate and graduate courses on microelectronics and basic electronics. His main research interests include circuit theory and analog design with emphasis on low-voltage and current-mode techniques, multi-stage amplifiers, data converters, analysis of high-frequency distortion in analog circuits, driving circuits for liquid crystal displays and micro-energy harvesting. He has published over 80 international journal papers, 120 contributions in conference proceedings, and is the coauthor of the books *CMOS Current Amplifiers* (1999), *Feedback Amplifiers: Theory and Design* (2001), both edited by Kluwer Academic Publishers, and *Liquid Crystal Display Drivers—Techniques and Circuits* (Springer, 2009).

Dr. Pennisi is member of the IEEE CASS Analog Signal Processing Technical Committee and served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS and of the *International Journal of Circuit Theory and Applications*.

Alfio Dario Grasso (S'99–M'03–SM'15) was born in Catania, Italy, in 1978. He received the Laurea degree (*summa cum laude*) and the Ph.D. degree in electronic engineering from the University of Catania, Italy, in 2003 and 2006, respectively.

From 2006 to 2011 he was a Freelance Engineer in the field of electronic systems. From 2009 to 2010 he has held the position of Adjunct Professor of electronics at the University Kore of Enna, Italy. In 2011 he became a Researcher (Assistant Professor) and in 2015 he was appointed an Associate Professor at the University of Catania. He teaches undergraduate and graduate courses on advanced VLSI digital design, microelectronics, and basic electronics.

His current research interests include low-voltage low-power analog circuit design, D/A conversion and analog and mixed signal processing for energy harvesting applications. He has coauthored more than 50 papers on referred international journals and conference proceedings.

Antonio Torralba (M'89–SM'02) received the industrial engineering (M.Sc. in electrical engineering) and Ph.D. degrees from the University of Seville, Seville, Spain, in 1983 and 1985, respectively.

Since 1983, he has been with the Department of Electronics Engineering, School of Engineering, University of Seville, where he was an Assistant Professor, Associate Professor from 1987 to 1996, Professor since 1996, and since 2008 he is the Director of the Department, where he leads a research group on mixed signal design. In 1999, he was a Visiting Researcher in the Klipsch School of Electrical Engineering, New Mexico State University, Las Cruces, NM, USA, and in the Department of Electrical Engineering, Texas A&M University, College Station, TX, USA. He is coauthor of 90 papers in international journals and his research interests include low power low voltage analogue and mixed signal microelectronics.

Ramón Gonzalez Carvajal (M'99–SM'04) was born in Seville, Spain. He received the Electrical Engineering and Ph.D. degrees (hons) from the University of Seville, Seville, Spain, in 1995 and 1999, respectively.

Since 1996, he has been with the Department of Electronic Engineering, School of Engineering, University of Seville, where he actually holds the position of professor since 2008. Dr. Gonzalez Carvajal has been visiting professor in research centers like Texas A&M University, New Mexico State University, The Imperial College of Engineering and Medicine (London), University of Catania or INAOE. He also holds the position of Adjunct Professor at the Klipsch School of Electrical Engineering, NMSU. He is co-author of ten patents, five of them under exploitation contract. He has published more than 300 research works, including 100 journal indexed papers. He has also participated in more than 70 research projects funded by organizations like NASA, National Science Foundation, EPSRC, EUREKA or the European Framework Program, among others. His research interests are related to low-voltage low-power analog circuit design, A/D and D/A conversion, and analog and mixed signal processing. Between 2009 and 2015 he has hold the positions of Vice-rector of Technology Transfer, General manager of the Research Foundation, and coordinator of the Excellence Campus AndalucTECH at the University of Seville.