# Flexible ΣΔ Modulators for Multi-Standard Wireless Transceivers: Novel Architectures and Circuit Solutions

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The increasing number of wireless standards and applications demands for transceivers capable to handle different sets of specifications, signal conditions and battery status. The trend is towards a maximum hardware reuse, by making as many transceiver building blocks as possible, digitally programmable, reconfigurable and suitable to be integrated in mainstream nanometer CMOS technologies [1]. One of the most challenging building blocks in such *multi-standard* transceivers is the Analog-to-Digital Converter (ADC), because of the varying sampling rates and resolutions required to digitize the wide range of signals corresponding to each individual operation mode [2]. The majority of reported multi-standard ADCs uses the ΣΔ Modulation (ΣΔM) technique, being the most commonly applied reconfiguration strategy just changing the OverSampling Ratio (OSR) according to the operation standard [3]. However, the increasing demand for high data rates in new standards restricts oversampling to low values, what forces to increase the noise-shaping filter order and/or the number of bits of the internal quantizers.

This work contributes to this topic and presents two novel ΣΔMs capable to reconfigure themselves with optimized power consumption. The first chip —designed and fabricated in a 0.13μm CMOS technology— is intended to cope with the main requirements of cellular and short-distance communication standards [3], while the second ΣΔM —designed in a 90-nm CMOS technology— faces the paradigm of 4G receivers, defined as the inclusion of wireless communication standards (such as WiMax and WLAN) together with the cellular ones [4].

Fig. 1(a) shows the microphotograph of the first chip. This prototype adjusts the biasing of the embedded folded-cascode amplifiers, the sampling frequency (fs), the filtering order and the resolution of the last-stage quantizer to get the required performance with adaptive power consumption. These reconfiguration strategies allow this modulator to adapt its performance to the required specifications. This is illustrated in Fig. 1(b) that shows the measured Signal-to-(Noise+Distortion) (SNDR) curves for all operation modes covered by this chip.

The second design, whose block diagram is shown in Fig. 2, extends the underlying principle of SMASH ΣΔMs to the implementation of global resonation while Unity Signal Transfer Function (USTF) is used in all stages of the modulator [5]. This implies a reduction in the requirements of the amplifiers in terms of DC gain, gain non-linearity and output swing. Besides, the use of adaptive resonation allows to enlarge the resolution when demanded. Moreover, this novel architecture employs a digital adder to implement an inter-stage feed-back path that allows to remove the digital cancellation logic —required in conventional cascade modulators— while the analog adders are used to obtain the USTF at each stage.

Both modulators use reconfigurable folded-cascode amplifiers with adaptive biasing. Indeed, as a result of the architectural-level strategies implemented in the second design, their embedded opamps demand very low DC gain —less than 35dB for all amplifiers. Another appealing feature of this last modulator architecture is the great reduction in the opamp output swing requirements —with maximum respective swings of 1.2V (reference voltage value for both ΣΔMs) and 0.4V for the first and second design— due to the use of USTF in all stages.

At the time of writing this abstract, the first design has been fabricated and measured while the second modulator is not fully electrically implemented yet. However, all its building blocks are already designed at transistor level. In fact, power estimations of all these blocks are done based on their electrical designs while taking into account their corresponding loads and operation frequencies.

Table I summarizes the performance of both designs, considering experimental measurements for the first one and time-domain behavioral simulations (including main non-ideal effects extracted from electrical simulations) for the second one. Both circuits comply with the specifications of the targeted wireless standards, and feature a competitive performance with cutting-edge state-of-the-art reconfigurable ΣΔMs [3], showing the benefits of using the proposed reconfiguration strategies at both architectural- and circuital-level.

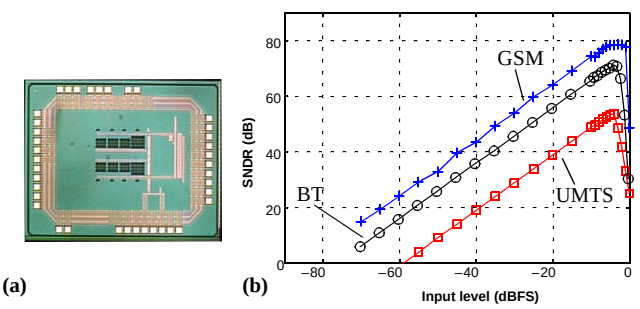


**Figure 1.** (a) Chip microphotograph, (b) Measured SNDR curves.

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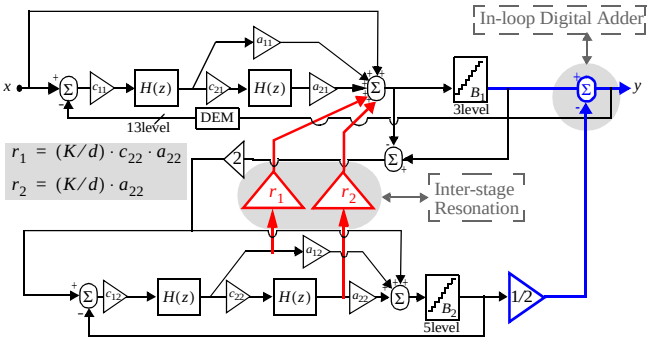


**Figure 2.** Second proposed ΣΔM architecture.

TABLE I. PERFORMANCE SUMMARY.

| Standard | OSR | fs (MHz) | Architecture | Peak SNDR (dB) | DR (dB) | Power Cons. (mW) | Process | Core Area | Supply Voltage |
|---|---|---|---|---|---|---|---|---|---|
| **First prototype (Measured results)** | | | | | | | | | |
| **GSM** | 100 | 40 | 2-1 | 77.8 | 82.3 | 25.2 | 130nm CMOS | 1.4mm$^2$ | 3.3V |
| **BT** | 20 | | 2-1-1 (2b) | 71.3 | 75.9 | 25.0 | | | |
| **UMTS** | 10 | 80 | | 53.7 | 58.7 | 44.5 | | | |
| **Second prototype (Estimated simulation-based results)** | | | | | | | | | |
| **GSM** | 200 | 40 | 2 | 80.2 | 90.0 | 4.1 | 90nm CMOS | 0.7mm$^2$ | 1.2V |
| **BT** | 80 | 80 | | 75.6 | 79.3 | 5.8 | | | |
| **UMTS** | 40 | 160 | | 65 | 69.4 | 8.7 | | | |
| **DVB-H** | 20 | | 2-2 | 70.0 | 74.3 | 14.9 | | | |
| **WiMax** | 12 | 240 | | 63 | 67.5 | 20.5 | | | |
| **WLANa** | 16 | | | 68 | 72.0 | 21.5 | | | |
| **WLANn** | 8 | 320 | 2-2 K=0.5 | 62.1 | 65.1 | 23.5 | | | |