Digital Test for the Extraction of Integrator Leakage in 2nd and 1st order ΣΔ Modulators

Gildas Leger, Adoración Rueda

Instituto de Microelectrónica de Sevilla (IMSE-CNM), Universidad de Sevilla
c/ Tarfia, s/n 41011 Sevilla (SPAIN)
Tel: +(34) 955056666
e-mail: {leger,rueda}@imse.cnm.es

***Abstract*— This paper proposes a digital technique to evaluate the integrator leakage within 1st and 2nd order ΣΔ modulators. Integrator leakage is known to be related to the converter precision and belongs to the basic set of design specifications. The technique proposed here involves very few hardware, which makes it specially suitable for Built-In Self-Test (BIST) implementation. Moreover, the integrator leakage evaluation allows its digital correction in cascaded modulators.**

***Index Terms*— ΣΔ modulators, testability, BIST**

I. Introduction

Analog to digital converters (ADCs) based on ΣΔ modulation can be found in a wide variety of systems. Indeed, when oversampling is affordable they are often the best ADC candidate in terms of cost/performance ratio. This consideration alone justifies the research effort to provide simple and cost effective solution to enhance the testability of such a widespread mixed-signal building block.

The test of ΣΔ modulators is not a trivial task and is faced to important issues. One of them is that these converters usually reach high resolutions, for which it is difficult to provide reliable stimuli. Moreover, the result analysis usually requires complex operations such as FFT (Fast Fourier Transform), sine-fit or histogram acquisition that are carried out over the filtered and decimated modulator bitstream [1].

Integrator leakage is known to be related to the converter precision and belongs to the basic set of design specifications, as it is related to the integrator amplifier DC gain. The effect of integrator leakage in a first order modulator is well-known as it is shown to stabilize the modulator limit-cycles over a range of DC input values, resulting in a precision loss [2][3]. Actually [4] shows that for high oversampling ratio the performance penalty due to integrator leakage can dominate the total noise power in some cases. Similarly, in chapter 3 of [5], the authors derive an expression of the SNR (Signal to Noise Ratio) loss due to leakage for a generic single-loop ΣΔ modulator.This paper proposes a fully digital technique to evaluate integrator leakage in 1st and 2nd order ΣΔ modulators. The stimulus is a digital sequence that can easily be generated on-chip or provided by a digital tester, and the test signature is derived by a simple counter that operates directly on the output bitstream The proposed technique is not for a functional characterization of the circuit; neither is it a defect-oriented test. It could be better described as a specification-driven structural test. Therefore it could be used as a production screening test, because it allows the use of digital ATE (Automatic Test Equipment) and provides a simple signature to reject bad circuits. The low complexity of the presented scheme also makes it specially suitable for Built-In Self-Test (BIST) purpose. Thus, it could be used to provide in-field periodic testing in order to assess if important drift has been produced in the circuit. Moreover, as the test realizes an evaluation of the integrator leakage it can be used for diagnosis or even for correction/calibration purpose.

The proposed test technique can be used in any application that contains 1st and/or 2nd order ΣΔ modulators as stand-alone parts, or in a cascaded modulator. In particular, first order modulators have been recently proposed as good candidates of signal digitizer for test purpose in complex SoCs (System-on-Chip) [6],[7]. It has also been stressed that such modulators should also be checked [8], in order to avoid improper operation.

The paper is structured as follows: Section 2 presents the mathematic foundation of the test principles for 2nd order modulators, multibit 1st order and single-bit 1st order modulators; Section 3 deals with the hardware requirements of the technique; Section 4 presents an example of the test application to a cascaded 2-1 modulator; Section 5 provides a short discussion of the technique and Section 6 presents the conclusions of the paper.

II. Test principles

The test scheme proposed in this paper is sketched in Figure 1. The modulator input is a periodic digital sequence and the test output is a signal carrying information on the difference between the mean value of the input signal and of the output bitstream.

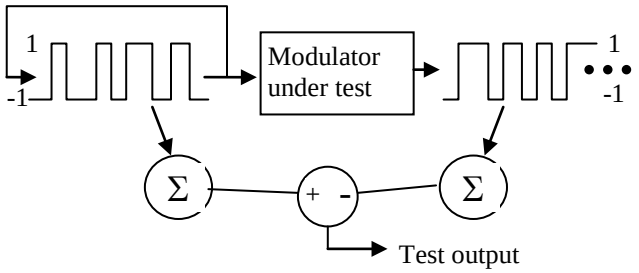

Figure 1: Test principle

The idea of using digital sequences as stimuli had already been proposed in [9] and [10]. Nevertheless, the authors used either a pseudo-random sequence or a ΣΔ encoded sine-wave as proposed in [11]. In this paper, however, a simple periodic sequence with non-zero mean value is used. The simplest example of such a sequence would be the sequence 11-1. The mean value of such a sequence is 1/3.

The basic principle of the proposed test is that the deviation of the output bitstream average from the input sequence mean value can be related to the modulator integrator leakage. If a linear model can be used to describe the modulator behavior, this relation can be easily derived.

The linear model of a modulator assumes that the quantization error is uncorrelated to the input signal, is uniformly distributed over [-Δ/2,Δ/2] (being Δ the quantization step of the modulator) and has a flat power spectral density (is white). The conditions for the application of the linear model have been drawn by Benet and can be found in [12]. These conditions are almost never fulfilled, and a digital sequence is far from being an ideal input from this viewpoint. Nevertheless, it will be shown that a linear model could apply to 2nd order modulators and mutibit 1st order modulators. However, in the case of a single-bit 1st order modulator, the linear model is far from describing the exact behavior and a specific treatment will be required.

1) Test of Second order modulators

The linear model for a second order ΣΔ modulator is presented in Fig. 2, where the quantizer is replaced by an additive white noise and a gain *k*. This term is introduced because the gain of a one-bit quantizer is undefined. Authors in [13] show that this gain is signal dependent and settles to the value that best decorrelates the quantization noise from the input signal. The leakages of the first and second integrator are modeled in Figure 2 by the terms p_1 and p_2 respectively. For an ideal modulator, these terms should be 1. In the following, an alternative expression $p_i=1-\Delta p_i$ will also be used for the integrator leakages, in order to simplify the notations. The coefficients g_1, g_2, g_1^*, g_2^*, have to be properly chosen such that the modulator fulfils the ideal second order transfer function,

$$Y = z^{-2}X + (1-z^{-1})^2 E \tag{1}$$

For this to be done, the following set of equations has to be verified,

$$\begin{aligned} kg_1g_2 &= 1 \\ kg_2^* &= 2 \\ kg_2g_1^* &= 1 \end{aligned} \tag{2}$$

One well-known solution [14] is to take half gain and full-scale feedback for both integrators (that is $g_1=g_2,=g_1^*=g_2^*=0.5$). In that case, the quantizer equivalent gain is shown to settle to 4 and (2) is fulfilled.

As was pointed out in [15], the first integrator leakage is proportional to the deviation of the output bit stream mean value from the input sequence mean value. Taking into account that p_1 and p_2 are different from one, an expression of the counter giving the deviation of the output bit stream sum over *N* samples from the input sum over *N* samples can easily be drawn from the model in Figure 2 [15]. It comes,

$$counter = \sum_{n=2}^{N+1} x_{n-2} - \sum_{n=2}^{N+1} y_n = \frac{\Delta p_1(2+\Delta p_2)\sum_{n=2}^{N+1} x_{n-2}}{1+\Delta p_1(2+\Delta p_2)} + Err \tag{3}$$

The error term *Err* depends mostly on the sum of the quantization error, which is white. Therefore, this error term remains bounded. If the sum is realized over a number of samples *N*, multiple of the input sequence period and sufficiently large, whenever the leakage of the integrators are small the counter output reduces to,

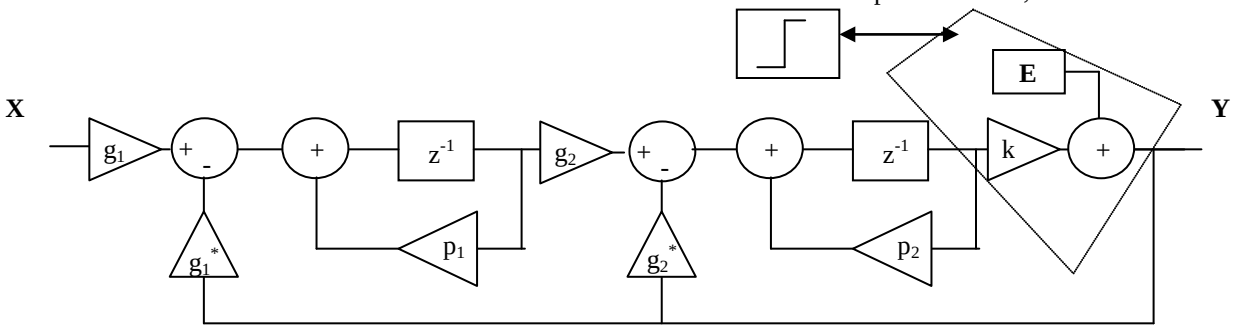

Figure 2: Linear model for a second order ΣΔ modulator

$$counter \approx 2NQ\Delta p_1 \quad (4)$$

where Q is the input sequence mean value. Notice that the counter state gives a measurement of the first integrator leakage.

If the modulator has a non-negligible input-referred offset, the counter output is modified as follows,

$$counter \approx -Noff + 2NQ\Delta p_1 \quad (5)$$

Therefore, the counter output depends on more than one parameter. The influence of the offset can be easily neutralized running the test with the opposite sequence. A new counter output is obtained,

$$ncounter \approx -Noff - 2NQ\Delta p_1 \quad (6)$$

By combining (5) and (6), it comes,

$$\Delta p_1 \approx \frac{counter - ncounter}{4NQ} \quad (7)$$

and

$$off \approx \frac{counter + ncounter}{-2N} \quad (8)$$

In order to validate these results, 500 simulations have been performed with Matlab SIMULINK using the model of Figure 2. The input sequence was set to [1111-11111-11], whose mean value is 7/11. For each simulation, an input-referred offset in the range [-1.10^{-3};1.10^{-3}] and a Δp value in the range [0;0.01] were randomly selected. The error between the actual simulated value and the measured value through (7) and (8) was calculated. Table 1 summarizes the obtained results for two cases: a count over 6600 samples and over 33000 samples.

	N=6600	**N=33000**
Mean offset error	$8.3\ 10^{-6}$	$9.6\ 10^{-6}$
Standard deviation of the offset error	$5.9\ 10^{-5}$	$1.4\ 10^{-5}$
Mean Δp error	$1.3\ 10^{-4}$	$7.2\ 10^{-5}$
Standard deviation of the Δp error	$1.1\ 10^{-4}$	$5.8\ 10^{-5}$

Table 1: Error between the simulated and evaluated parameters for a 2nd order modulator

It appears clearly that the measurement error is very small and can be reduced by increasing the number of count samples.

For the estimation of the second integrator leakage, a different scheme should be employed. A possible way is disable the first loop and input the digital test sequence directly to the second integrator. A first order modulator is thus obtained that can be tested as explained in the next subsection.

2) Test of first order modulators

Applying the proposed test to the first order modulator is not straightforward, due to its highly non-linear behavior. Let us consider, first of all, the case of multibit 1st order modulators. For these modulators, the linear description still stands to some extent. This linearized model is shown in Fig. 3. Notice that the signal dependent gain k that was introduced to model a single-bit quantizer has been removed as the gain of a multibit quantizer is precisely defined by its transitions. A consequence of this is that the integrator must also have a unity gain to match the ideal 1st order equation.

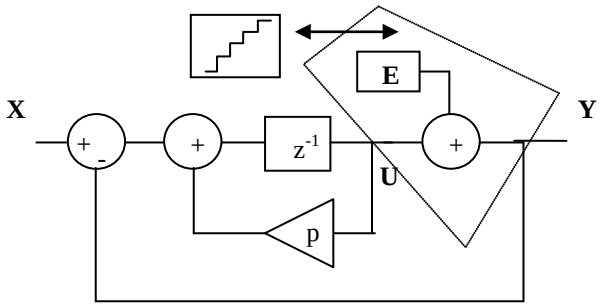

Figure 3: Linear model for a 1st order ΣΔ modulator

From this model, the same reasoning as for the second order modulator can be carried out, and the deviation of the output bit stream mean value from the input sequence mean value Q can be written, in a first order approximation, as

$$counter = NQ\Delta p \quad (9)$$

where N is again the number of samples, Q the input sequence mean value and $\Delta p = 1 - p$ the integrator leakage.

In the same way as for the 2nd order modulator, the influence of an input-referred offset could be neutralized by running the test with two opposite sequences. Then, the parameters are measured as,

$$\Delta p \approx \frac{counter - ncounter}{2NQ} \quad (10)$$

and

$$off \approx \frac{counter + ncounter}{-2N} \quad (11)$$

Nevertheless, the usage of the linear model is restricted to some sequences, namely the one that have a mean value higher than Δ/2, being Δ the quantizer step. Such sequences manage to stimulate more than the two extreme levels of the feedback DAC (Digital-to-Analog Converter), which is a key factor for the model to be applied.

In order to understand this, a close look must be taken at the leakage influence. It has been shown in [16] that 1st order ΣΔ modulation is a projection. This means that the modulator response to a digital sequence is the same digital sequence. This can be demonstrated through the behavioral equation of the modulator,

$$u_{n+1} = u_n + x_n - Quant(u_n) \quad (12)$$

Where *Quant* represents the quantization function, x is the input sequence and u is the integrator output.

An obvious solution to this is,

$$u_{n+1} = x_n + \alpha \tag{13}$$

where α is such that,

$$Quant(x_n + \alpha) = Quant(x_n) = x_n \tag{14}$$

which is equivalent to

$$\alpha \in [\frac{-\Delta}{2}; \frac{\Delta}{2}] \tag{15}$$

being Δ the quantizer step.

The modulator output $y_n=Quant(u_n)=x_{n-1}$ follows the input, as was stated in [16]. In the presence of integrator leakage, however, this behavior is slightly altered. Indeed, the leakage can be seen as a small perturbation that tends to push the integrator output (noted *U* in Figure 3) towards zero. The modulator output will follow the input while $Quant(u_n)=x_{n-1}$. This condition is broken when the decrease due to integrator leakage is such that u_n excites another transition than the two extreme ones. Nevertheless, it can be shown that in some cases, this condition is never broken and the output always follows the input, loosing any sensitivity to integrator leakage.

While the pattern is maintained, $Quant(u_n)=x_{n-1}$ and the integrator output can be expressed as,

$$u_{n+1} = pu_n + x_n - x_{n-1} \tag{16}$$

Therefore, if the input sequence *x* has a period of *L* samples, the decay over one period can be expressed as,

$$u_{(k+1)L+j} = p^L u_{kL+j} + \beta_j$$
$$\beta_j = \sum_{i=0}^{L-1} p^i (x_{j-1-i} - x_{j-2-i}) \quad j \in [1; L] \tag{17}$$

The terms β_j can be calculated exclusively from the input sequence. It can thus be seen that the integrator leakage actually pushes the integrator output towards zero through the term p^L, but the actual decay depends also on β. Actually, β can counteract the effect of p^L. If β is positive for a negative u_n, there may be a stable solution u^s such that,

$$u_{kL+j} = u_j^s \quad \forall k$$
$$u_j^s = \frac{\beta_j}{1 - p^L} \tag{18}$$

For that solution to be stable, it must verify (14), that is,

$$Quant(u_j^s) = x_{j-1} \Leftrightarrow \left\{ \begin{array}{lll} u_j^s > 1 - \frac{\Delta}{2} & if & x_{j-1} = 1 \\ u_j^s < -1 + \frac{\Delta}{2} & if & x_{j-1} = -1 \end{array} \right\} \tag{19}$$

In order to ease the interpretation for any sequence, the study can be restricted for values of *p* close to 1 (small leakage). Then, by taking $p=1-\Delta p$, we get,

$$u_j^{s\infty} = \lim_{\Delta p \to 0} u_j^s = \frac{-\sum_{i=1}^{L-1} i(x_{j-1-i} - x_{j-2-i})}{L} = -Q + x_{j-1} \tag{20}$$

In this case, the stability condition for the output sequence to follow the input sequence (19) becomes,

$$|Q| < \frac{\Delta}{2} \tag{21}$$

Notice that for a one-bit quantizer Δ=2 and the stability condition is always fulfilled, meaning that for any input sequence, the output will always follow the input. That is consistent with the result of [16]. The condition (21) can be better understood taking a look at Figure 4. A 2-bit quantizer modulator is simulated for 200 input sequences with different mean value, over 4000 points. The output bit stream average is represented against the input sequence mean value for three values of integrator leakage, namely p=0.8, 0.9 and 1. It can easily be seen that the three curves collapse to the leakage-free case for small input sequence mean values. Actually, it can be seen that the limit value corresponds to Δ/2=0.25 as expected.

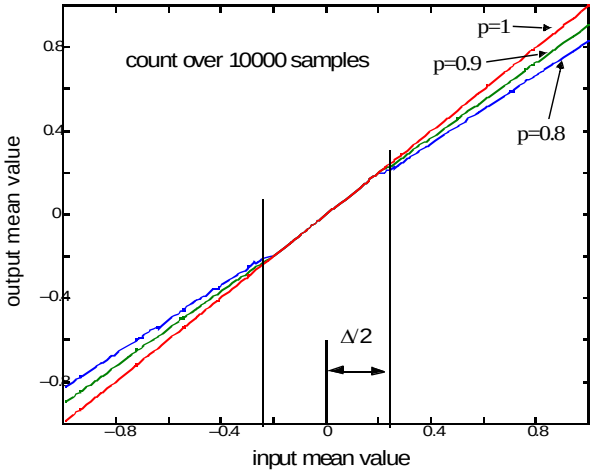

Figure 4: Input/Output mean value transfer function for a 2-bit first order ΣΔ modulator, for 3 values of integrator leakage

If a proper sequence with mean value superior to Δ/2 is chosen, the linear model of Figure 3 applies and so do the equations (10) and (11), making possible the measurement of Δp with the proposed method. The same kind of validation simulations as for the second order modulator has been carried out, for a 1st order modulator with a 3-bit quantizer. The input test sequence had a mean value of 9/11, which is higher than Δ/2=1/4. For each of the 500 simulations, an input-referred offset in the range $[-1.10^{-3};1.10^{-3}]$ and a Δp value in the range [0;0.01] were randomly selected. The error between the actual simulated value and the measured value through (10) and (11) was calculated. Table 2 summarizes the obtained results for a count over 550 samples and over 8800 samples.

	N=550	N=8800
Mean offset error	$6.6\ 10^{-6}$	$9.5\ 10^{-7}$
Standard deviation of the offset error	$1.4\ 10^{-4}$	$1.2\ 10^{-5}$
Mean Δp error	$7.8\ 10^{-5}$	$6.9\ 10^{-5}$
Standard deviation of the Δp error	$1.5\ 10^{-4}$	$5.1\ 10^{-5}$

Table 2: Error between the simulated and evaluated parameters for a 1st order 3-bit modulator

It can be seen that the simulations match the expected results as the measurement error is very small. Moreover, the precision of the measurements improves with the number of count samples *N*.

In the case of a single-bit modulator, the linear model does not apply in any way and its behavior is better described by non-linear dynamics. The best known example of such a complex behavior is probably the modulator DC transfer function. Indeed, it has been shown that this transfer function is the function known as Devil's staircase [2]. It reflects the fact that in the presence of integrator leakage, DC input values close to rational numbers lock into a limit cycle that is a periodic bit stream sequence. As was seen in the case of the multibit modulator study, if a digital sequence is applied at the input of a single-bit 1st order modulator its output bitstream follows the input, whatever the value of the integrator leakage. That was pointed out in [16] and is verified using (21). Therefore the test procedure described at the beginning of this section will require a slight modification.

Conceptually, it seems that the feedback is too tight to allow any deviation from the input sequence. As the first order modulator under normal operating conditions is very robust to non-idealities, what is proposed is to relax the feedback and bring the modulator out of its normal operation, in over-range. For this to be done, an extra delay is introduced in the feedback path, as shown in Figure 5.

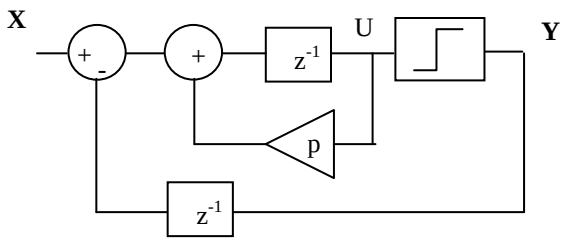

Figure 5: Model of the modified 1st order ΣΔ modulator

Then, the same procedure is used to evaluate the integrator leakage. A sequence with a non-zero mean value is fed to the modulator, and the output bitstream mean value depends on the integrator leakage. Nevertheless, the reasoning to derive this relation is not as simple as for the second order modulator as the linear model cannot be used. Actually, the output bitstream mean value will reveal to be a complex non-linear function of the integrator leakage. Fortunately, a Taylor development of this function for a small leakage will ease its evaluation.

The reasoning that has to be followed to derive the relation between the integrator leakage and the output bit stream mean value is similar to the one that was carried out to derive the validity range of input sequences in the case of a multibit modulator. In the ideal case of an integrator with no leakage, the modified modulator output bitstream is periodic and its mean value is equal to the input sequence mean value. Moreover, the integrator output u_n follows a periodic pattern on three levels,

$$u_n = \gamma + \begin{bmatrix} 2 \\ 0 \\ -2 \end{bmatrix} \quad ,|\gamma| < 2 \tag{22}$$

If the integrator is leaky, a decay will be superposed to that pattern just like in the case of the multibit modulator. However, in the case of the multibit modulator it was possible to solve the modulator equation for finding the pattern. But when an extra delay is introduced in the feedback loop, it becomes very difficult to derive a general solution for any input sequence. Therefore, we limit our study to sequences of the form L-1 "1" and 1 "-1". For such sequences, it can be shown (doing a case analysis in the time domain) that the integrator output pattern is of the form shown in Figure 6. The pattern period (of length 2L) begins with L samples at a central level γ strictly positive and inferior than 2. The 2 next samples are at γ-2 and are thus negative. The following sample brings the integrator output back to the central level γ and the remaining L-3 samples are at level γ+2. The modulator output is equal to the sign of the integrator output, $y_n=sign(u_n)$, and consists of L "1", 2 "-1" and L-2 "1". The modulator output mean value is thus (L-2)/L, which is equal to the input sequence mean value *Q*.

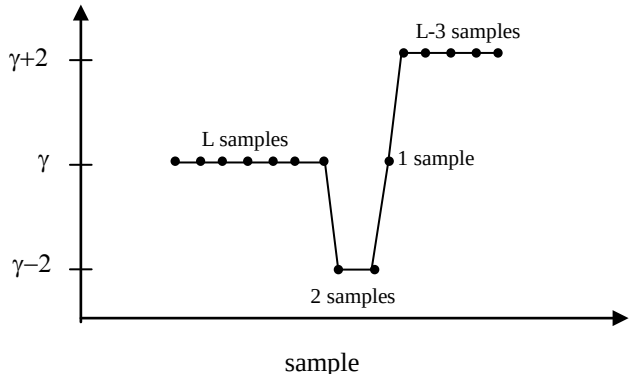

Figure 6: Integrator output pattern for an input sequence with L-1 "1" and 1 "-1"

For a leaky integrator, a small decay perturbs the ideal pattern. If this decay is sufficient to make the central level cross zero, the pattern is broken and the modulator output is modified. When the central level crosses zero, the integrator output experiments transition of the form shown in Figure 7.

This transition (of length L) brings the central level (γ in Figure 6) back to 2, and the integrator output enters in a new cycle of decaying patterns. The first two samples of this transition are close to zero but negative. The third sample is close to 2 and the following L-3 samples are close to 4. Then the modulator output during the transition is 2 "-1" and L-2 "1" and its mean value is (L-4)/L.

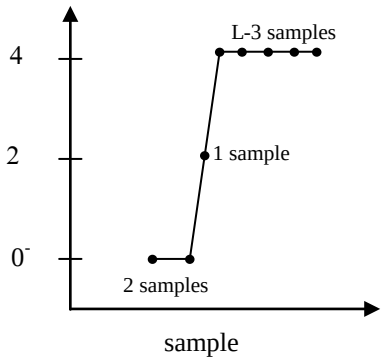

Figure 7: Integrator output transition between two pattern periods

Thus the counter output measuring the deviation of the output bitstream from the input bitstream can be written as,

$$counter = LN_{tran}\frac{(L-2)}{L} - LN_{tran}\frac{(L-4)}{L} = 2N_{tran} \qquad (23)$$

Where N_{tran} is the number of transitions over the record length N. In order to calculate explicitly N_{tran}, one must find in how many pattern periods the central level decays from 2 to 0.

Let u_{2jL} be the integrator output at the beginning of a pattern period. From the behavioral model of Fig. 5, it can be shown that the integrator output at the beginning of the next pattern period will be,

$$\begin{aligned} u_{(j+1)2L} &= p^{2L}u_{j2L} + \alpha \\ \alpha &= -2 + 2p^{L-2} + 2p^{L-3} - 2p^{L} \end{aligned} \qquad (24)$$

If α compensates the decay due to the term p^L, the modulator can lock into a stable pattern, just like it has been seen for the multibit 1st order modulator. This occurs if the solution u_s of the equation ,

$$u_s = p^{2L}u_s + \alpha \qquad (25)$$

is of the adequate sign. As u_{j2L} must correspond to a positive output, the lock condition can be written,

$$u^s = \frac{\alpha}{1-p^{2L}} > 0 \qquad (26)$$

By taking the limit of this value when p tends to 1, it comes,

$$u^{s\infty} = \frac{5-L}{L} > 0 \Leftrightarrow L < 5 \qquad (27)$$

Therefore, in order to get sensitivity to integrator leakage, that is, for the modulator not to lock into a fixed pattern, a sequence of length higher than 5 should be used.

If u_{mid} is the value of the medium level just after a transition, the integrator output after k pattern periods is,

$$u_{2kL} = p^{2kL}u_{mid} + \alpha\frac{1-p^{2kL}}{1-p^{2L}} \qquad (28)$$

Actually, the transition will bring the central level to a value u_{mid} slightly lower than 2. This level can be calculated, taking into account that the first point in the transition in Figure 7 is zero. It comes,

$$u_{mid} = -2 + 2p^{L-2} + 2p^{L-3} \qquad (29)$$

Then, the number of pattern periods between two transitions is the solution of, $u_{2kL}=0$, which is, using (28)

$$k = \left\lceil \frac{\ln\left(\dfrac{\alpha}{\alpha-(1-p^{2L})u_{mid}}\right)}{2L\ln(p)} \right\rceil \qquad (30)$$

Therefore, N_{tran} can be written as,

$$N_{tran} = \left\lfloor \frac{N}{2Lk+L} \right\rfloor \qquad (31)$$

taking into account that the pattern period has a length of $2L$ samples and the transition of L samples. The counter output can thus be written explicitly using (23), (30) and (31) as,

$$counter = 2\left\lfloor \frac{N}{2L\left(\left\lceil \frac{\ln\left(\frac{-2+2p^{L-2}+2p^{L-3}-2p^{L}}{-2+2p^{L-2}+2p^{L-3}-2p^{L}-(1-p^{2L})(-2+2p^{L-2}+2p^{L-3})}\right)}{2L\ln(p)} \right\rceil +1\right)} \right\rfloor \qquad (32)$$

This is a strongly non-linear function of p, but it can be simplified, assuming that $\Delta p=1-p$ is small. It can be shown that,

$$counter \xrightarrow[\Delta p\to 0]{} \frac{2N\Delta p}{\ln\left(\dfrac{5-3L}{5-L}\right)} \qquad (33)$$

Here again, if a small input-referred offset is present at the modulator input the result will be slightly modified. Actually, the offset contribution has to be taken into account in the calculation of α in (24). If *off* is the input referred offset, it comes,

$$\alpha = -2 + 2p^{L-2} + 2p^{L-3} - 2p^{L} + off\,\frac{1-p^{2L}}{1-p} \qquad (34)$$

This new α has thus to be plugged in (30) Nevertheless, some care must be taken if the offset compensate the decay. Taking a close look at the lock condition (26), it can be seen that there is a domain (*off*, *p*) where the modulator will lock to the input sequence. This will translate in that the term in the logarithm of the numerator in (30) becomes negative. This is not numerically valid, and one should thus take it as zero. Therefore, *k* tends to infinity and the counter output to zero. That is consistent with what was said, as the output locks into the fixed pattern which has a same mean value as the input.

If the input referred offset is sufficiently small, one can still

use a first order approximation,

$$counter \xrightarrow[\Delta p \to 0]{} \frac{2N\Delta p}{\ln\left(\frac{5-3L}{5-L}\right)} + Noff \qquad (35)$$

Here again, testing with two opposite sequences will allow to compensate the offset, and we should thus have,

$$\Delta p \approx \frac{counter - ncounter}{4N} \ln\left(\frac{3L-5}{L-5}\right) \qquad (36)$$

and

$$off \approx \frac{counter + ncounter}{-2N} \qquad (37)$$

One drawback of this method is that, as two opposite sequences are used, the input referred offset will tend to compensate the leakage effect for one of the two. Thus the linearity of the counter output may be severely compromised. Another solution could be to calculate the parameters using two sequences of different lengths (L_1 and L_2) but same sign, providing that their mean value has a sign opposite to the offset. In that case, the strong non-linearity does not occur, and it comes,

$$\Delta p \approx \frac{counter_1 - counter_2}{2N} \left(\frac{1}{\ln\left(\frac{3L_1-5}{L_1-5}\right)} - \frac{1}{\ln\left(\frac{3L_2-5}{L_2-5}\right)} \right)^{-1} \qquad (38)$$

and,

$$off \approx \frac{counter_1 \times \ln\left(\frac{3L_1-5}{L_1-5}\right) - counter_2 \times \ln\left(\frac{3L_2-5}{L_2-5}\right)}{N\left[\ln\left(\frac{3L_1-5}{L_1-5}\right) - \ln\left(\frac{3L_2-5}{L_2-5}\right)\right]} \qquad (39)$$

These results can be validated by simulation. Figure 8 represents the counter output as a function of the integrator leakage Δp in the case of a sequence of length $L=6$ [11111-1] and its opposite [-1-1-1-1-11] and for an input referred offset $off=0.0005$. For the negative sequence, the opposite of the counter is represented (trace a)). It can be seen that (32) perfectly models the modulator behavior, as the matching is very good between the simulations and the expected values. 500 simulations were realized varying Δp from 0 to 0.001.

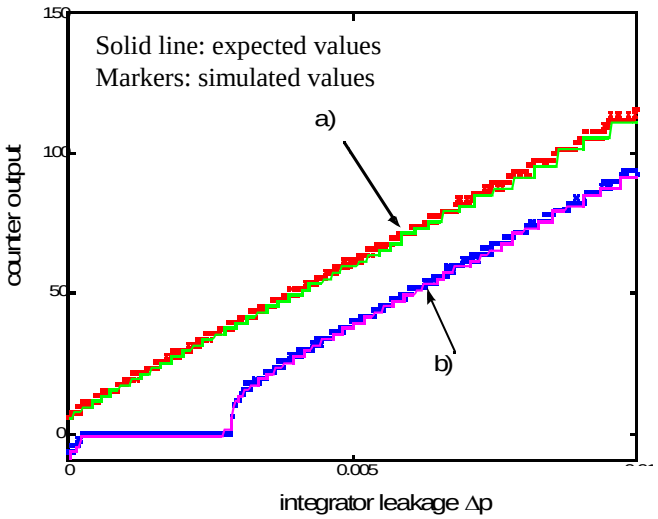

Figure 8: Counter output as a function of the integrator leakage, a) opposite of the counter for a negative sequence, b) counter for a positive sequence

Moreover, Figure 9 represents the integrator leakage estimates derived from (36) and (38), and Figure 10 shows the modulator offset estimates drawn from (37) and (39). 500 simulations were realized with four input sequences: $L_1=6$, $L_2=11$ and their opposites. The integrator leakage Δp vas varied from 0 to 0.01 in Figure 9 and the offset was set to 0.0005. For Figure 10, the offset was varied from 0 to 0.0005 and the integrator leakage set to Δp=0.0011.

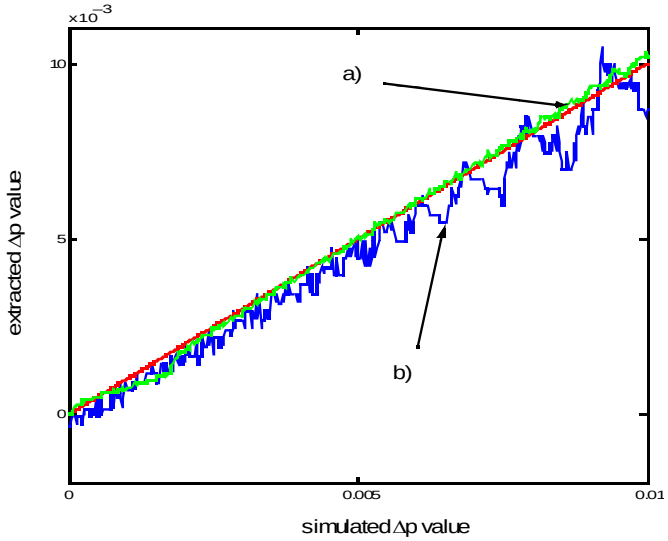

Figure 9: Integrator leakage estimate a) with equation (36) and $L=6$, b) with equation (38) and $L_1=6$ and $L_2=11$

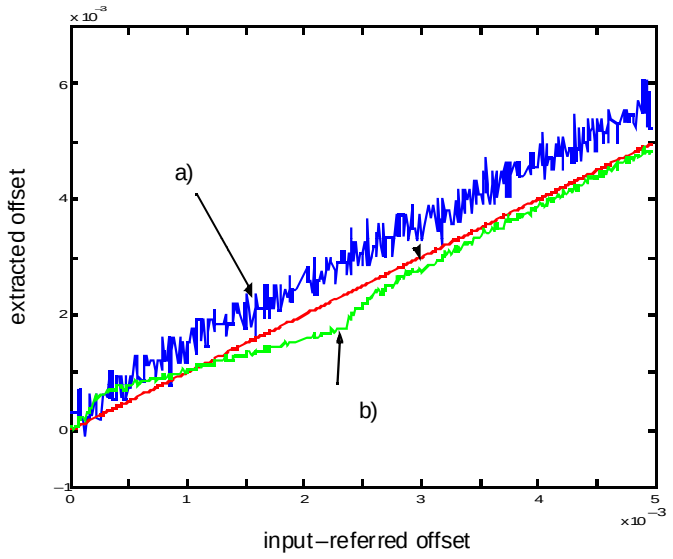

Figure 10: Modulator offset estimate with a) equation (37) b) equation (39)

III. INVOLVED HARDWARE

In the previous section the test procedure has been described for a second order modulator and a first order modulator, and simple expressions have been derived through the use of linear approximations. This section will detail the hardware necessary to carry out the test.

The digital sequence that is sent to the modulator has to be sampled by the modulator under test and its high and low levels should precisely match the modulator feedback DAC levels. A possible solution to alleviate these requirements would be to replicate the feedback DAC at the input of the converter. In case of a single-bit DAC, this would only consist in four switches (for a fully differential implementation). During test mode, this extra-DAC is enabled and the "normal" input is disabled. However, if a close look is taken at the modulator, it can be seen that there is no need to add any extra DAC. The feedback DAC can be configured to be used as the input DAC during the sampling phase and as the feedback DAC during the feedback phase. Only the clocking scheme of the modulator has to be altered and this only requires some additional logic gates. In the case of the second order modulator, the same thing can be done. Moreover, in order to test the second integrator leakage, the first loop is easily disabled and the input sequence is directly fed to the second integrator. Let us detail this on the implementation proposed in [14] that has been reproduced in Figure 11.

The modulator is driven by two non-overlapping clocks, P_1 and P_2, and the test modification requires the addition of two control signal T_1 and T_2 and the digital input sequence I. The test of the second integrator leakage also requires the addition of a a delay in the feedback loop. This can be easily implemented by enabling a memory element that buffers the output bit stream over one sample. This extra memory element is not shown in Figure 11. Let us note the buffered output Dz. Table 3 summarizes the original clocking scheme and the modifications necessary to perform the test.

Switch	Normal	Modified
A_1	P_1	$(P_1 \cdot \bar{T}_1) \cdot \bar{T}_2$
B_1	P_2	$(P_1 \cdot T_1 + P_2) \cdot \bar{T}_2$
C_1	P_1	P_1+T_2
D_1	P_2	P_2+T_2
A2	P_1	$P_1 \cdot \bar{T}_2$
B2	P_2	$P_2 + P_1 \cdot T_2$
C2	P_1	P_1
D2	P_2	P_2
R	D	$(D \cdot P_2 + I \cdot P_1) \cdot T_1 \cdot \bar{T}_2$ $+(Dz \cdot P_2 + I \cdot P_1) \cdot T_2 + D \cdot \bar{T}_1 \cdot \bar{T}_2$

Table 3: Clocking modification for a 2nd order modulator

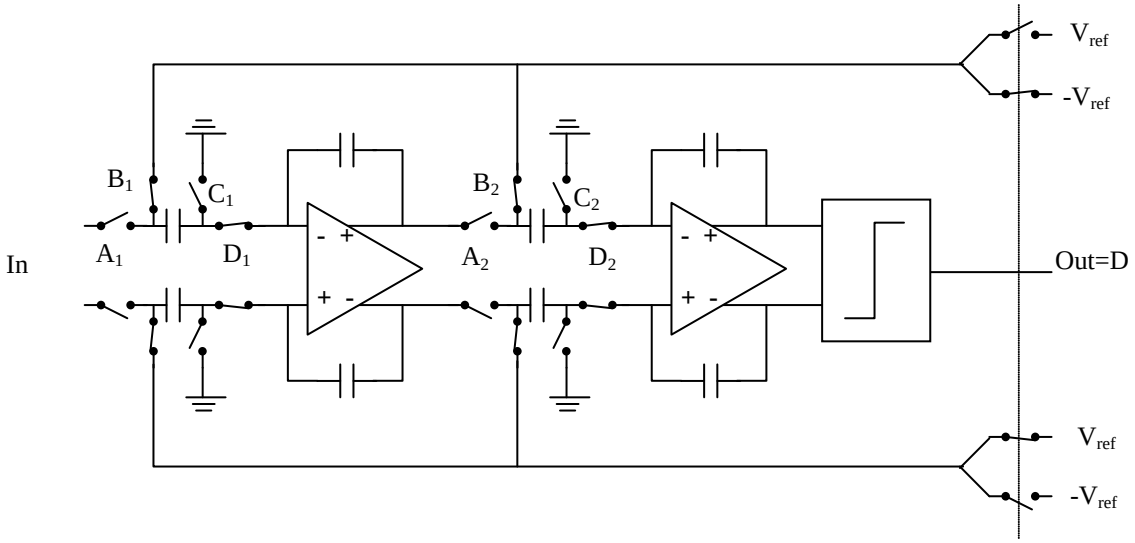

Figure 11: 2nd order modulator implementation

For $T_1=0$ and $T_2=0$, the modulator is in normal operation. For $T_1=1$ and $T_2=0$, the first integrator is tested. And for $T_2=1$ the second integrator is tested.

Another important point that should be taken into account is the stability. The first order modulator is known to be stable for any input within the limits of the full-scale. Moreover, the second order modulator has also been shown to be stable for any input that can be expressed as a DC level within full-scale plus a finite number of pure tones [17]. That is the case for the proposed test, as the periodic digital sequences can be decomposed in their Fourier series. However, global stability is not a sufficient condition for a successful implementation. Indeed, the integrator output has to remain bounded but to a manageable value. When using digital sequences as test input, the modulator is submitted to signal levels higher than under normal operation. Moreover, the addition of an extra delay in the feedback path for the single-bit first order modulator makes the integrator output vary between –4 and 4, which is the double of the normal requirements. Therefore, it could be necessary to use lower reference levels during test mode to avoid any interference with amplifier saturation or slew-rate limitations. Nevertheless, these levels do not have to be provided with precision as both the input and the output are defined with respect to them.

At this point, the modulator integrator leakage can be evaluated by a digital tester at very little cost, which is already a valuable DfT (Design for Testability) feature. But another step toward a full BIST implementation can easily be taken by generating the digital test sequence on-chip. As the procedure makes use of periodic sequences, they can be stored in registers that are read in a circular manner just as in [11]. However, in this work, the period of the sequences does not have to be high and will typically be lower than 16 memory elements. As it has been seen in the previous section, the opposite of the sequence may be required to get rid of the offset. This can be implemented easily without the need of storing it on-chip.

In the same way, the counting operation can be done in a very simple form, to avoid the need of acquiring the output bit stream at full-speed. The counting operation would have to sum the input sequence and subtract the output bit stream over a given number of samples. In the case of a multibit modulator, no obvious simplification is possible, but the words to be processed are of low precision. In the case of a single-bit modulator, however, the counting operation is greatly simplified. Indeed, as can be seen in Figure 12, some logic gates can be added such that the counter is incremented only when the input is 1 and the output is –1 and decremented only when the input is –1 and the output is 1.

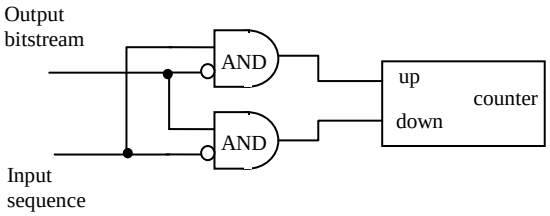

Figure 12: Counter implementation

The depth of the counter is determined as function of the desired precision. The finer the precision, the higher the number of acquired samples and the deeper the counter.

At the end of the evaluation period, the counter output can be read as a test result. Another possibility would be to make an on-chip comparison of the counter output with the value corresponding to the specified leakage. The test output would thus be of the type Go/No-Go. Conversely, it is also possible to directly calculate the parameters of interest, namely Δp and off, from the counter output, which would require some arithmetic operations to implement (7) and (8), (10) and (11), (36) and (37) or (38) and (39). Notice that these operations do not have to be implemented at full-speed.

IV. CASCADED MODULATOR EXAMPLE

In order to provide further validation of the proposed test strategy, the case of a third order 2-1 cascaded ΣΔ modulator will be considered as demonstrator. Figure 13 gives the scheme of the modulator.

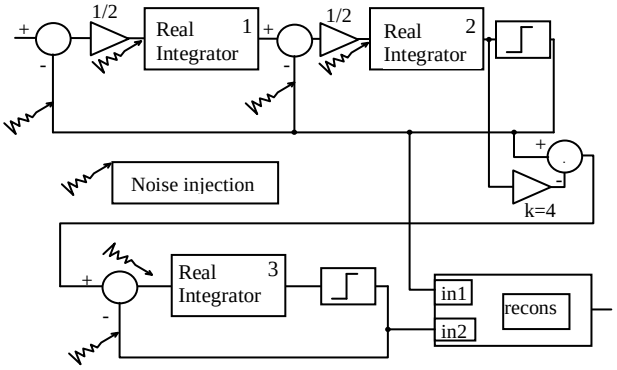

Figure 13: model of a cascaded 2-1 ΣΔ modulator

A 2nd order modulator is used as the first stage and its quantization error (noted E in Figure 2) is acquired and digitized by the second stage: a first order modulator. Using a proper reconstruction filter, the quantization error term in (1) can be cancelled and it is shown that the remaining quantization error is of order 3 [12]. If the integrators are leaky, the error cancellation is only partial and the modulator performance decreases. Nevertheless, in a cascaded ΣΔ modulator, it is possible to take into account the integrator leakage of all but the last stages and to digitally correct its

effect within the reconstruction filter. This possibility has also been inserted in the model used for simulation. The reconstruction filter in Figure 13 would be ideally,

$$recons = z^{-1} in_1 - (1 - z^{-1})^2 in_2 \quad (40)$$

And to take the leakage into account, it is modified as,

$$recons = z^{-1}\begin{bmatrix} 1 + (2 - p_{1c} - p_{2c})z^{-1} \\ +(1 + p_{2c}p_{1c} - 2p_{2c})z^{-2} \end{bmatrix} in_1 \quad (41)$$
$$-4(1 - p_{1c}z^{-1})(1 - p_{2c}z^{-1}) in_2$$

Where Δp_{1c} and Δp_{2c} are the evaluated integrator leakage for the first and second integrators.

The high-level Matlab model proposed in [18] is used to provide more realistic simulations. This model takes into account capacitor-related noise, amplifier noise, amplifier slew-rate, finite-bandwidth and saturation, amplifier offset and comparator offset and hysteresis. To validate the measurement scheme, a Monte Carlo simulation is performed. The ranges of variation for all the parameters are quoted in Table 4. Parameter T_s is the sampling time. The full-scale is set to 2.

Parameters	Range
Amplifier gains	[10;2000] (defines the leakage)
Slew-rates	[1.9;6]/Ts
Gain-Bandwidth	[1.9;6]/Ts
Saturation	[1.9;2.9]
Integrator gains	+/- 1%
Capacitor noise	$[0.65;6.5].10^{-6}$
Amplifier noise	$[0;1].10^{-6}$
Comparator hysteresis	[0;0.01]
Comparator offset	[0;0.04]
Integrator offsets	[0;0.002]
Quantization noise factor *k*	+/- 1%

Table 4: Variation range of the model parameters for a 2-1 ΣΔ modulator

A total of 215 simulations have been performed according to the following test flow:

- Initialization of the model parameters
- Simultaneous test of the 1st integrator and the 3rd integrator using the same periodic sequence of ten "1" and one "-1" for both, and its opposite. The count is realized over 6600 points for each sequence. The reference levels are lowered by a factor 2 for the test of the third integrator.
- Simultaneous test of the 2nd integrator and the 3rd integrator using the same periodic sequence of five "1" and one "-1" for both, and its opposite. The count is realized over 6600 points for each sequence.
- Estimates of the integrator leakages using (7) and (36)
- Simulation of the modulator for an input sine-wave of amplitude 0.5, and decimation of 256 by a 4th order Chebychev filter. The SNR is calculated using a DFT over 2048 points.
- Simulation of the same modulator, but with the amplifier gains set to 10^5. This gives the maximum achievable SNR with no integrator leakage.
- Simulation of the modulator, taking into account the measured leakages in the reconstruction filter. This gives the corrected SNR.

Table 5 summarizes the results obtained for the evaluation of the three integrator leakages. It presents the mean value and the standard deviation of the error between the evaluated value of the leakage and its exact value. It can be seen that a good precision is achieved despite the variation of other model parameters

Integrator	Error mean value	Error standard deviation
First L=11	$-1.2\ 10^{-4}$	$0.9\ 10^{-4}$
Second L=6	$1.4\ 10^{-4}$	$3.9\ 10^{-4}$
Third L=11	$-1.8\ 10^{-4}$	$2.3\ 10^{-4}$
Third L=6	$-0.5\ 10^{-4}$	$5.6\ 10^{-4}$

Table 5: Error between the simulated and evaluated parameters

It can thus be said that the proposed method is very robust and accurate. Even for a single-bit first order ΣΔ modulator, a good precision is achieved with only 13200 bit stream samples, which is a very small time as the output bit stream runs at the modulator sampling frequency. To make a comparison, the obtained precision is several orders of magnitude better than what was done in [8].

Figure 14 shows the histogram of the leakage-free modulators SNR. This SNR is what will be achieved at best for a perfect correction. It can be seen that integrator leakage is not the only parameter that affect the modulator precision. Other parameters such as amplifiers slew-rate can produce distortion. Figure 15 shows the histograms of the difference between the uncorrected SNR and the maximum achievable SNR (shown in Figure 14), and the difference between the corrected SNR and the maximum achievable SNR. The mean improvement for this set of simulations is 8.8dB and the maximum improvement is up to 29dB.

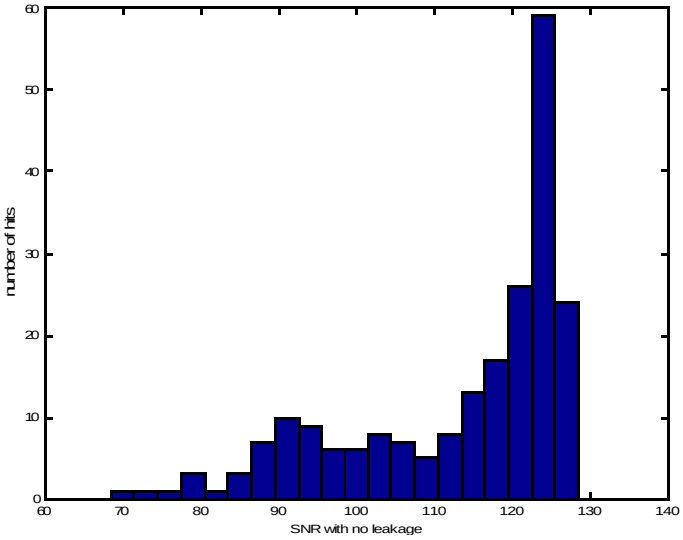

Figure 14: Histogram of the leakage-free modulators SNR

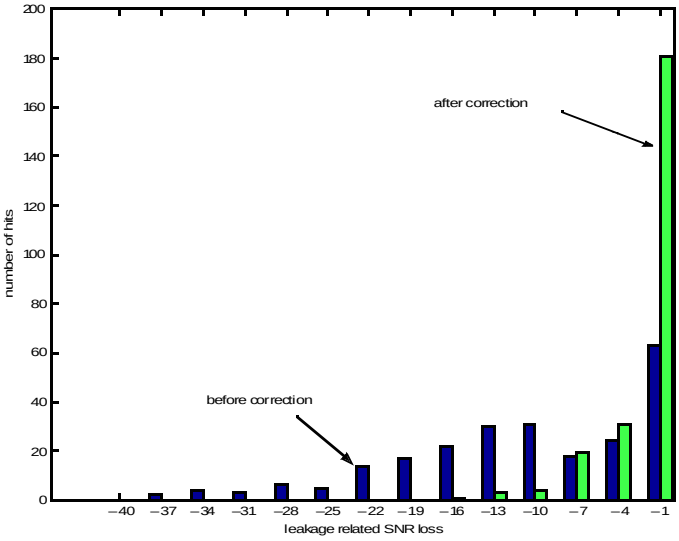

Figure 15: Histogram of the difference between the modulator SNR and the leakage-free modulator SNR, before and after correction.

V. Discussion

It has been shown across this paper that the proposed procedure to evaluate the integrator leakage in a ΣΔ modulator is efficient and robust. Theoretical basis have been provided and realistic simulations have been performed to support the technique. These simulations have shown that integrator leakages can be measured with great precision even in the presence of other strong non-idealities. Nevertheless, the modulator SNR does not depend exclusively on integrator leakage, as could be seen on Figure 14. This means that the estimation of the leakage cannot directly map onto the modulator performance as presented in [9], and hence it is not a functional test. Indeed, the digital test herein proposed is something hybrid between functional and structural and ideally, it would have to be complemented by a set of tests covering the full set of basic design specifications. We will focus further research effort on the evaluation of other parameters, like amplifier slew-rate or bandwidth, noise levels… but also on the generalization of the method to higher order modulators and on the impact of techniques such as dithering. While this is still to be done, the proposed procedure is nevertheless very appealing for screening test, diagnosis and drift monitoring, mostly because of its very reduced cost.

VI. Conclusions

In this paper, a simple and cost effective technique has been proposed to evaluate the integrator leakage in 1st and 2nd order ΣΔ modulators. The integrator leakage is known to degrade the performance of ΣΔ converters. And hence, the proposed test technique serves as an indirect test of this SNR degradation.

The theoretical basis and the feasibility of the technique have been proved through rigorous simulations using realistic models. As an additional result, it has been shown that the proposed technique can be used to correct the SNR loss due to leakage in cascaded modulators.

References

[1] IEEE standard 1241-2000

[2] O. Feely, L.O. Chua: "The effect of Integrator Leak in ΣΔ Modulation", IEEE Trans on Circuits and Systems, vol. 38, n°11, pp. 1293 -1305, November 1991

[3] V. Friedman: "The structure of the limit cycles in sigma delta modulation", IEEE Trans. on Communications, Vol. 36, no. 8, pp. 972 -979, August. 1988

[4] D.B. Ribner: "A comparison of modulator networks for high-order oversampled ?? analog-to-digital converters" IEEE Trans. Circuits and Systems, n° 40 (2) , 1991, pp. 145 -159

[5] F. Medeiro, B. Pérez-Verdú, A. Rodríguez-Vázquez: *Top-Down design of high performance sigma-delta modulators*, Kluwer Academic Publishers, 1999

[6] H.C. Hong, J.L. Huang, K.T. Cheng, C.W. Wu: "On-chip Analog Response Extraction with 1-Bit ΣΔ Modulators", Proc. of the Asian Test Symp, pp. 49-54, 2002

[7] D. Vazquez, G. Huertas, G. Leger, A. Rueda, J.L. Huertas: "On-Chip Evaluation of Oscillation Based Test Output Signals for Switched-Capacitor Circuits", Int. Journ of Analog Integrated Circuits and Signal Processing, vol. 33, pp.201-211, 2002

[8] L.L. Huang, K.T. Cheng: "Testing and Characterization of the One-Bit First-Order Delta-Sigma Modulator for On-Chip Analog Signal Analysis", Proc. of the International Test Conf., pp.1021-1030, 2000

[9] C.K. Ong, K.T. Cheng: "Testing second-order delta- sigma modulators using pseudo-random patterns" Microelectronic Journal, n° 33, pp. 807-814, 2002

[10] C.K. Ong, K.T. Cheng: "Self-Testing Second-Order Delta-Sigma Modulators Using Digital Stimulus." Proc. of VLSI Test Symp., pp. 123 -128, 2002.

[11] B. Dufort, G.W. Roberts: "On-chip analog signal generation for mixed-signal built-in self-test" IEEE Journ. Solid-State Circuits, n° 34 (3) , 1999, pp.318 -330

[12] S.R. Norsworthy, R. Schreier, G. Temes: Delta-Sigma Data Converters: Theory, Design, and Simulation, IEEE Press, 1997

[13] S.H. Ardalan, J.J. Paulos: "An Analysis of Nonlinear Behavior in Delta-Sigma Modulators", IEEE Trans. Circuits and Systems, 1987, n° 34, (6), pp. 593-603

[14] B.E. Boser, B.A. Wooley: “The Design of Sigma-Delta Modulation Analog-to-Digital Converters”, IEEE J. Solid-State Circuits, 1998, nº 23, (6), pp. 1298-1308

[15] G. Leger, A. Rueda: ”Simple BIST for integrator leak in second-order double-loop sigma-delta modulators”, Proc. of the Int. Mixed-Signal Test Workshop, pp. 53-57, 2003

[16] R. Schreier, W.M. Snelgrove: “ΣΔ Modulation is a Mapping” Proc. of the ISCAS 1991. pp. 2415-18, June 1991.

[17] S.C. Pinault, P.V Lopresti: “On the Behavior of the Double-Loop Sigma-Delta Modulator” IEEE Trans. Circuits and Systems II, 1993, nº 40, (8), pp. 467-479

[18] P. Malcovati *et al.*: “Behavioral Modeling of Switched-Capacitor Sigma-Delta Modulators” IEEE Trans. Circuits and Systems I, 2003, nº 50 (3), pp. 352-364