On-Chip Evaluation of Oscillation-Based-Test Output Signals for Switched-Capacitor Circuits

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ABSTRACT

This work presents a simple and low-cost method for on-chip evaluation of test signals coming from the application of the Oscillation-Based-Test (OBT) technique. This method extracts the main test signal features (amplitude, frequency and DC level) in the digital domain requiring just a very simple and robust circuitry. Experimental results obtained from an integrated chip demonstrate the feasibility of the approach.

1.INTRODUCTION

Testing embedded building blocks is much more difficult than testing their stand-alone counterparts, and usually this cannot be done by replicating conventional test techniques. In mixed-signal ICs, the most affected components are the analog cores, since analog testing is based on checking functional specifications, which can be conflictive when the test time has to be kept short, the number of available pins is reduced (as it normally happens in SOCs) and full access to input/ output core terminals cannot be granted. Furthermore, functional test techniques greatly differ depending on the involved analog components, making it almost impossible to define a general (functional) test methodology applicable to any analog block. Additionaly, mixed-signal testers need to cope with demanding requirements of speed, accuracy and memory storage, which means a high cost. As a consequence, analog cores play a crucial role in the feasibility of a complex system, and their market appeal depends on the development of test strategies that can be used in very different application environments.

During the last years, the test community has centered its attention on the structural test solution called Oscillation-Based-Test (OBT) [1-8]. Several reasons can be outlined:

a) The Built-In Self-Test (BIST) implementation of the OBT (Oscillation BIST or OBIST) avoids the need of extra resources dedicated to the test stimuli generation.

b) It can be applied to many kinds of circuits with a wide variety of different specifications (filters, A/D, etc.).

c) The test parameters are reduced to the oscillation parameters independently of the type of the Circuit Under Test (CUT). In this sense, it provides a way to the standardization of the testing approaches.

d) Complex analog or mixed-signal circuits can be split into simpler blocks where OBT can be applied separately.

Although the OBT is mainly a fault-driven approach, it can be shown that the oscillation parameters are closely related to the behaviour and performance of the circuit under normal operation [3, 6], making possible to extract functional specifications from them [4]. Nevertheless, it has been demonstrated elsewhere [6] that the oscillation frequency may not be enough to achieve a reasonable fault coverage. In general, it can be improved drastically when taking into account the oscillation amplitude. Although undoubtedly the amplitude measurement will require additional dedicated efforts, the accuracy needed in the measurements can be relaxed if both parameters are considered [6]. Moreover, the test quality can also be improved using additional oscillation parameters such as the distortion of the generated waves, their DC level, etc.

Thus, one of the crucial issues to be considered is concerned on how to give support to the evaluation of the test signals, that is, to the measurement of the oscillation parameters. In this sense, it would be preferable to encode the information into a single digital signal. To solve this problem, Roh and Abraham recently proposed the use of a Time-division Multiplexing comparator [8] which provides a digital signature related to the frequency and amplitude characteristics of the test signal. A solution based on oversampling modulators has been proposed by the present and other authors in [4,7]. In these works, the OBT output signal is digitally coded by a SD modulator, and can be processed either internally using a digital algorithm or externally by a pure digital tester. The work

in [7] discusses the problem of internal node access and provides possible procedures for on-chip decision mechanisms.

The present paper proposes a more elaborated and practical solution. Its aim is to discuss a practical and low-cost mechanism for the on-chip evaluation of the OBT signals and the test interpretation. The provided solution is based on the use of a first order sigma-delta (ΣΔ) modulator for analog to digital code conversion of the test output signals. Exploring both the properties of the test signals and the behavior of the first order SD modulator allows to extract the amplitude, frequency and DC level of the oscillation waveforms using simple and low-cost pulse digital counters. In addition, a low-cost digital decision mechanism can easily be implemented on-chip.

For the sake of simplicity, we will restrict our discussions along the paper to the discrete-time domain. However, it can be formally extended to the continuous case. The paper is organized as follows. Section 2 briefly reviews the use of a ΣΔ modulator for the Analog to Digital conversion of the test signals. Sections 3 details the principles of a novel, low cost and robust approach for a digital evaluation and interpretation of the test signal and, in Section 4, the basic algorithm is modified in order to improve the measurement accuracy. The extraction of the main oscillation parameters, like the frequency, amplitude and DC-level are addressed. Experimental results from an integrated prototype and its application to an industrial demonstrator like a Dual Tone Multifrequency Detector (DTMF) are shown in Section 5. And finally, Section 6 presents some conclusions.

2. USING A Σ–Δ MODULATOR FOR ANALOG TO DIGITAL CONVERSION

Figure 1 shows the basic use of a ΣΔ modulator for general evaluation purposes. The test signal *x(n)* coming from the Circuit Under Test (CUT) is fed to a ΣΔ modulator to obtain a train of modulated pulses *d(n)* containing all the information of *x(n)*. Thus, the output *d(n)* can be seen as a digital encoding of the test output signal *x(n)*. Depending on the modulator characteristics in terms of factors like the oversampling ratio, order, quantizer levels, etc. this digital encoding has a higher or lower accuracy. Normally, practical modulators must be preceded by an antialiasing filter to ensure that band-limited signals are processed. However, it is not necessary when *x(n)* is close to a pure tone. To extract the oscillation parameters, *d(n)* can be processed either externally using a pure digital tester or internally using a Digital Signal Processor (DSP). But the last procedure usually

requires complex processors that may be very important in terms of area and power and even intolerable for many applications.

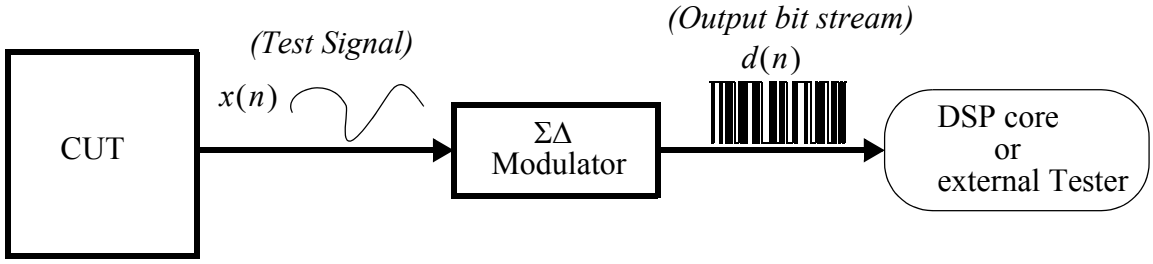

Figure 1:*Basic use of a* ΣΔ *modulator for the evaluation of a test signal.*

3.A LOW-COST A/D CODE CONVERSION AND EVALUATION UNIT

Figure 2-a illustrates the proposed approach for a simple on-chip evaluation of the test signals coming from the application of the OBT technique. For convenience, it has been considered that the CUT is a filter (or a part of it) represented by its transfer function H(z). The oscillator has been built following the guidelines given in [6], where a comparator followed by a 1-bit Digital to Analog converter is used as a feedback loop during the test mode to obtain an oscillator where the amplitude is controlled by limitation. The block named *Evaluation unit* is composed by a ΣΔ modulator and a set of digital counters (*count-freq, count-amp and count-DC*). The ΣΔ modulator is used to obtain a digital encoding *d(n),* of the oscillation signal*, x(n).* The counters extract the oscillation parameters by processing the train of the modulated pulses *d(n)* together with the signal *q(n)*, coming from the non-linear feedback loop, which indicates the sign of the oscillation signal. Finally, a digital *decision mechanism* will provide the final result of the test evaluation.

The different waveforms are depicted in Figure 2-b. The test signal, x(n), is characterized by its frequency, amplitude, DC level, distortion, etc. that are directly related to the operation of the filter [5,6].

The clock that rules the operation of the oscillator and the modulator is assumed to be the same. It is convenient to remark that the use of the comparator that provides the signal *q(n)* is not mandatory in the implementation of the oscillation mode. However, it would be necessary to include it as an additional block in the evaluation unit.

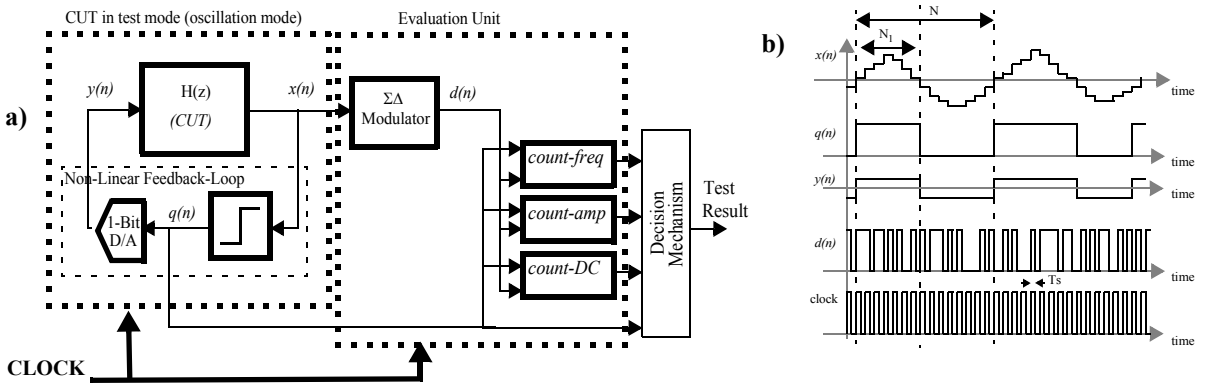

Figure 2: *Illustration of the proposed on-chip evaluation solution. a) Block diagram. b) Waveforms.*

To explain how the proposed approach works, we will consider the first order modulator depicted in Figure 3. The response *d(n)* can be expressed, [9] as a function of the input *x(n)* and the quantization error as,

$$d(n) = x(n-1) + e(n) - e(n-1) \tag{1}$$

The modulator model described by Eq (1) considers that the signal *x(n)* is normalized to the modulator Full-Scale (FS). As can be deduced, the output of the modulator contains all the information about the test signal, *x(n)*. Thus, all the test parameters of the oscillation waveform can be ideally extracted from it.

Now, let us make some considerations about the oscillation wave *x(n)*:

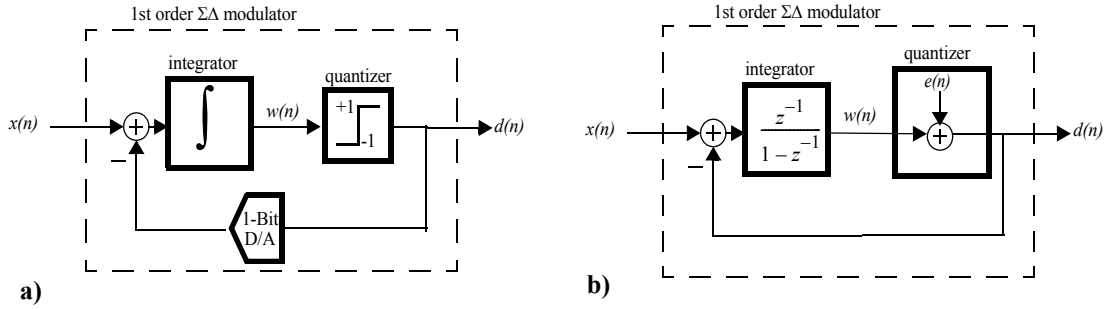

Figure 3:*1st order ΣΔ modulator. a) Block diagram. b) Used model*

1.- *x(n)* is a periodic signal of frequency $w_{osc} = 2\pi\frac{f_{osc}}{f_s} = \frac{2\pi T_s}{T_{osc}}$, where T_s is the sampling period and T_{osc} the oscillation period. Thus it can be described by its Fourier series expansion as,

$$x(n) = B + A\sin(w_{osc}n + \Phi) + \sum_{k>1} A_k \sin(kw_{osc}n + \Phi_k) \quad (2)$$

where *B* represents its DC level, A_k the amplitude of the k-th harmonic and Φ_k its corresponding phase shift.

2.- From Figure 2, it is clear that the input signal of the filter $y(n)$ is a square-shaped wave, so it contains no harmonics of even order (or at least their contribution is very small). As the filter behaves as a linear system, even harmonics in Eq (2) can be neglected. So,

$$x(n) = B + A\sin(w_{osc}n + \Phi) + \sum_{k(odd)>1} A_k \sin(kw_{osc}n + \Phi_k) \quad (3)$$

3.- Moreover, following the guidelines to build the oscillator given in [6], a Low-Pass or Band-Pass filter is involved, and a low distorted signal ($A_k \ll A$) results at the output of the filter. Let us then consider that *x(n)* can be approached by,

$$x(n) \approx B + A\sin(w_{osc}n + \Phi) \quad (4)$$

The last part of this section describes the set of operations implemented by the counters in order to extract a digitally encoded measure of the main oscillation parameters (frequency, amplitude and DC-level).

count-freq

The oscillation frequency can be extracted by counting the number of clock periods that lie between two positive (or negative) edges of *q(n)* (see Figure 2). Thus, the block named *count-freq* is no more than a simple counter. The accuracy will be determined by the oversampling ratio (*Tosc/ Ts*) and will depend on the uncertainty in the determination of the zero-crossings (given by q(n)). This error will always be less than one clock period. Hence, the state of the counter at the end of each period of *q(n)* will be a number ($N \in \aleph$) whose value can be formally expressed as,

$$\left\lceil \frac{T_{osc}}{T_s} - 1 \right\rceil \leq count\text{–}freq = N \leq \left\lfloor \frac{T_{osc}}{T_s} + 1 \right\rfloor \quad (5)$$

For example, for an oversampling ratio as low as 33, the accuracy of the frequency measurement is of 3% approximately. This precision is larger than the needed, for instance, in the case of the DTMF industrial demonstrator presented by the authors in [5,6], where the required accuracy in the oscillation parameter measurements was around 10% to achieve a 100% fault coverage.

count-amp

The operation performed by the block named *count-amp* is based on the fact that the area under a rectified sinusoid over a whole period (*T*) is proportional to the amplitude, and more concretely,

$$\int_{0}^{T/2} [B + A\sin(\omega t)dt] - \int_{T/2}^{T} [B + A\sin(\omega t)dt] = \frac{2A}{\pi}T \ . \tag{6}$$

This idea can be extended to our case if the sign of *x(n)*, which is provided by *q(n)*, is used to synchronize the beginning of the computation with the zero-crossing points of the test signal. The discrete-time counterpart would be the sum of positive values of *x(n)* (i.e. over *q(n)=1*) minus the sum of negative values of *x(n)* (i.e. over *q(n)=0*). However, Eq (1) suggests to perform the indicated operation using the output of the modulator *d(n)*.

Let N_1 be the number of clock periods where *x(n)* is positive and *N* the total number of clock periods between two positive edges of *q(n)*. The parameter named *count-amp* is defined as,

$$count-amp = \sum_{n=0}^{N_1-1} d(n+1) - \sum_{n=N_1}^{N-1} d(n+1) \tag{7}$$

which can also be written,

$$count-amp = [n_1 - n_0]_{q(n)=1} - [n_1 - n_0]_{q(n)=0} \tag{8}$$

where n_1 and n_0 denote the number of ones (high levels) and zeros (low levels) at d(n) respectively. Notice then that the implementation of this block only requires some simple counters and basic arithmetic functions.

Using Eq (1) and Eq (7), it can be shown that,

$$count-amp = \left\{ \sum_{n=0}^{N_1-1} x(n) - \sum_{n=N_1}^{N-1} x(n) \right\} + \{-e(N) + 2e(N_1) - e(0)\} \quad (9)$$

which leads, assuming that there is no overrange in the modulator ($e(n) \in [-1, 1]$), to,

$$count-amp = \left\{ \sum_{n=0}^{N_1-1} x(n) - \sum_{n=N_1}^{N-1} x(n) \right\} \pm 4 \quad (10)$$

It means that the sum of the modulator output as described in Eq (7) or Eq (8) gives the same result as the sum over *x(n)* plus a term representing the quantization error, that is limited to ± 4.

Using the expression of *x(n)* given by Eq (4), and assuming that the DC level (*B*) is small (as is usually the case under fault-free conditions) and $T_{osc}/T_s \gg 1$, it can be shown that,

$$count-amp \approx \frac{2A}{\pi} N \pm 4 \quad (11)$$

where, as was said above, A has to be normalized to the modulator Full-Scale.The operation indicated in Eq (7) can be interpreted as a measure of the test signal amplitude . Notice that although the result also depends on N (frequency), this parameter is extracted separately by *count-freq*, avoiding fault masking.

The relative error in the measurement for a normalized amplitude of *A=1* is given by $4\pi/2N = 2\pi/N$. Obviously, the larger the oversampling ratio ($T_s/T_{osc} \approx 1/N$) is, the smaller this value will be. For example, referring again to the work in [6], the accuracy in the amplitude measurement required to have a very high fault coverage was around 10%. This accuracy could be achieved with an oversampling ratio of around 60.

In fact, there are other sources of errors, apart from the quantization one, contemplated in Eq (11). These are due to the discrete nature of *x(n)*, to the presence of harmonics (distortion) and to the DC level shift (the zero-crossing instants, given by *q(n)* are taken as time references and depend on the DC-level). Nevertheless, if the oversampling ratio is high, the DC level is kept small and the input signal *x(n)* exhibits low distortion, it can be shown that these errors are negligible with

respect to the "quantization" error.

A more general interpretation of the information provided by this block can be deduced from Eq (9). It computes the area under the discretized signal *x(n),* being this area the actual extracted parameter that can be directly used as a test parameter. In the particular case of low distorted sinewaves it can be demonstrated that only the fundamental harmonic amplitude has a significant contribution to this area as shown in Eq (11).

count-DC

The operation performed by this block is based on the assumption of that the area under a periodic signal over a whole period defines its DC-level.

Translating it to the discrete-time domain, the operation of block named *count-DC* is defined as,

$$count-DC = \sum_{n=1}^{N} d(n) \tag{12}$$

where the sum is performed over the N samples between two succeeding positive (or negative) edges of *q(n)*. Notice that it is equivalent, from a digital point of view, to perform the difference between the number of 1's (n_1) and the number of 0's (n_0) at the modulator output during the corresponding period of the signal. That is,

$$count-DC = (n_1 - n_0)_{period} \tag{13}$$

Again only simple digital counters are needed for its implementation.

Using Eq (1) and Eq (12), it can be written,

$$count-DC = \sum_{n=0}^{N-1} x(n) + \{e(N)-e(0)\} \tag{14}$$

Assuming that there is no overrange in the modulator ($e(n) \in [-1, 1]$), it leads to,

$$count-DC = \sum_{n=0}^{N-1} x(n) \pm 2 \tag{15}$$

For *x(n)* given by Eq (4), and $T_{osc}/T_s \gg 1$, it can be shown that,

$$count - DC \approx NB \pm 2 \tag{16}$$

Because N is a known value through count-freq, the result given by Eq (16) can be interpreted as a measure of the DC-level (B) of the test signal.

The total error is dominated by the ± 2 quantization term. The relative accuracy is thus limited to $\pm 2/N$.

Eq (5), Eq (8) and Eq (13) show that the counter states at the end of an evaluation period are directly related to the parameters of interest (the amplitude, the DC level and the frequency). Thus the test decision mechanism can be straightforwardly deduced: it should be no more than a digital block performing a comparison between the expected fault-free counter states (stored on-chip) and the actual counter states.

4.PRECISION ENHANCEMENT

The precision of the measurements is mainly driven by the quantization error and the oversampling ratio (T_{osc}/T_s). Indeed, the higher the oversampling ratio, the smaller the weight of the quantization error in the final state of the counters. But unfortunately, there may be applications where the accuracy obtained for a specified sampling frequency is not sufficient. In such cases it is necessary to increase the precision through another strategy.

For example, the precision of the frequency measurement can be increased if the count is performed over a number $m>1$ of periods. In this case, the counter state N' at the end of the m-periods will be,

$$\left\lceil m\frac{T_{osc}}{T_s} - 1 \right\rceil \leq count - freq \; = \; N'(\; \approx mN) \leq \left\lfloor m\frac{T_{osc}}{T_s} + 1 \right\rfloor \tag{17}$$

So, the relative accuracy is increased in the same factor m. The price to be paid is, obviously, the need of additional memory elements in the counter, as well as an increased test time.

In the same way, the precision of the DC-level measurement can also be increased by extending the number of periods for the counting process. Going back to Eq (14), the error depends only on the quantization error at the beginning and at the end of the counting process. So, if it is extended to $m>1$ periods, the weight of the quantization error will be divided by the same factor. That is,

$$count-DC = \sum_{n=0}^{N'-1} x(n) + \{e(N')-e(0)\} \approx N'B \pm 2 \quad (18)$$

where $N' \approx mN$ and thus, the relative error will be now of $2/(mN)$ as explained.

On the other hand, the above strategy is not valid to increase the precision in the case of the amplitude measurement. Looking at Eq (9), it can be seen that the quantization error corresponding to the zero-crossings contributes with a weight of 2. Then, if the count is extended to m periods ($m>1$) , the number of zero-crossings would be increased in the same factor, and consequently, the total weight of the quantization error would remain unaltered ($\pm 4m$).

The following algorithm allows to increase the precision by a factor of two not only in the case of the amplitude measurement but also in the case of the DC-level measurement.

Let *count-amp'* be the result of the counter when the beginning of the counting process is advanced one clock period, that is,

$$count-amp' = \sum_{n=-1}^{N_1-2} d(n+1) - \sum_{n=N_1-1}^{N-2} d(n+1) \quad (19)$$

Assuming $T_{osc}/T_s \gg 1$ and a low distorted signal *x(n),* Eq (19) would give the same accuracy as Eq (7). However, the term corresponding to the quantization error contribution is different. Concretely, it is given by,

$$\pm 4 \Leftrightarrow -e(N) + 2e(N_1) - e(0) \quad (20)$$

in *count-amp*, and

$$\pm 4 \Leftrightarrow -e(N-1) + 2e(N_1-1) - e(-1) \quad (21)$$

in *count-amp'*. On one hand, from Eq (1),

$$e(N-1) = x(N-1) + e(N) - d(N) \quad (22)$$

But if the signal has low distortion and $T_{osc}/T_s \gg 1$, *x(N-1)* will be very close to zero, and then,

$$e(N-1) + e(N) \approx 2e(N) - d(N) \quad (23)$$

On the other hand, by definition,

$$e(N) = d(N) - w(N) \tag{24}$$

where *w(n)* is the output of the integrator within the modulator (see Figure 3). Then, Eq (23) can be re-written as,

$$e(N-1) + e(N) \approx d(N) - 2w(N) \tag{25}$$

If there is no overrange in the modulator, then

$$-1 < w(N) < 1 \tag{26}$$

Moreover, the digital output is obtained comparing the integrator output with zero. Thus, if *w(N)>0*, it means that *d(N)=1*. It comes,

$$-1 < d(N) - 2w(N) < 1 \tag{27}$$

In the same way, if *w(N)<0*, then *d(N)=-1,* and Eq (27) is still verified. Therefore, using Eq (25), it can be concluded that,

$$|e(N-1) + e(N)| < 1 \tag{28}$$

for all zero-crossing index N.

It means that, around the zero-crossing instants, the sum of two consecutive quantization errors remains, approximately, in the range [-1,1]. Consequently, the mean value of the two count versions (*count-amp* and *count-amp'*) gives,

$$\left(\frac{count-amp + count-amp'}{2}\right) \approx \frac{2A}{\pi}N \pm 2 \tag{29}$$

and thus, the relative precision for the amplitude is improved by a factor of 2 ($\pm 4 \rightarrow \pm 2$).

The same considerations can be made for the DC-level case. In the same way, it can be improved by a factor of 2 as follows,

$$\left(\frac{count-DC + count-DC'}{2}\right) \approx BN \pm 1 \tag{30}$$

From a hardware point of view, the computation of the second version of the count (*count-amp'*) only requires to add (or subtract) the bit preceeding each zero-crossing to the first count version (*count-amp*). Indeed, re-writing Eq (19) using Eq (7)

$$count-amp' = count-amp + d(0) - 2d(N_1) + d(N) \tag{31}$$

Provided that *d(n)* is *+1* or *-1*, it appears that the sum of the two counts will always be even. Thus,

there would be no truncation error in the division by two when taking the mean value.

5.Example of Application to a Dual Tone Multifrequency Detector

We have taken advantage of the chip shown in Figure 4 (integrated in a 0.6μm double-poly double-metal technology) to validate the proposed strategy, because it contains the essential elements of the scheme in Figure 2. More concretely, a Switched-Capacitor programable biquad that can be reconfigured as an oscillator throught the OBT methology reported in [6] and a first-order ΣΔ modulator. The programable biquad reproduces some of the DTMF detector filter sections reported in [6].

Provided that the digital part of the proposed scheme (Figure 2) was not available in the chip, the test setup of Figure 5 has been implemented, where this digital part has been emulated by a workstation. Anyway, a practical on-chip implementation would only require few digital elements, as suggested by the simplicity of the evaluation algorithm. In the case of the DTMF reported in [6], all the blocks required for this evaluation solution, not only the analog part but also the digital part, could be implemented reusing the available on-chip circuitry and, that way, the extra area overhead would be negligible.

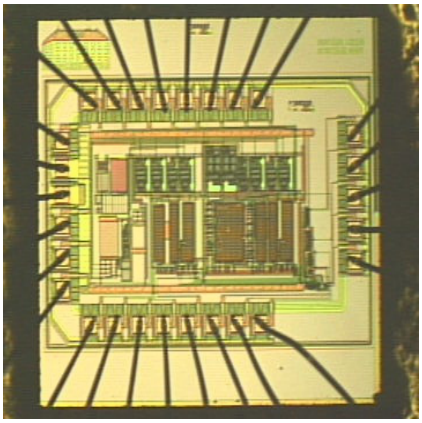

Figure 4:*Integrated chip.*

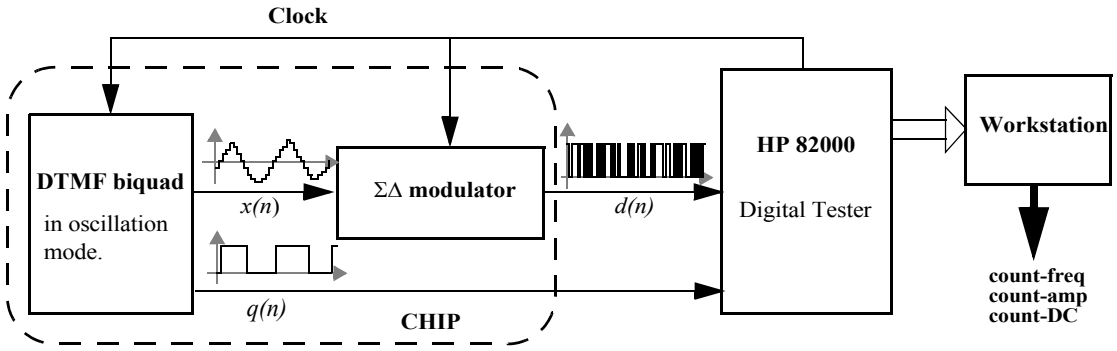

Figure 5:*Test setup for the validation of the proposed approach.*

x(n) parameter	Nominal value
Frequency	598Hz
Amplitude	459 mVp
3rd harmonic	-30 dB
5th harmonic	-40 dB
DC level	must be small

Table I: Nominal characteristics of the expected fault-free oscillation wave.

For one of the biquad configurations, the predicted nominal parameters of the OBT output signal (*x(n)* in Figure 5) were estimated by simulation and they are shown in Table I. The DC level is must be small but its exact value cannot be predicted quantitativaly. The full scale range of the modulator, to which the amplitude has to be normalized, has been set to FS=1.12V_{pp}, and the clock frequency to $1/T_s$= 55.934KHz. These conditions, together with Table I, lead to the expected count values given in Table II. Notice that the uncertainty of the counter states (due to the quantization

	Basic Algorithm	**Improved Algorithm**
count-freq	93,53 → [93, 94]	
count-amp	48,8 ± 4 ∈ [45, 52]	48,8 ± 2 ∈ [47, 50]
count-DC	SN±2	SN±1

Table II: Predicted counters values for both algorithms (SN: Small Number)

error) is taken into account to define the expected window for each counter.

As was said above, there is no tight control over the fault-free DC-level in this implementation (see Table II). Anyway, for a given sample, the dispersion of the obtained count-DC values should remain between the predicted limits ± 2 or ± 1 .

In the test set-up (Figure 5), the biquad is forced to oscillate and the resulting sine wave *x(n)* feeds the sigma-delta modulator. The output bit-stream, *d(n),* and the square-wave, *q(n)*, are then acquired by the digital tester and processed by a workstation. Figure 6 shows the experimental response, *d(n)* of the modulator to the experimental test signal, *x(n)*.

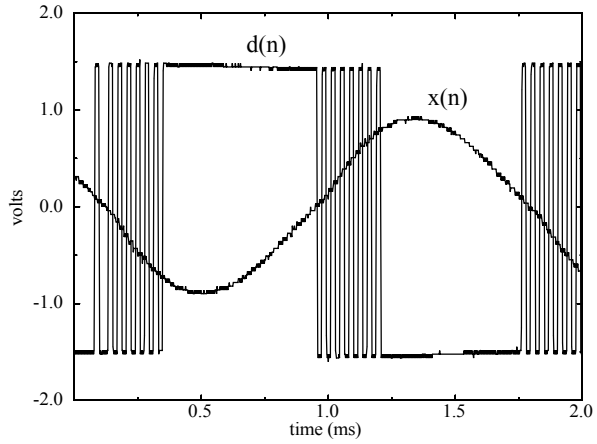

Figure 6:*Modulator input x(n) and output d(n).*

Five samples have been tested. For each one, 60 evaluation periods have been acquired by the digital tester. Thus, after the workstation processing, a set of 60 values of *count-amp, count-freq, count-DC* has been obtained for each sample. Notice that these 60 values of *count-amp* (respectively count-freq and count-DC) must be distributed within the window given in Table II.

The results for *count-freq* are displayed as 5 histograms in Figure 7, where it can be seen the perfect agreement with the expected results of Table II. Moreover, the mean value of the counters varies from 93.80 to 94, which also agrees very well with the nominal one (93.53).

The results for *count-amp* are shown in Figure 8 for both the basic algorithm and the improved one. Although both histograms are centered around 49 for all the samples as predicted, the

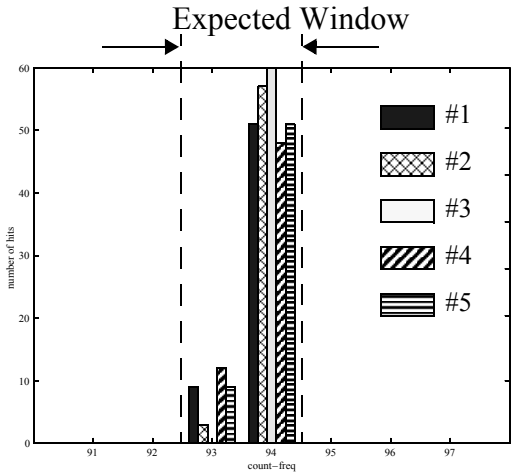

Figure 7:*Histograms for count-freq (5 samples).*

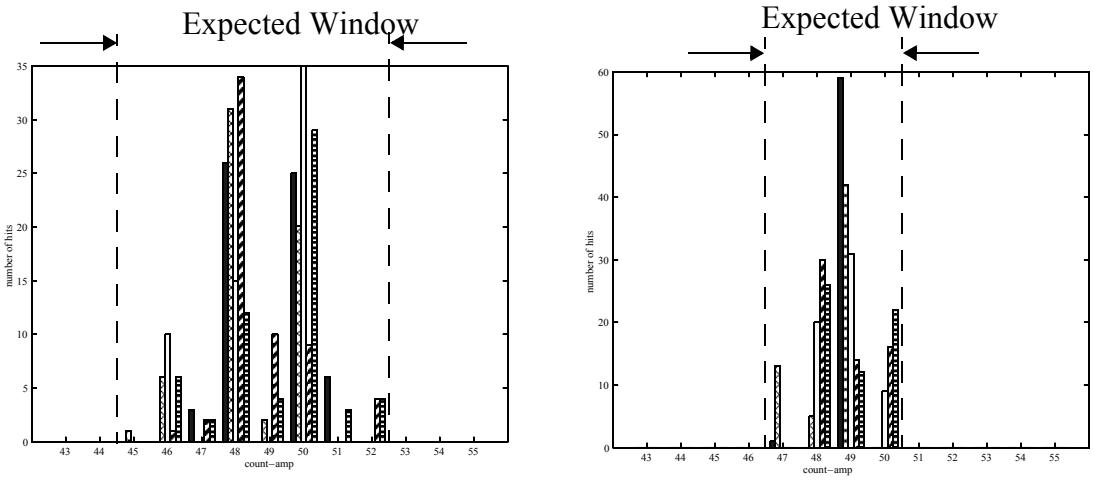

Figure 8:*Histograms for count-amp (5 samples). a) Basic algorithm. b) Improved one.*

improvements in Figure 8-b are clear because the dispersion of the values is only ± 2.

Finally, the results for *count-DC* are shown in Figure 9. As predicted, the results agree with a low DC-level of the signals. Here it is important to notice that each sample has its own central value due to the fact that there is no explicit control over the DC level, as explained before. However, each sample exhibits the expected window width. Again, the improved algorithm (Figure 9-b) is shown to be more precise because the dispersion for all samples is no more than ± 1

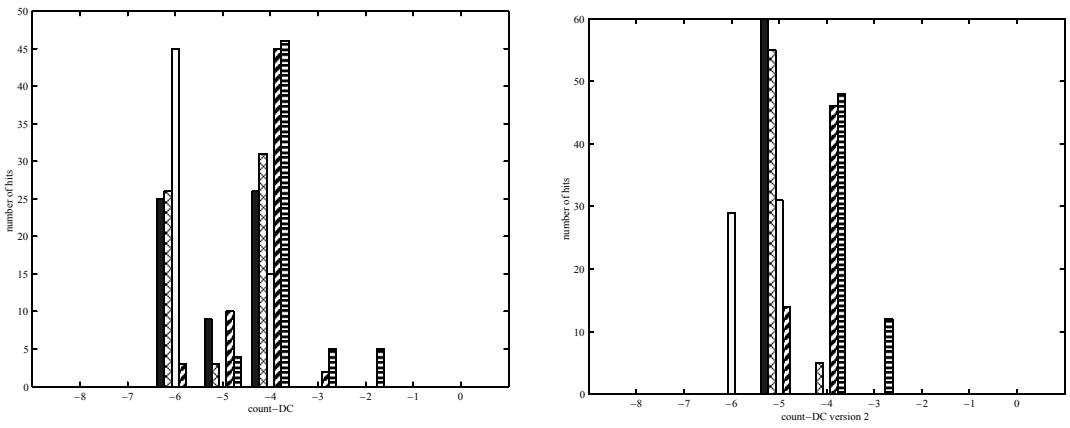

Figure 9:*Histograms for count-DC (5 samples). a) Basic algorithm. b) Improved one.*

6.CONCLUSIONS

This work presents a simple and low-cost method for on-chip evaluation of test signals coming from the application of the OBT technique. It extracts the amplitude, frequency and DC level of the test signal, with an accuracy that is mainly determined by the oversampling ratio, allowing to take a decision about the result of the test. The required circuitry consists of a first order sigma-delta modulator for A/D conversion, a comparator to provide the signal sign, and a set of simple digital counters. The simplicity and robustness of such type of circuitry, together with the experimental results, make the present approach very suitable for on-chip evaluation of signals coming not only from the application of the OBT, but also for any other application where it is necessary to perform this kind of measurements.

7.REFERENCES

[1] K. Arabi and B. Kaminska.“Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits". VLSI Test Symposium, 1996, pp. 476-482.

[2] K.Arabi,B.Kaminska."Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method". Trans. on Comp.-Aided Design of Int. Circ. and Sys. , vol.16, no. 7, July 1997.

[3] K.Arabi,B.Kaminska.“Oscillation- Test Methodology for Low-Cost Testing of Active Analog Filters" *Trans. on Instrum. and Meas.,* vol. 48, no. 4, pp. 798-806, Aug. 1999.

[4] Hassan IHS, K. Arabi,B. Kaminska. "Testing Digital to Analog Converters Based on Oscillation-Test Strategy Using Sigma-delta Modulation". Int. Conf. on Comp. Design (ICCD 98), Oct. 1998.

[5] G. Huertas, D. Vazquez, A. Rueda,J.L. Huertas: "Oscillation-based Test Experiments in Filters: A DTMF Example", *Int. Mixed-signal Test Workshop*, pp.249-253, Whistler, June 1999.

[6] G. Huertas, D. Vazquez, A. Rueda, J.L. Huertas: "Effective Oscillation-Based Test for application to a DTMF Filter Bank". *Proc. IEEE Int. Test Conf.*, Sept. 1999, pp. 549-555.

[7] G. Huertas, D. Vazquez, A. Rueda and J.L. Huertas. "Practical Methods for Reading Test Outcomes in Oscillation-Based Test". *Int. Mixed-signal Test Workshop*, June 2000.

[8] J. Roh and J. Abraham. "A Comprehensive TDM Comparator Scheme for Effective Analysis of Oscillation-based Test". *Proc. IEEE VTS,* April 2000, pp143-148.

[9] S. Norsworthy, R. Schreier, G. temes: "Delta-sigma data converters", IEEE Press, 1997.