Multirate Cascaded Discrete-Time Low-Pass $\Delta\Sigma$ Modulator for GSM/Bluetooth/UMTS

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***Abstract*—This paper shows that multirate processing in a cascaded discrete-time $\Delta\Sigma$ modulator allows to reduce the power consumption by up to 35%. Multirate processing is possible in a discrete-time $\Delta\Sigma$ modulator by its adaptibility with the sampling frequency. The power reduction can be achieved by relaxing the sampling speed of the first stage and increasing it appropriately in the second stage. Furthermore, a cascaded $\Delta\Sigma$ modulator enables the power efficient implementation of multiple communication standards.**

The advantages of multirate cascaded $\Delta\Sigma$ modulators are demonstrated by comparing the performance of single-rate and multirate implementations using behavioral-level and circuit-level simulations.

This analysis has been further validated with the design of a multirate cascaded triple-mode discrete-time $\Delta\Sigma$ modulator. A 2-1 multirate low-pass cascade, with a sampling frequency of 80 MHz in the first stage and 320 MHz in the second stage, meets the requirements for UMTS. The first stage alone is suitable for digitizing Bluetooth and GSM with a sampling frequency of 90 and 50 MHz respectively. This multimode $\Delta\Sigma$ modulator is implemented in a 1.2 V 90 nm CMOS technology with a core area of 0.076 mm^2. Measurement results show a dynamic range of 66/77/85 dB for UMTS/Bluetooth/GSM with a power consumption of 6.8/3.7/3.4 mW. This results in an energy per conversion step of 1.2/0.74/2.86 pJ.

***Index Terms*—Cascade, CMOS, delta sigma modulation, multimode, multirate, sigma delta modulation.**

I. Introduction

BY exploiting oversampling, a $\Delta\Sigma$ modulator can digitize a narrow frequency band with a high resolution. Moreover, such a modulator is less sensitive to the non-idealities of its intrinsic building blocks compared to other analog to digital converters. This is partly due to the spread in frequency of the non-ideal effects by the oversampling and partly by the shaping obtained by the feedback action. This advantage will be increasingly important as the industry is driven by technology scaling, that continuously challenges the design of analog circuits with the ever increasing process variations and reduced supply voltages.

Although continuous-time (CT) $\Delta\Sigma$ modulators are sometimes favored over discrete-time (DT) modulators for their low-power consumption and wide-bandwidth performance, in case a high resolution is required, DT $\Delta\Sigma$ modulators are preferred for their easier implementation as cascaded structures. Indeed, higher resolution can be achieved by increasing the order of noise shaping. However, high-order single-loop $\Delta\Sigma$ modulators require careful design to prevent instability [1] and this can be avoided by cascading several inherently stable first- and second-order stages (known as Multi-stAge noise SHaping, MASH [2]–[4]). The cancellation of the quantization noise of the first stage in cascaded architectures is based on the perfect match between the transfer functions in the $\Delta\Sigma$ modulator and the digital filtering in the digital cancellation filters. This perfect match is more difficult to realize in CT $\Delta\Sigma$ modulators [5]. Moreover, CT $\Delta\Sigma$ modulators are highly sensitive to jitter and process variations [5]–[7], while DT $\Delta\Sigma$ modulators are appreciated for their robustness as their transfer functions rely on capacitor ratios. This advantage will become even more pronounced as technology will scale further. Finally, DT $\Delta\Sigma$ modulators offer a straightforward reconfigurability of the system by adjusting the sampling frequency. Nevertheless, since operational amplifiers (opamps) are required, the application of these $\Delta\Sigma$ modulators remains limited, so far, to sampling frequencies up to 300 MHz [8]–[11] and signal bandwidths up to 10 MHz [8], [9].

In this work, we exploit the distribution of the sampling frequency throughout DT $\Delta\Sigma$ modulators as an extra degree of freedom by adding a multirate dimension to the system [12]. This allows to reach a better power optimum for the overall system. The benefits of a multirate approach in a DT $\Delta\Sigma$ design can easily be seen when considering the first integrator in the modulator: the first integrator is usually the largest contributor in the overall power consumption. Errors in the first stage are not filtered by the loop and thus have the strongest impact on the $\Delta\Sigma$'s resolution [13]. Hence, the first integrator must be designed according to the overall dynamic range of the modulator. This results in higher specifications on its building blocks and consequently, larger power consumption. By reducing the sampling speed in the input stage, the power of the first integrator can be reduced while the resulting loss in resolution can be recovered by increasing the clock speed in the later stages of the system. This increased clock speed in the later stages of the modulator will hardly influence the required specifications

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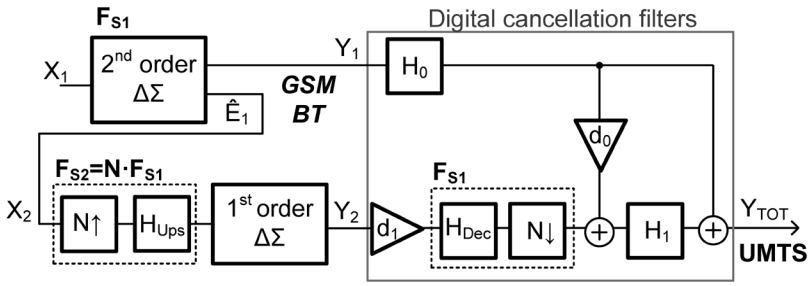

Fig. 1. Architecture of the triple-mode multirate 2-1 cascaded ΔΣ modulator with digital cancellation filters for UMTS, GSM and Bluetooth.

of its building blocks since their non-idealities (noise and distortion) are attenuated by the first stage. In this way, multirate processing can be exploited to trade performance for power and flexibility.

Multirate processing inside a single-loop ΔΣ modulator requires a decimator in the feedback path [12]. This decimation is critical since all its non-idealities are not suppressed by the loop. This complexity can be avoided when implementing a cascaded architecture in which the sampling frequency is modified between the cascaded stages, since there is no feedback from the second to the first stage.

A cascaded architecture also offers another advantage: a power efficient implementation in a multimode context by switching off the appropriate last stages when needed [9]. Each communication standard (in this work GSM, Bluetooth and UMTS) requires a certain resolution specification and hence a different order for the noise shaping [14], [15]. In a cascaded architecture, the modulator order is not fixed by the most demanding communication standard. Instead, the modulator can work for example as a second-order single-loop or as a 2-1 cascade depending on the standard specifications.

The multirate processing technique was already proposed in [12] in which behavioral-level simulations were used to show that the resolution of a cascaded ΔΣ with the first loop operating at a sampling frequency $F_S/2$ and the second loop at $2F_S$ is equivalent to the resolution of a cascade ΔΣ with both loops operating at F_S. That paper [12] concluded that the evidence of the power reduction of the first structure could only be quantified by transistor-level simulations. No integrated multirate cascaded discrete-time ΔΣ modulator has been reported to the author's knowledge. To date, two multirate ΔΣ modulator designs can be found in the literature: a single-loop discrete-time [16] and a multirate cascaded continuous-time [17] ΔΣ modulator. However, both these designs report simulation results only.

First, this work proves with behavioral-level and circuit-level simulations that multirate processing in DT cascaded ΔΣ modulators enables to reduce the power consumption. Second, this work presents the first implemented triple-mode DT multirate cascade ΔΣ modulator. The design was realized in 90 nm CMOS technology and achieves state-of-the-art performance [11]. The measurement results show a dynamic range of 66/77/85 dB for UMTS/Bluetooth/GSM with a power consumption of 6.8/3.7/3.4 mW. This results in an energy per conversion step of 1.2/0.74/2.86 pJ.

The paper is structured as follows. Section II describes the system-level architecture of the triple-mode multirate cascaded ΔΣ modulator. Section III presents a performance analysis, supported by circuit simulations, in which both single-rate and multirate approaches are compared in terms of resolution and power consumption. This analysis provides the specifications of the building blocks for the electrical design of the modulator. In Section IV, the system architecture and the circuit topologies of its various building blocks (opamps, switched-capacitor integrators, quantizers) are specified. Also the limitations and non-ideal effects on the design are discussed and advice for future implementations is given. Section V reports the measurement results and emphasizes the improvements that are obtained over a single-rate approach. Finally, Section VI concludes the work.

II. System-Level Architecture

The system-level architecture of the multirate cascaded ΔΣ modulator is shown in Fig. 1 together with the digital cancellation filters. The cascaded structure consists of a second-order first stage operating at a sampling frequency of F_{S1}, an upsampler with an integer upsampling factor N and a first-order second stage operating at a sampling frequency of $F_{S2} = N \cdot F_{S1}$. The digital output streams of both stages are recombined within the digital cancellation logic that, ideally, eliminates the quantization noise of the first stage. This recombination can be done at two different rates: either the output of the first stage is upsampled or the output of the second stage is downsampled, the latter being shown in the schematic of Fig. 1. The first second-order stage alone achieves a sufficient performance for the Bluetooth and GSM standards while the full 2-1 cascade is necessary to meet the UMTS specification.

A detailed block diagram of the modulator, without digital cancellation filters, is shown in Fig. 2. The first stage uses a feedback topology with an extra feedforward branch from the input to the second integrator input to reduce the output swing of the first integrator. In both stages, 1.5-bit quantizers are employed to further reduce the output swing of the integrators and improve the dynamic range of the modulator. This can be done easily because a 1.5-bit (three-level) digital analog converter (DAC) can readily be implemented using a fully differential switched-capacitor circuit [18].

To calculate the transfer function of a ΔΣ modulator, the quantizer is replaced by a linear model ($y = k_q x + e(x)$ with

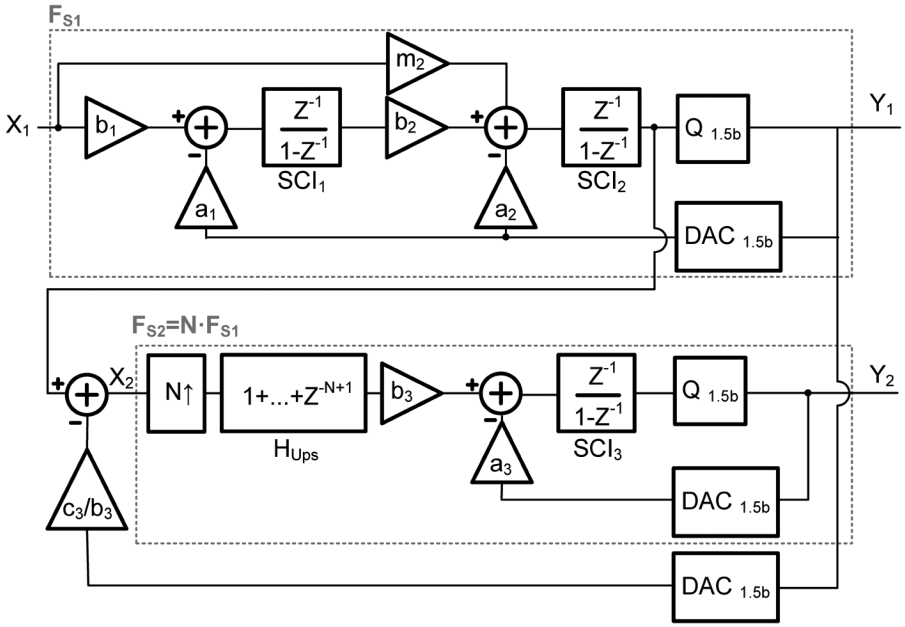

Fig. 2. Circuit implementation of the multirate 2-1 cascaded $\Delta\Sigma$ modulator.

k_q the quantizer gain and $e(x)$ the quantization noise). The digital output streams of the first and second stages Y_1 and Y_2 operating with a sampling frequency of F_{S1} and $F_{S2} = NF_{S1}$ respectively can be expressed as

$$Y_1(z) = \frac{b_1}{a_1}z^{-2}X_1(z) + m_2 z^{-1}(1-z^{-1})X_1(z) + (1-z^{-1})^2 E_1(z) \quad (1)$$

$$Y_2(z) = \frac{b_3}{a_3}z^{-1}H_{\mathrm{Ups}}X_2(z^N) + (1-z^{-1})E_2(z) \quad (2)$$

with

$$X_2(z) = \frac{Y_1(z)-E_1(z)}{k_{q1}} - \frac{c_3}{b_3}Y_1(z) = b_2 a_1 \left(Y_1(z)-E_1(z)\right) - \frac{c_3}{b_3}Y_1(z) \quad (3)$$

and the upsampling filter H_{Ups}

$$H_{\mathrm{Ups}} = 1 + \ldots + z^{-N+1} \quad (4)$$

while k_{q_1}, k_{q_2} are respectively the quantizer gain of the first and second stage, $X_1(z)$, $E_1(z)$ and $X_2(z)$, $E_2(z)$ stand for the input signal and quantization noise of the first and second stage, respectively. The relationship between the loop coefficients and the quantizer gain are derived by ensuring a second-order noise shaping in the first stage:

$$b_2 a_1 k_{q_1} = 1 \quad (5)$$

$$a_2 = 2a_1 b_2 \quad (6)$$

and a first-order shaping in the second stage [13]:

$$a_3 k_{q_2} = 1. \quad (7)$$

After upsampling the digital output of the first stage and processing the two digital streams in the cancellation filter, the output of the full cascade becomes

$$Y_{\mathrm{tot}}(z) = H_{d1}(z)(1+\ldots+z^{-N+1})Y_1(z^N) + H_{d2}(z)Y_2(z). \quad (8)$$

In order to cancel the quantization noise of the first stage $(E_1(z))$, the digital cancellation filters must be chosen equal to

$$H_{d1} = z^{-1}\left(d_0(1-z^{-N})^2 + 1\right) \quad (9)$$

$$H_{d2} = d_1(1-z^{-N})^2 \quad (10)$$

with

$$d_0 = \frac{c_3}{b_3 b_2 a_1} - 1 \quad (11)$$

$$d_1 = \frac{a_3}{b_3 b_2 a_1}. \quad (12)$$

The output of the cascade gives after perfect cancellation of $E_1(z)$

$$Y_{\mathrm{tot}}(z) = H_{\mathrm{Ups}}(z)z^{-(N+1)}\left[\frac{b_1}{a_1}z^{-N} + m_2(1-z^{-1})^N\right]X_1(z) + d_1(1-z^{-N})^2(1-z^{-1})E_2(z). \quad (13)$$

III. Performance Analysis

This section extracts the performance in terms of resolution and power consumption for the 2-1 cascaded $\Delta\Sigma$ modulator (shown in Fig. 2) for different settings of the upsampling factor N and the sampling frequency F_S used in the first stage. First, the resolution is estimated using behavioral-level simulations with an ideal model. Next, to compare the power consumption of each configuration, simulations of transistor-level opamps are performed. Since the global power consumption is dominated by the opamps, the required specifications on these amplifiers,

TABLE I
RESOLUTION OF THE DIFFERENT CONFIGURATIONS OF 2-1 CASCADE ΔΣ MODULATOR OBTAINED BY BEHAVIORAL-LEVEL SIMULATIONS

Configuration	Stage 1 F_{S_1} [MHz]	Stage 2 F_{S_2} [MHz]	Resolution ENOB	
Single-rate	80	80	10	(1)
	160	**160**	**13.3**	**(2)**
Multirate N=2	80	160	11.3	(3)
	160	320	15	(4)
Multirate N=4	**80**	**320**	**13.5**	**(5)**

GBW and SR, are determined to estimate the global power consumption.

A. Extraction of the Resolution

In this section the resolution is determined for an ideal cascaded ΔΣ modulator for different upsampling factors and sampling frequencies. The 2-1 cascade ΔΣ modulator described in Section II has been modeled by using functional blocks in Simulink [19].

The five different test cases in the behavioral-level simulations are shown in Table I. Among these test cases, three upsampling factors were considered: $N = 1$ for the single-rate case, $N = 2$ and $N = 4$ for the multirate case. The $N = 4$ multirate setting is chosen as a reference for comparison. In this reference design, the oversampling ratio for the first stage is chosen to achieve an overall ENOB for the cascade higher than 10 bits in a signal bandwidth of 1.92 MHz (the specification for UMTS). This leads to a sampling frequency in the first stage of 80 MHz. In the single-rate as well as in the $N = 2$ multirate case, sampling frequencies of 80 MHz and 160 MHz have been considered for the first stage to study the effect of the sampling frequency and the upsampling factor on the resolution and power consumption.

The following settings were used in the behavioral-level model:

- All the loop coefficients, shown in Fig. 2, are equal to 1/2. Their value was maximized, in order to minimize the capacitive load, until the output swing of the integrators hits half the supply voltage ($V_{\text{swing}}^{\text{MAX}} = V_{\text{dd}}/2$). In these conditions, d_0 is equal to 3 [using (11)] and d_1 equal to 2 [using (12)].
- The reference voltage of the DAC is fixed to 0.8 V. Increasing the reference voltage increases the dynamic range of the modulator. However, the outputs of the opamps require a certain headroom to function properly. This headroom is determined by the saturation requirement of the output stage of the opamp.
- The input sine wave amplitude is set to $V_{\text{dd}}/2$.

The resulting ENOB are given in Table I. We observe that the single-rate setting with $F_{S_1} = 160$ MHz (second row in Table I), the multirate setting with $N = 2$ and $F_{S_1} = 160$ MHz (fourth row in Table I) as well as the multirate setting with $N = 4$ and $F_{S_1} = 80$ MHz (fifth row in Table I) achieve the highest ENOBs. Hence, they are the preferred configurations to provide a sufficient SNDR margin for the transistor-level design. As predicted by [12], the resolution of the single-rate cascade at 160 MHz (second row in Table I) and the multirate cascade, with the first stage at 80 MHz and the second stage at 320 MHz (fifth row in Table I), achieve similar performance.

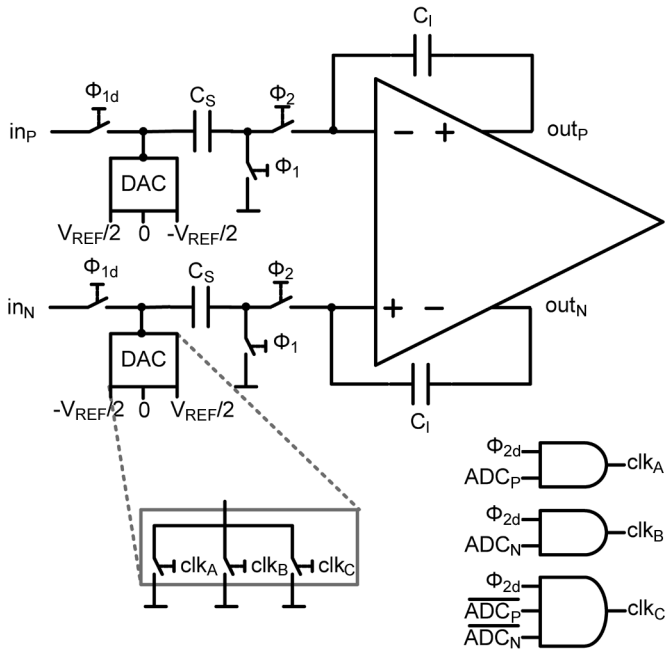

Fig. 3. Implementation of the discrete-time switched-capacitor integrator with a three-level DAC.

B. Extraction of the Power Consumption

In this section, the power consumption is analyzed for three out of the five test cases above [(1), (2), and (5)] from Table I. The total power consumption of the system is mainly determined by the GBW and SR metrics of the opamps and these amplifiers are assumed to be the dominant contributors in the global power consumption. This assumption will be confirmed by the transistor-level simulations of the global system as described in Section IV-E. The modulator in Fig. 2 has been implemented in Spectre with all the opamps blocks mapped to a transistor-level design in a 90 nm CMOS technology. All the other building blocks were modeled using a Verilog-A model. The power consumption estimation was realized by extracting the required current specifications for the opamps in the different configurations.

The circuit-level model was built as follows:

- Each switched-capacitor integrator (SCI) was implemented as shown in Fig. 3 (more explanation can be found in Section IV-A). The capacitive loading for each opamp was added in the circuit-level model.
- The main design criteria for the opamp in the SCI are sufficient DC gain and output swing, large GBW and SR. A two-stage opamp topology was chosen to provide DC gain up to 55 dB [20]. The amplifier consists of a folded-cascode input stage followed by a Miller compensated common-source stage [Fig. 4(a)]. As can be seen, one cascode transistor in the first stage was removed to ensure the saturation for the three stacked transistors fed with a supply voltage of 1.2 V. The second stage was added to increase the output swing of the opamp. The specifications on the GBW and

TABLE II
SPECIFICATIONS ON THE OPAMPS AND RESOLUTION FOR DIFFERENT CONFIGURATIONS OF THE 2-1 CASCADE $\Delta\Sigma$ MODULATOR OBTAINED BY OPAMP TRANSISTOR-LEVEL SIMULATIONS

Configuration	Opamp	GBW [MHz]	I_{Bias} [mA]	I_{out} [mA]	I_{TOT} [mA]	Resolution ENOB
(1) Single-rate F_{S_1}=80 MHz	1	235	0.075	0.17	0.53	9.5
	2	235	0.075	0.17	0.53	
	3	140	0.05	0.11	0.35	
(2) Single-rate F_{S_1}=160 MHz	1	950	0.55	0.32	2.1	12.9
	2	950	0.55	0.32	2.1	
	3	800	0.425	0.17	1.4	
(5) Multirate N=4 F_{S_1}=80 MHz	1	660	0.278	0.17	1.06	12.1
	2	660	0.278	0.17	1.06	
	3	760	0.34	0.35	1.6	

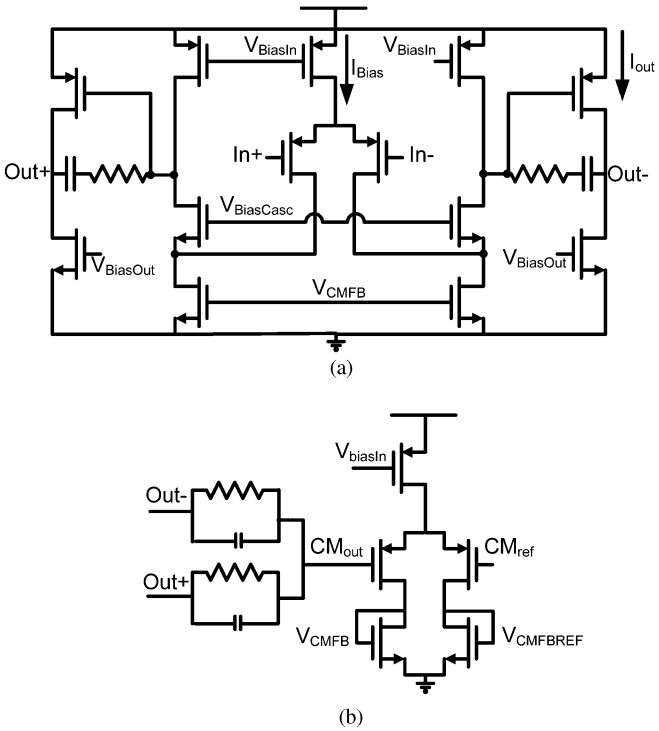

Fig. 4. Topology of (a) the opamp and (b) its common-mode feedback circuit.

the internal SR (determined by the bias current $I_{\rm Bias}$ of the input stage and the Miller capacitor) determine $I_{\rm Bias}$. The external SR (determined by the output stage current $I_{\rm Out}$ and the load capacitance) of the amplifiers can be adjusted according to the required sampling frequency by varying $I_{\rm Out}$. The Miller capacitor is chosen to be about a factor of 2 smaller than the load capacitor. To reduce the power consumption, the output current is reduced as much as possible (which decreases the external SR). Therefore, in this case, the external SR is similar to the internal SR. The continuous-time common-mode feedback circuit is given in Fig. 4(b). A small capacitor was added in parallel with the common-mode sensing resistors to provide sufficient common-mode phase margin.

- The input sampling capacitors are set to 450 fF and 300 fF for the first and second SCI of the first stage and 200 fF in the SCI of the second stage. These capacitor values result from a compromise between kT/C noise, matching sensitivity and capacitive loading of the opamps.
- The switches are modeled in Verilog-A with an on/off-resistance.
- The quantizers in Verilog-A have a delay, rise and fall time.
- The upsampler is modeled by an ideal sample and hold controlled by the clock of the first stage. The samples held are then transferred to the second stage at a rate N times higher depending on the test case.

The minimum requirements (shown in Table II) for the three opamps in the 2-1 cascade in the three configurations have been found by iteratively decreasing their value until the modulator resolution starts to degrade.

The external SR and the related $I_{\rm out}$, behave as expected; doubling the sampling frequency in the first stage requires doubling the $I_{\rm out}$ of the first stage amplifiers [from case (1) to (2) for Opamp 1 and Opamp 2]. The external SR requirement on the second stage amplifier (Opamp 3) is relatively lower than that of the first stage (Opamp 1 and 2) in the single-rate cases [(1) and (2)]. This can be explained by the fact that the first stage has the highest impact on the overall resolution and thus the specifications on its building blocks are the most demanding.

Considering the GBW, the internal SR and the related $I_{\rm Bias}$, it can be seen that the requirements in the second-stage amplifier (Opamp 3) are also relatively lower than those of the first stage (Opamp 1 and 2) in the single-rate cases [(1) and (2)]. The $I_{\rm Bias}$ requirements of the first stage are halved when comparing the single-rate case at 160 MHz and the multirate case [case (2) to (5)]. The requirements of the single-rate case at 80 MHz and the one at 160 MHz cannot be compared since the resolution of the first test-case is lower.

These observations lead to the conclusion that, in order to achieve low power consumption, the sampling frequency of the first integrator needs to be kept as low as possible. Moreover, increasing the sampling frequency in the second stage can be done without substantially affecting the power consumption.

To obtain the total current consumption $I_{\rm TOT}$ of each opamp for each configuration, the current of the input stage, the output stage, the cascode and the CMFB circuit of each opamp are summed. Consequently, the multirate setting with a minimal F_{S_1} and a maximal F_{S_2} $(N = 4)$ appears to be the optimal in terms of power consumption for a fixed resolution. The total output current consumption of this setting (5) is 35% lower than that of the single-rate case, sampling at 160 MHz (2).

The resolution of the different circuit-level configurations (Table II) is comparable with the results found by behavioral-level simulations in Simulink (Table I).

IV. Circuit Implementation

To validate the concept at the transistor-level and verify the results obtained in Section III, the multirate 2-1 cascade ΔΣ modulator of Fig. 2 has been implemented in a 90 nm digital CMOS process. The circuit was designed to operate at an upsampling factor of 4 and a sampling frequency $F_{S_1} = 80$ MHz. A single-rate setting of 80 MHz was also implemented for comparison purposes.

To demonstrate the multimode performance of the cascaded ΔΣ modulators, the first stage alone was designed to digitize GSM and Bluetooth at a sampling frequency of 50 MHz and 90 MHz, respectively. The two-stage cascade was targeted for the UMTS standard with a sampling frequency of 80 MHz and 320 MHz in the first and the second stage, respectively.

This section describes the overall chip implementation and the topology of the building blocks in the ΔΣ modulator. The different building blocks used in the system are the switched-capacitor integrators, the quantizers and the upsampler.

A. Switched-Capacitor Integrator

The topology of the SCI is shown in Fig. 3. This circuit employs bottom-plate sampling to reduce the sensitivity to parasitic capacitances and charge injection. The switches are implemented as MOS transmission gates, which comprise the parallel connection of an nMOS and a pMOS switch to reduce the dependency of the on-resistance with the drain source voltage. The bias current I_{Bias} of the input stage of the opamp shown in Fig. 4, is determined by the specifications on the GBW and the internal SR. It is set to approximately 350 μA. As this current has a negligible contribution to the total power consumption, it is fixed for the three amplifiers. The width of the output transistor of the amplifier for the third integrator was doubled with respect to the first and second one, in order to provide the necessary double output current I_{out} in the multirate case with $N = 4$. The bias current I_{Bias} and output stage current I_{Out} can be adjusted to achieve the required GBW, the internal SR and the external SR of all opamps during measurements. The continuous-time common-mode feedback only consumes about 300 μA of current. MOM-capacitors were used to enable the fabrication in a digital 90 nm CMOS process.

B. Quantizer

The 1.5-bit quantizer needs to perform a three-level quantization of the input. It consists of two identical blocks, comprising a comparator preceded by a switched-capacitor (SC) network [Fig. 5(a)]. This SC network generates two voltage thresholds at a level of $V_{\mathrm{DD}}/2 + V_{\mathrm{REF}}/3$ and $V_{\mathrm{DD}}/3 - V_{\mathrm{REF}}/3$ by shifting the positive or the negative input signal by $V_{\mathrm{REF}}/3$ depending on the threshold. The used sampling capacitor is 200 fF. The 1.5-bit output data, is extracted by subtracting both outputs.

The comparator [Fig. 5(b), left] is based on a regenerative latch driving a Set-Reset (SR) latch [Fig. 5(b), right].

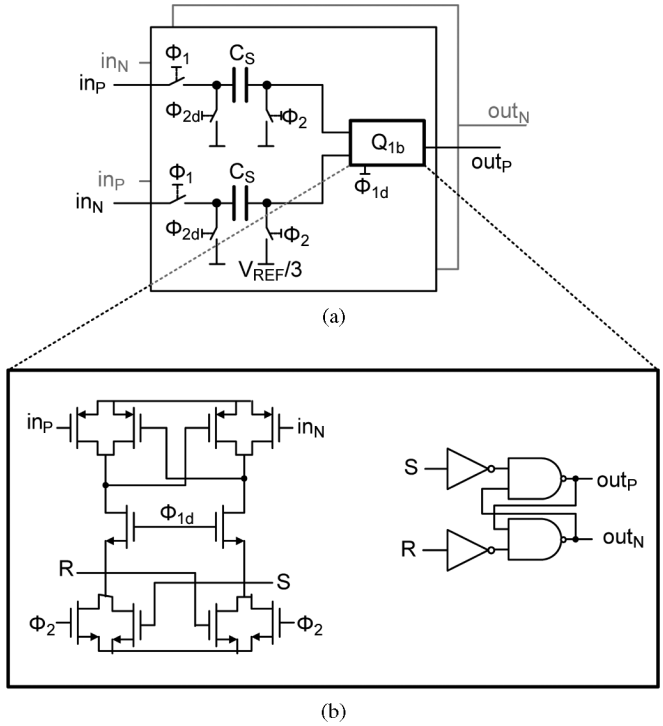

Fig. 5. Implementation of (a) the 1.5-bit quantizer and (b) the comparator.

C. Upsampler

The upsampler interpolates the quantization error signal of the first stage by a factor of 4. The quantization error is equal to the subtraction of the output of the loop filter and the digital output of the ADC. The upsampling operation for the output of the loop filter is implemented by replacing the switched-capacitor sampling network of *SCI*$_3$ by the structure in Fig. 6. During Φ_{ups}, the output of *SCI*$_2$ is sampled on four equal sampling capacitors, each with a value of 200 fF. The samples are then successively processed in four clock phases $\Phi_{22\mathrm{divi}}$ by *SCI*$_3$, using the 4 times faster clock of the second stage. Since the output of the 1.5-bit quantizer is held constant during the entire sampling period of the first stage, its voltage can be sampled directly with the sampling clock of the second stage.

In addition to this multirate mode, a single-rate mode for the cascade is foreseen by processing only one of the four upsampling capacitors.

D. Non-Idealities and Limitations of the Modulator

This section provides some considerations about the non-idealities in this multirate cascade ΔΣ modulator. It also gives some hints for future implementations. Finally, the limitations for the application of this multirate cascade ΔΣ modulator are discussed.

- In the current implementation, the upsampler loads the second SCI by its four parallel sampling capacitors, which increases the capacitive load for this SCI. Moreover, the short sampling time Φ_{Ups} of the upsampler requires the second SCI to settle in a 4 times shorter time frame. This constraint therefore increases the required GBW and SR specifications and this results in similar requirements for the second opamp as for the first one. This effect was also

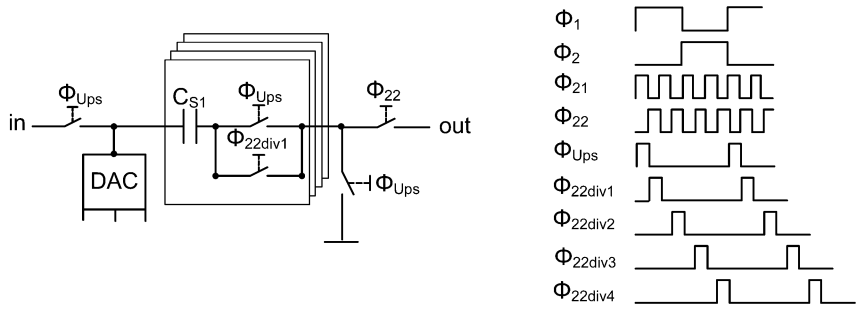

Fig. 6. Implementation of the upsampler.

TABLE III
PERFORMANCE FOR THE 2-1 CASCADE $\Delta\Sigma$ MODULATOR OBTAINED BY TRANSISTOR-LEVEL SIMULATIONS

Standard	F_S [MHz]	Resolution ENOB	Power [mW]
UMTS	80/320	11	6.6
UMTS	80/80	9.5	6.2
GSM	50	12.9	3.2
Bluetooth	90	11.3	3.36

observed in the circuit-level simulations in Section III-B. In addition, the quantizer of the first stage needs to settle 2 to 4 times faster, because its decision is already needed in Φ_{22}. Fortunately, the power consumption of this faster quantizer is negligible with respect to the one of the amplifiers. The two discussed issues could be alleviated by several techniques, e.g., the time-interleaving of the sampling capacitor of the second stage and allowing a clock cycle delay $1/F_S$ in the architecture.

- In a future design, extra attention will be devoted to isolating the sampling of the output of the second integrator by the upsampler from the sampling by the quantizer of the first stage. If both sampling events occur at the same instant, the load of the second integrator is increased and sampling spikes are produced. To counteract this, the quantizer of the first stage was slightly skewed, but in a future design a more elegant solution should be found. An alternative solution is to use a feedforward structure in the first stage. Indeed, in a feedforward structure, the input of the second stage is taken directly after the second integrator, so before the feedforward addition. This ensures a proper isolation between the quantizer sampling and the upsampler by the adder. Unfortunately, this architecture requires an adder, which results in extra power consumption.
- As mentioned in the introduction, cascaded $\Delta\Sigma$ modulators in general are sensitive to capacitor mismatches. To verify this sensitivity, the sampling capacitors were modified by 1% and the performance, resulting from this transistor-level simulation, showed that there is no impact. This was confirmed by the measurements, which proved that an optimization of the digital coefficients in the digital cancellation filters did not increase the performance. A simulation of the transistor-level implementation in the four process corners showed a maximum loss of 1 bit in the case of slow–slow.

TABLE IV
CURRENT BREAKDOWN FOR THE MULTIRATE 2-1 CASCADE $\Delta\Sigma$ MODULATOR AS OBTAINED BY TRANSISTOR-LEVEL SIMULATIONS

Part	Current [mA]	Percentage %
SCI_1	1.1	20
SCI_2	1.1	20
Q_1	0.2	3.6
Clk	0.12	2.2
SCI_3	1.6	29
Q_2	0.35	6.3
Clk_2	0.46	8.3
BiasOA	0.43	2.8

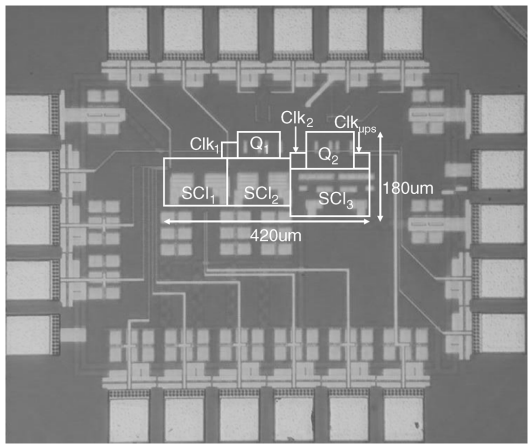

Fig. 7. Chip microphotograph.

- The proposed multirate cascade requires a 4 times higher sampling frequency in the second stage. The attainable bandwidth in the design of operational amplifiers limits the maximum sampling frequency to about 320 MHz nowadays. The simulations of the implemented switched-capacitor integrator in the second stage show, however, that the output only has to settle to about 70% of the theoretical predicted output, without deteriorating the performance. Nevertheless, for communications standards with signal bandwidths larger than 10 MHz, the application of this multirate cascading can be limited by the achievable sampling frequency of the opamps. In this case, it will be necessary to limit the upsampling factor to maximally 2.

E. Simulated Transistor-Level Performance

To extract the nominal resolution of the multirate cascade, transistor-level simulations of the full chip for each standard

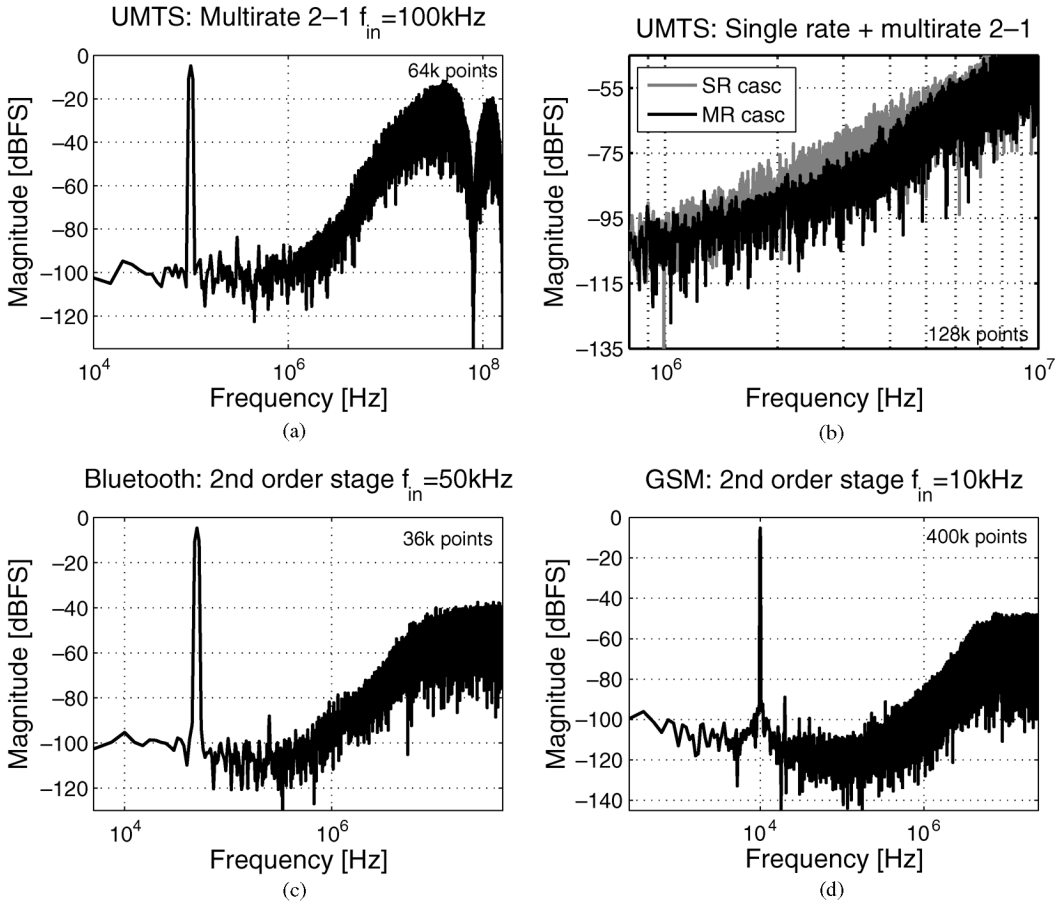

Fig. 8. (a) Measured spectra at peak SNDR for UMTS; (b) the comparison of the multirate and single-rate cascade for UMTS zoomed in from 0.8 MHz until 10 MHz, (c) Bluetooth and (d) GSM.

have been performed. The resolution and power consumption are summarized in Table III. The UMTS standard was simulated with a sine wave input with an amplitude of 0.8 V and a frequency of 0.5 MHz. The cascade is also simulated in a single-rate mode at 80 MHz. The cascade could not be simulated with a sampling frequency of 160 MHz since the first stage is not designed for this higher sampling frequency.

A simulated current consumption breakdown of the full multirate cascade is also shown in Table IV. These power figures show that, although the second stage works at four times the sampling frequency of the first stage, its consumption remains comparable to the first stage SCIs. This is achieved by relaxing its specifications and therefore demonstrates the potential of a multirate approach in cascaded $\Delta\Sigma$ modulators. It also confirms the assumption that the power consumption is determined by the operational amplifiers. The transistor-level simulations of both the resolution and the power consumption are in good agreements with the mixed-level simulations of Section III-B.

The modulator has been fabricated in a digital 90 nm CMOS process [11], which means that no analog options were provided. The chip microphotograph is shown in Fig. 7. The active area of the modulator including switched-capacitor integrators, quantizers, clock generation and DAC is only 0.076 mm^2. The processing by the digital cancellation filters is done in Matlab.

V. Experimental Results

This section discusses the measurement results: resolution, power consumption, distortion, comparison of multirate and single-rate mode and the comparison with other multimode discrete-time $\Delta\Sigma$ modulators.

A. Resolution and Power Consumption

The measurement of the UMTS mode spectrum generated by the multirate cascaded technique is shown for the peak SNDR in Fig. 8(a), where the notch at $F_{S_2}/4$ results from the upsampling in the digital cancellation logic. With a total power consumption of 6.83 mW drawn from 1.2 V supply, a peak SNDR of 65.5 dB is achieved. This results in an ENOB of 10.5-bit and a figure of merit $\text{FoM} = \text{Power}/2\text{BW}2^{\text{ENOB}}$ of 1.2 pJ per conversion step for the multirate cascade.

The output spectrum of the modulator in the GSM and Bluetooth modes are shown for peak SNDR in Fig. 8(c) and (d). With a power consumption of 3.43 mW and 3.7 mW, a peak SNDR of 77 dB and 76 dB is achieved for GSM and Bluetooth, respectively. This results in a FoM of 2.86 pJ/conv and 0.74 pJ/conv.

The resolution as well as the power consumption are in good correlation with the transistor-level estimations.

Fig. 9 shows the SNDR versus the input amplitude for the different modes. A dynamic range (DR) of 66/77/85 dB is achieved for UMTS/Bluetooth/GSM, respectively.

TABLE V
MEASURED PERFORMANCE OF THE 2-1 CASCADE $\Delta\Sigma$ MODULATOR FOR 3 STANDARDS

Performance	GSM	Bluetooth	UMTS
Architecture	2^{nd} order 1^{st} stage	2^{nd} order 1^{st} stage	2-1 multirate
Signal bandwidth	100 kHz	500 kHZ	1.92 MHz
Sampling frequency	50 MHz	90 MHz	80/320 MHz
OSR	250	90	20/80
DR	85 dB	77 dB	66 dB
Peak SNDR	77 dB	76 dB	65.5 dB
THD at peak SNDR	-80.5 dB	-81 dB	-75 dB
SFDR	83 dB	83 dB	79 dB
IM3	76 dB	76 dB	76 dB
Input Range	$0.8\ V_{pp-diff}$		
Power (1.2 V supply)	3.43 mW	3.7 mW	6.83 mW
FoM	2.86 pJ/conv	0.74 pJ/conv	1.17 pJ/conv
Core area	$0.076\ mm^2$		

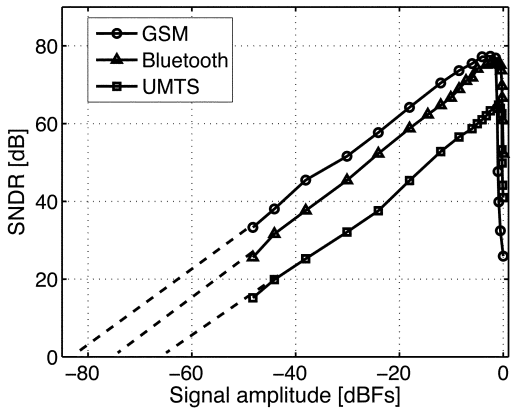

Fig. 9. Measured SNR versus input amplitude of the $\Delta\Sigma$ modulator for three standards: UMTS, Bluetooth and GSM.

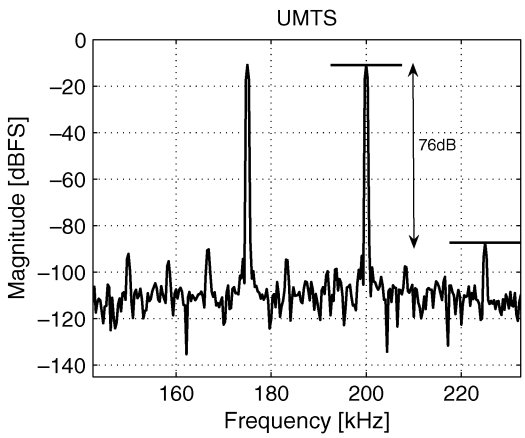

Fig. 10. Measured third order intermodulation distortion of the multirate 2-1 $\Delta\Sigma$ modulator for UMTS.

B. Distortion

The spectrum resulting from a 2-tone test with 175 and 200 kHz in the UMTS mode is shown in Fig. 10. The third-order intermodulation distortion (IM3) is 76 dB with each tone at -10.9 dBFS (the power where the peak SNDR has been reached). Similar performance is obtained for the other modes.

A total harmonic distortion (THD) of 75/81/80.5 dB and a spurious-free dynamic range (SFDR) of 79/83/83 dB is reached at the peak SNDR for UMTS/Bluetooth/GSM.

C. Comparison of Single-Rate and Multirate Performance

The multirate performance was also compared to a single-rate performance at a sampling frequency of 80 MHz (the slew-rate requirements of the amplifiers are reduced accordingly). The single-rate setting provides a marginal reduction of the power consumption (6.43 mW). However, the SNDR dropped by 7 dB. The resulting FOM is 2.38 pJ/conv, which is the double of the multirate setting. This clearly shows that multirate operation offers a performance improvement. The top right of Fig. 8(b) shows the shaping improvement of the multirate approach on the output spectrum.

The single-rate setting has a THD of -68.3 dB at a peak SNDR and a SFDR of 70.5 dB.

D. Conclusion

Table V summarizes the measured performance of the design. Fig. 11 compares the FoM (computed with DR) of different multimode discrete-time $\Delta\Sigma$ modulators [9], [21]–[25]. Refs. [21], [22], [24] use a single-loop architecture to realize a multimode $\Delta\Sigma$ modulator, while [9], [23], [25] employ a cascaded architecture. The four stars on the figure represent the achieved performance for GSM, Bluetooth, the non-optimized single-rate alternative for UMTS and the proposed multirate solution for UMTS. It can be observed that the proposed chip demonstrates state-of-the-art performance. Refs. [21], [24] use 0.18-μm technology, the rest 0.13-μm technology and their area is at least 2.5 times as large as this work [11].

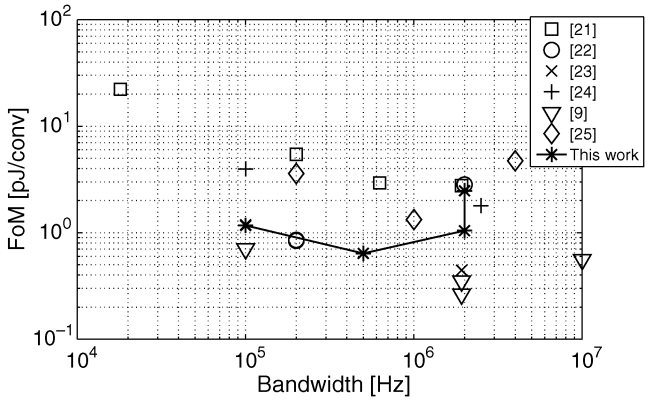

Fig. 11. Comparison of FoM with other multimode discrete-time $\Delta\Sigma$ modulators.

VI. Conclusion

This work proves that multirate processing in cascaded discrete-time $\Delta\Sigma$ modulators allows to reduce the power consumption without a significant resolution penalty. The high-level and mixed-level simulations show a power reduction of up to 35% by halving the sampling frequency of the first stage and doubling the one of the second stage in a 2-1 cascaded architecture.

The implementation of the proposed triple-mode multirate cascaded $\Delta\Sigma$ modulator verify the concept and show a close match between the simulated and the measured performance.

The measurement results show that this triple-mode $\Delta\Sigma$ modulator for UMTS/GSM and Bluetooth has state-of-the-art performance. This triple-mode multirate cascaded $\Delta\Sigma$ modulator achieves a dynamic range of 66/77/85 dB for UMTS/Bluetooth/GSM with a power consumption of 6.8/3.7/3.4 mW. This results in an energy per conversion step of 1.2/0.74/2.86 pJ.

Furthermore, this implementation shows that a cascaded structure is a power-efficient architecture for multimode requirements.

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