

LC-VCO Design Optimization Methodology Based on the g_m/I_D Ratio for Nanometer CMOS Technologies

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Abstract

In this paper, an LC-VCO design optimization methodology based on the g_m/I_D technique and on the exploration of all inversion regions of the MOS transistor is presented. An in-depth study of the compromises between phase noise and current consumption permits optimization of the design for given specifications. Semi-empirical models of MOS transistors and inductors, obtained by simulation, jointly with analytical phase noise models, allow to get a design space map where the design trade-offs are easily identified.

Four LC-VCO designs in different inversion regions in a 90 nm CMOS process are obtained with the proposed methodology and verified with electrical simulations. Finally, the implementation and measurements are presented for a 2.4 GHz VCO operating in moderate inversion. The designed VCO draws 440 μA from a 1.2V power supply and presents a phase noise of -106.2 dBc/Hz at 400 kHz from the carrier.

I. INTRODUCTION

The increasing demand of wireless applications with special emphasis on low power requirements forces radio-frequency designers to work at the limits of the technology. To achieve these challenging specifications, best performance is mandatory in each block of the circuit, especially in terms of power consumption, noise and linearity. In addition, since a few years ago, the extended use of CMOS technologies enables RF designers to reduce costs as well as reaching good performance.

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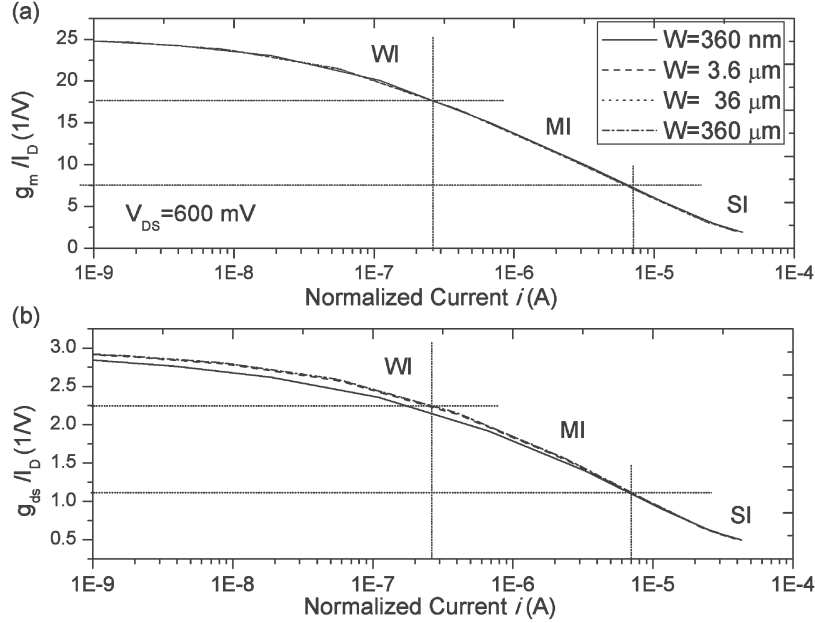


Fig. 1. (a) g_m/I_D and (b) g_{ds}/I_D vs. $i = I_D/(W/L)$ for four nMOS transistors and a $V_{DS} = 600$ mV. Typical limits of strong (SI), moderate (MI) and weak (WI) inversion regions are shown.

The requirements of an RF block, such as gain, noise or power consumption, strongly depend on the RF application. For example, an application that is very demanding in terms of noise would need to accept high power consumption, whereas a very low power design would cope with just enough non-very-low noise values. As these two characteristics are directly related, their trade-off has to be achieved optimizing the design of RF blocks. This work explores those compromises in order to optimize inductor-capacitor-tank voltage controlled oscillators (LC-VCOs). This study is relevant as VCOs, due to their phase noise, are responsible for most part of the error in the processed signal in an RF receiver [1], as well as for a non-negligible percentage of the system current consumption. The mentioned optimization is done by exploiting the consumption-spectral purity trade-off of the VCOs in order to use just the needed current to fulfill the application requirements. This is achieved by using the ratio of transconductance to drain current g_m/I_D methodology presented in [2], [3] and taking advantage of operation in all the inversion regions (weak, moderate and strong) of the MOS transistor (MOST) [4].

The g_m/I_D ratio of a saturated MOST is directly related to its inversion level. The inversion level is directly associated with the normalized current or current density, defined as $i = I_D/(W/L)$ and dependent on the gate, source and drain voltages [5]–[7]. The relationship between g_m/I_D and i -and hence I_D for a certain MOST aspect ratio W/L - is biunivocal; a typical form of this curve can be

appreciated in Fig. 1(a). Several factors make the g_m/I_D ratio a very useful parameter for describing the state of operation and performance of a MOST and exploring its design space. Firstly, the ease to write circuit design expressions as a function of this parameter, since generally the transconductance or the current are part of them. Secondly, its value gives a direct indication of the inversion region and of the efficiency of the transistor in translating current consumption into transconductance. Finally, its variation is constrained to a very small range, efficiently covered with a grid of some tens of values of g_m/I_D (e.g. from $3 V^{-1}$ to $28 V^{-1}$ for a nanometer bulk nMOS). Utilizing this variable on the expressions of the VCO characteristics and sweeping g_m/I_D allows to obtain a set of design space maps of phase noise, gain, power consumption, among others, as it will be shown in Section V. This graphical representation helps the designer to study the evolution and trade-offs of some of these characteristics when working in any of the three inversion regions.

The MOST channel length reduction, as it is shown below, permits the design of RF blocks in weak and moderate inversion (WI/MI) with less power consumption than when they are biased in the traditional way, in the strong inversion (SI) region. Several RF blocks designed in CMOS technologies and working in MI or WI have been reported in the last decade. Porret et al. [8] and Melly et al. [9] present, respectively, the design of a receiver and a transmitter working at 433 MHz in MI. Ramos et al. [10] showed a 950 MHz LNA in MI-WI. The authors have presented an RF amplifier for 900 MHz [11] and a 2.4 GHz VCO [12] both designed in MI regions. Lee and Mohammadi [13] presented a 2.4 GHz VCO design in WI whereas Hsieh and Lu [14] designed a 5 GHz receiver front-end in MI and WI. Finally, Perumana et al. [15] designed a subthreshold 2.4 GHz receiver. Although the mentioned works successfully take advantage of working in these MOS regions of operation, they do not present a systematic methodology for choosing the operating point. This issue is covered in this paper for LC-VCOs.

The effect of moving from SI through WI implies a considerable current reduction, but as a counterpart, parasitic capacitances are higher as the transistor dimensions increase. That is why, with sub-micrometer technologies, high frequency design in MI is limited to around one gigahertz [11]. Nowadays, the advent of nanometer CMOS technologies prepared for radio-frequency designs enable to design in MI with working frequencies of several gigahertz. This idea considers the conservative limit where the MOS transistor frequency is below the quasistatic-limit frequency of one tenth of f_T [4], with f_T the MOST transition frequency. To visualize these facts, f_T and g_m/I_D versus I_D are depicted in Fig. 2 for a pMOS transistor in 90 nm technology. These results show that increasing I_D (i.e. moving to SI) leads to a rise in f_T and a reduction in the g_m/I_D ratio. It is also appreciated in Fig. 3, where the relation between f_T and g_m/I_D and the overdrive voltage $V_{OD} = V_{GS} - V_T$, a parameter classically utilized in RF designs

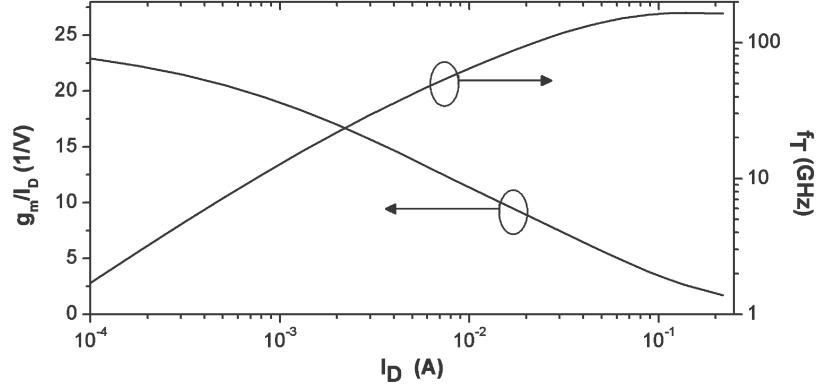


Fig. 2. g_m/I_D and f_T versus I_D of a pMOS transistor with an aspect ratio of $360 \mu\text{m}/100 \text{ nm}$.

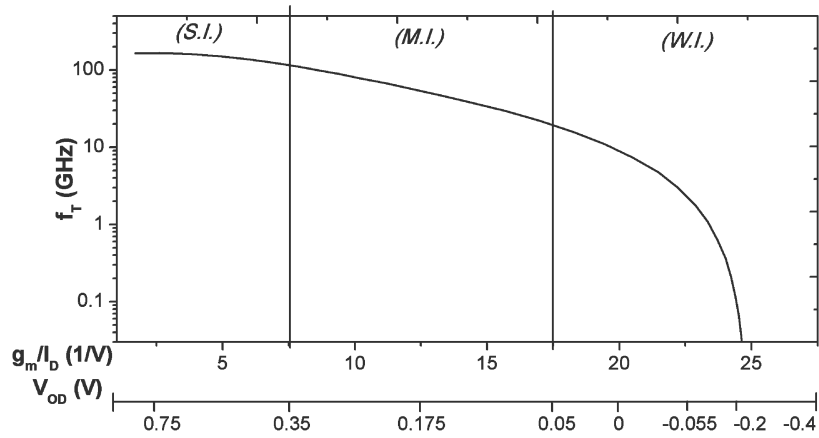


Fig. 3. f_T versus g_m/I_D and versus the overdrive voltage V_{OD} for nMOS transistors.

to indicate the bias point, are depicted. These plots also show that, in spite of the considerable fall in f_T when working in MI, the resulting value is enough to work in the RF range of some gigahertz.

The proposed optimization methodology follows four steps. First of all, the DC and low frequency, small signal behaviour of the MOS transistor has to be reflected in suitable expressions or curves of g_m/I_D , g_{ds}/I_D and intrinsic capacitances versus i , as it will be discussed in Section II. In second place comes the extraction of the models for passive components, presented in Section III. In third place is the modeling of the LC-VCO, where the expressions of phase noise (\mathcal{L}), output voltage V_{out} and VCO flicker corner frequency $f_{c,1/f^3}$ are reordered to make them function of g_m/I_D and i . This step is presented in Section IV. Finally, a design flow is provided; it organizes the necessary computations based on the third step and the decisions constrained by the VCO specifications, while it uses the technological data

collected in the first two steps. This fourth phase is developed in Section V. Sections VI and VII validate this design methodology, contrasting four VCO designs with their correspondent electrical simulations as well as presents measurement results of a specific implementation. Section VIII summarizes the main contributions of this work.

II. MOS TRANSISTOR ANALYSIS

The first step of the methodology, in order to generate a database with its three most important characteristic data, is the correct modeling of the MOST in DC behaviour and in small signal, low frequency of operation. Firstly, the transconductance to current ratio g_m/I_D versus i is used to give an indication of the transistor operation region as well as for calculating MOST dimensions. Secondly, the output conductance g_{ds} is also considered because in nanometer technologies this value is considerably increased, and especially for LC-VCOs it affects the final transconductance value. The ratio g_{ds}/I_D versus i is also applied here [3]. In third place, the MOST intrinsic capacitances are included because, in RF, they substantially modify the circuit behaviour. Considering the quasistatic limit frequency, only C_{ij} , with $ij=\{gs, gd, gb, bs, bd\}$, are included. In order to simplify the modeling, the capacitances are considered to be proportional to the MOST gate area, WL . Hence, each normalized MOST capacitance $C'_{ij} = C_{ij}/(WL)$ is considered equal for all transistors for a specific width range. Because C'_{ij} are also dependent on the inversion zone, the curve C'_{ij} versus i is used. Finally the noise constants have to be known. In this work we have considered these two constants: a) the excess noise factor λ of the white noise [5], and b) the flicker noise constant K_F (or K'_f , if it is divided by the MOS normalized oxide capacitance C'_{ox}).

The g_m/I_D , g_{ds}/I_D and C'_{ij} versus i curves vary only slightly with MOST width and length [3]; this change is only non-negligible in very narrow devices. Fig. 1(b) shows, for a 100 nm nMOS transistor, and four widths $W = \{360 \text{ nm}, 3.6 \mu\text{m}, 36 \mu\text{m}, 360 \mu\text{m}\}$, the simulated results of the curves of g_m/I_D and g_{ds}/I_D versus i . For this technology, the spread of the curves is almost imperceptible. Because of the slight variation in the curves for such a large width range, the methodology presented here succeeds.

In this paper, a semi-empirical MOS model is utilized to describe the MOST because it considers the second and higher order effects of nanometer technologies, and it is easily obtained by extracting MOS characteristics via DC simulation. The use of analytical compact models, such as EKV [5], ACM [6] or PSP [16], have been discarded because the fitting of parameters is very time consuming; however, if properly set, these models can also be used. To acquire the required characteristics curves for this semi-empirical model, a very simple scheme is utilized: transistor gate and drain nodes are connected to

a DC voltage source, while source and bulk nodes are connected either to ground (nMOS transistor) or to the supply voltage (pMOS transistor). Then, the gate voltage V_G is swept extracting I_D , g_m , g_{ds} and C'_{ij} . The drain voltage is set around its expected DC value in the target circuit. To get a very complete dataset the same simulation should be run for a set of widths (for example, the set chosen for Fig. 1), when a fixed transistor length value is used. Otherwise, following the same idea, a small set of lengths should be chosen. Finally, λ and K_F values should be obtained from handling MOST noise data provided by the foundry or estimated from simulations or measurements [17].

III. ANALYSIS OF PASSIVE COMPONENTS

The second step in the methodology is the characterization of passive components. LC-VCOs performance is very much dependent on their non-idealities. Their characterization can be done either by semi-empirical models of library cells provided by the foundry or by electromagnetic solvers such as ASITIC [18] or ADSTMMomentum. Electromagnetic solver has major drawbacks: 1) the need to have the technological data provided by the foundry to obtain accurate descriptions, and 2) the high computational time spent to obtain the solutions.

In this paper, for the sake of efficiency, we utilize passive element cells supplied by the foundry. By means of S-parameter analysis, we obtain their equivalent complex admittance at the working frequency, f_0 .

A. Inductor modeling

In this work, the differential tank inductor is modeled at the oscillation frequency as a network of an equivalent inductor L_{ind} and a parallel parasitic resistor R_{ind} . S-parameter analysis is applied to extract the parameters of the model with the inductor in a differential configuration. In order to obtain a complete database, the analysis has to be done for a large set of inductors. In this work, the best inductor is considered the one with the highest parallel resistance, since it will lead to the lowest required transconductance and hence consumption, as it will be shown in Section IV. Looking for biunivocal relationships between L_{ind} and R_{ind} , computational routines are implemented to find, for a particular inductance value, the nearest best inductor. Figure 4 displays the resulting R_{ind} of sweeping coil conductor width for our standard 90 nm CMOS process and highlights the inductors dataset with the maximum resistances. The data in this plot show that the highest resistances come with the largest inductance values.

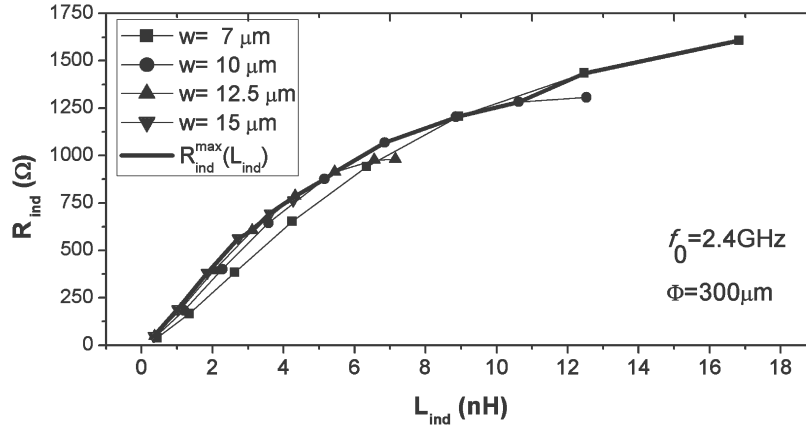


Fig. 4. Parallel resistance versus inductance value L_{ind} for four inductor widths w with a common external diameter of $300 \mu\text{m}$, at $f_0=2.4 \text{ GHz}$. The black line represents the inductors with the highest resistance.

B. Varactor modeling

Varactor parasitic resistance has been usually neglected, especially due to its high value compared with inductor parasitic resistance. However, on-chip coils have improved and it is possible to have a varactor conductance comparable with inductor conductance. Therefore, varactor parasitic resistance extraction by simulations is now necessary, in order to check whether it must be considered in the design.

For the accumulation nMOS varactors used in the design presented in Section VI, the maximum value of g_{var} over the varactor control voltage range is approximately $70 \mu\text{S}$; so varactor conductance can be ignored compared to the conductances of the other VCO components.

IV. VCO MODELING

The LC-VCO topology used in this work is depicted in Fig. 5. It shows a cross-coupled complementary VCO with its LC tank, biased with a pMOS current mirror, which drives the I_{bias} current to the LC-VCO. This pMOS structure is used for its better flicker noise performance with respect to an nMOS one with the same size. Cross-coupled transistors provide the needed negative feedback and a pMOS-nMOS complementary structure increases VCO transconductance while consuming the same quiescent drain current, I_D , with $I_{bias} = 2 \cdot I_D$.

A small-signal model of the LC-VCO of Fig. 5 is displayed in Fig. 6(a) jointly with its simplified model in Fig. 6(b). It comprises the equivalent inductance of the differential inductor L_{ind} and the equivalent capacitance of the varactors C_{var} , both calculated at the oscillation frequency f_0 ; the equivalent parasitic capacitances of the nMOS and pMOS transistors C_{nMOS} and C_{pMOS} ; and the load capacitance

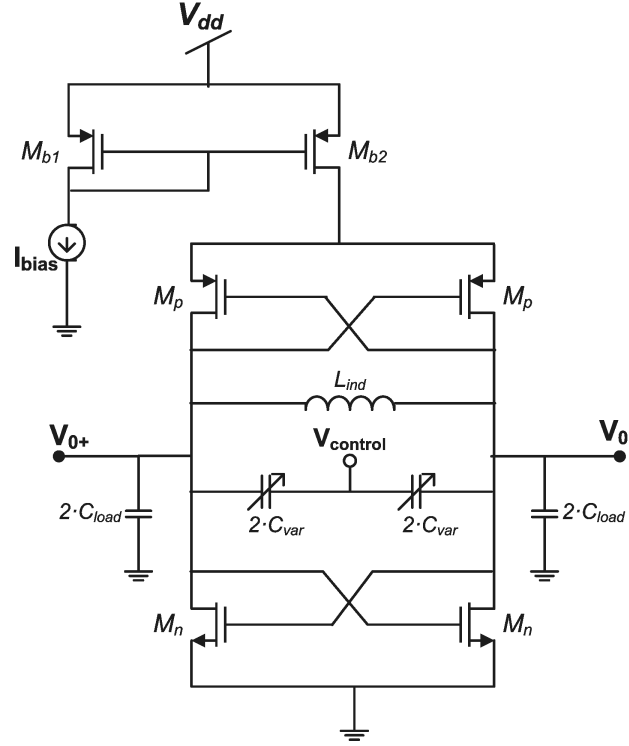


Fig. 5. Cross coupled complementary LC-VCO. C_{load} represents the differential capacitive load at the output of the VCO.

C_{load} . In this paper, the nMOS and pMOS sizing is done in order to match the pMOS and nMOS transconductances, $g_{m,p}$ and $g_{m,n}$, i.e $g_{m,n} = g_{m,p} = g_m$. Considering, respectively, C_{tank} and g_{tank} as the equivalent capacitance and conductance of the VCO tank, the well-known oscillation frequency and oscillation condition expressions are, respectively

$$f_0 = \frac{1}{2\pi\sqrt{L_{ind}C_{tank}}} \quad (1)$$

and

$$g_{tank} \leq \frac{g_{m,p}}{2} + \frac{g_{m,n}}{2} = g_m \quad (2)$$

where

$$C_{tank} = C_{var} + \frac{C_{pMOS} + C_{nMOS}}{2} + C_{load} \quad (3)$$

and

$$g_{tank} = g_{ind} + g_{var} + \frac{g_{ds,p}}{2} + \frac{g_{ds,n}}{2} \quad (4)$$

where $g_{ds,n}$ and $g_{ds,p}$ are the output conductances of the nMOS and pMOS transistors; $g_{ind} = 1/R_{ind}$ and g_{var} are the parasitic conductances of the inductor and varactor, respectively.

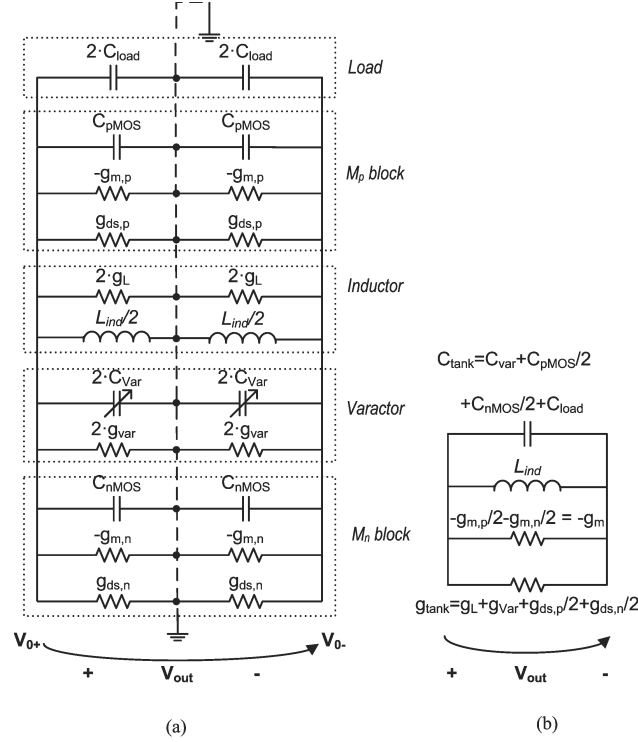


Fig. 6. Small signal LC-VCO model: (a) a complete model and (b) a reduced model. C_{tank} and g_{tank} are, respectively, the VCO equivalent capacitance and conductance.

Considering the five capacitance model of the MOS transistor, the equivalent cross-coupled transistor capacitance C_{MOS} , valid both for the nMOS and pMOS transistors, is

$$C_{MOS} = 4C_{gd} + (C_{gs} + C_{gb} + C_{db} + C_{ds}). \quad (5)$$

Due to the expected technology parameter variations, a safety margin factor k_{osc} -usually called oscillation factor- is utilized in (2) to transform the inequality to

$$g_m = k_{osc} g_{tank} \quad (6)$$

where k_{osc} is generally in the range of 1.5 to 3.

The MOST intrinsic gain A_i , defined as the gain of a common source transistor amplifier loaded by an ideal current source [2], is $A_i = g_m/g_{ds} = (g_m/I_D)/(g_{ds}/I_D)$. Since g_{var} is considered negligible with respect to g_{ind} and g_{ds} , (4) is transformed into

$$\begin{aligned} g_{tank} &\cong g_{ind} + \frac{1}{2} \left(\frac{g_{m,p}}{A_{i,p}} + \frac{g_{m,n}}{A_{i,n}} \right) \\ &= g_{ind} + \frac{g_m}{2} \left(\frac{1}{A_{i,p}} + \frac{1}{A_{i,n}} \right). \end{aligned} \quad (7)$$

Using (6)

$$g_{ind} = g_m \left(\frac{1}{k'_{osc}} - \frac{1}{2A_{i,p}} - \frac{1}{2A_{i,n}} \right) = \frac{g_m}{k'_{osc}}. \quad (8)$$

Then, g_m results finally in

$$g_m = k'_{osc} g_{ind}. \quad (9)$$

The differential output voltage of the tank V_{out} is estimated as in [19]

$$V_{out} = V_{0+} - V_{0-} \cong \frac{4}{\pi} \frac{2I_D}{g_{tank}} = \frac{8}{\pi} \frac{k'_{osc}}{g_m/I_D}. \quad (10)$$

A. Phase noise model

Phase noise \mathcal{L} is a fundamental characteristic of a VCO that describes its spectral purity around its oscillation frequency f_0 [20]. Considering a frequency offset Δf around f_0 , three asymptotic zones can be defined [21]. Very near f_0 , \mathcal{L} decreases proportionally to $1/f^3$ and it is directly related to the flicker noise of MOS transistors. Then, a spectrum zone inversely proportional to f^2 appears, mainly caused by the white noise of VCO elements. Finally, far from f_0 , there is a flat zone, the VCO floor noise, where the external noise sources dominate. Generally it is the $1/f^2$ zone where the VCO phase noise is specified. The asymptotic limits of the three regions can be found making equal the expressions for two adjacent zones and solving for f . Particularly, the flicker corner frequency $f_{c,1/f^3}$ is the VCO parameter that defines the lower limit of the $1/f^2$ zone.

To visualize and fully exploit the phase noise-current consumption trade-off, an analytical model for phase noise valid for all the inversion regions is used in this work by means of expressing the phase noise equations as functions of the g_m/I_D ratio. The initial expressions of this phase noise model were presented by Hajimiri in [20]. This is a linear time variant model, with compact equations, very suitable for our methodology. In the $1/f^2$ region of the spectrum (see Appendix A for derivation) the phase noise expression is

$$\mathcal{L}_{1/f^2}(\Delta f) = 10 \log \left(k_B T \frac{\pi^2}{64} \frac{1}{Q^2} \frac{g_m}{I_D} \frac{1}{I_D} \frac{f_0^2}{\Delta f^2} \lambda \right) \quad (11)$$

where $\lambda = \frac{\gamma}{\alpha_{eq}} + \frac{1}{k_{osc}}$, γ is the excess noise factor, k_B is the Boltzmann constant, T is the absolute temperature, f_0 is the oscillation frequency, Δf is the frequency offset and α_{eq} is defined as

$$\alpha_{eq} = \left(\frac{g_{d0,n}}{g_{m,n}} + \frac{g_{d0,p}}{g_{m,p}} \right)^{-1} \quad (12)$$

with $g_{d0,n}$ and $g_{d0,p}$ the zero-bias (i.e. $V_{DS} = 0$) drain conductances g_{ds} , for nMOS and pMOS respectively.

Tank quality factor, Q , is calculated as

$$Q = \frac{1}{2\pi f_0 L_{ind} g_{tank}}. \quad (13)$$

Similarly, we derive a phase noise expression for the $1/f^3$ zone (see Appendix B for derivation):

$$\mathcal{L}_{1/f^3}(\Delta f) = 10 \log \left(\frac{\Gamma_{av}^2 \pi^2}{8 \cdot 64} \left(\frac{K'_{F,n}}{W_n L} + \frac{K'_{F,p}}{W_p L} \right) \frac{1}{Q^2} \left(\frac{g_m}{I_D} \right)^2 \frac{f_0^2}{\Delta f^3} \right) \quad (14)$$

where $K'_{F,n}$ and $K'_{F,p}$ are the nMOS and pMOS normalized flicker noise constants, and Γ_{av} is the average value of the impulse sensitivity function Γ defined in [20].

The LC-VCO flicker corner frequency $f_{c,1/f^3}$ is expressed as a function of the transistor corner frequency f_c . It is approximately (see Appendix D):

$$f_{c,1/f^3} = k_0 f_{c,eq} \cong k_0 \frac{K_F \alpha_{eq} g_m}{4k_B T \gamma} \frac{1}{I_D} \frac{1}{L^2} \quad (15)$$

where k_0 and $f_{1/c,eq}$ are defined in Appendix D.

The data obtained from previously designed LC-VCO allow us to estimate the Γ_{av} coefficient on which k_0 depends. For these circuits, $\Gamma_{av} \leq 0.4$ and $k_0 \leq 0.16$. It means that $f_{c,1/f^3}$ is generally much smaller than f_c . Γ_{av} is dramatically reduced if the VCO layout is highly symmetrical [20] and if the output signal is a low distorted sinusoidal waveform.

The equations formulated before, particularly (11) and (14), help us to quantitatively visualize the compromises between phase noise and current consumption. Considering a fixed g_m , imposed by (9), when g_m/I_D rises, i.e when moving towards weak inversion, I_D decreases in the same proportion. Rising g_m/I_D and reducing I_D leads to a phase noise increment in the $1/f^2$ and $1/f^3$ spectrum regions. The design methodology, presented in the following section, explores these trade-offs, making it possible to optimize consumption while achieving the specified phase noise level.

V. PROPOSED DESIGN METHODOLOGY

The methodology proposed hereafter intends to give a simple way to size the LC-VCO components and to visualize graphically the trade-offs inherent in the design. The flow diagram of the method is represented in Fig. 7, and it is organized in the following steps:

Step 1: Start fixing a set of initial parameters and limits: minimum transistor channel length L_{min} , safety margin factor k_{osc} , maximum equivalent inductance $L_{ind,max}$, minimum varactor capacitance $C_{var,min}$ and C_{load} . Next, set the VCO specifications: oscillation frequency f_0 , maximum current $I_{D,max}$, maximum phase noise in the white noise zone $\mathcal{L}_{1/f^2,max}$ at an offset Δf and minimum output voltage $V_{out,min}$.

Step 2: Pick a pair of values of inductor L_{ind} and g_m/I_D ratio, from the technological database of inductors and transistors, which is assumed previously collected.

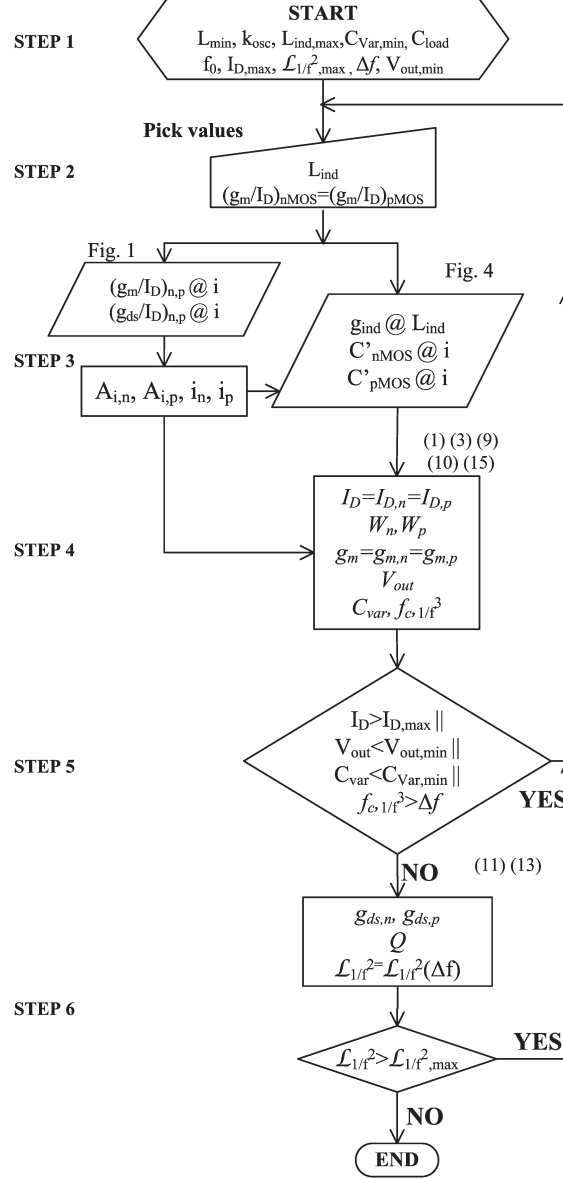


Fig. 7. Flow diagram of the proposed VCO design methodology.

Step 3: From the inductor database, derive the g_{ind} of that inductor. Obtain the normalized currents of nMOS and pMOS, i_n and i_p , as well as g_{ds}/I_D , from the picked g_m/I_D and the characteristic curves (g_m/I_D vs. i) and (g_{ds}/I_D vs. i). Calculate the intrinsic gains $A_{i,n}$ and $A_{i,p}$ and then deduce k'_{osc} . Extract the transistors equivalent capacitance from C'_{nMOS} vs. i and C'_{pMOS} vs. i tables.

Step 4: Deduce g_m from (9). With g_m and g_m/I_D calculate the drain current I_D , and with (10) compute V_{out} . Then, calculate the transistors widths W_n and W_p from I_D and i_n and i_p and compute C_{nMOS} and

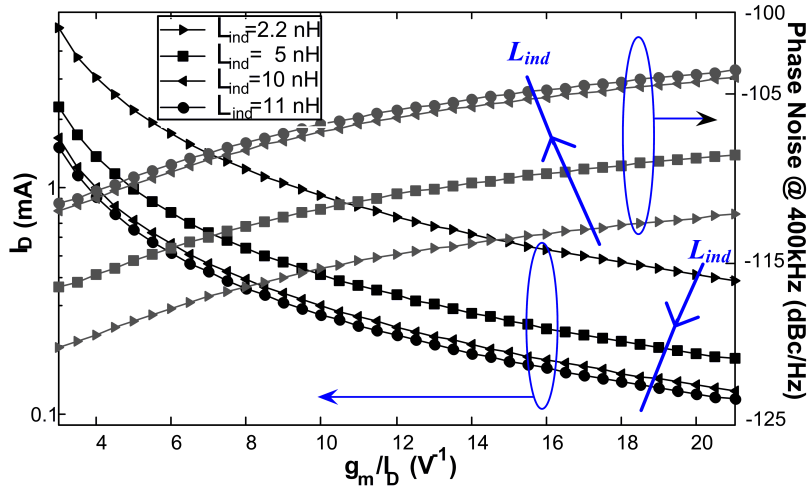


Fig. 8. Drain current I_D (left axis) and phase noise in the $1/f^2$ region (right axis) versus g_m/I_D for four inductance values L_{ind} .

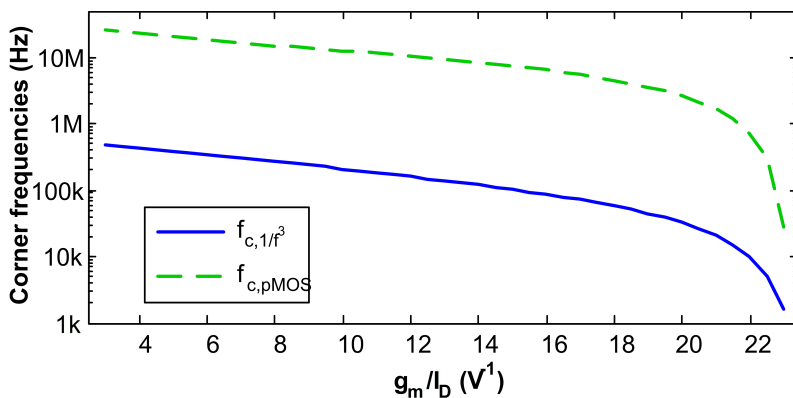


Fig. 9. Corner frequencies $f_{1/f}$ and f_{1/f^3} .

C_{pMOS} . With (1) and (3), solve for C_{var} . Calculate $f_{c,1/f^3}$ using (15).

Step 5: If $I_D > I_{D,max}$ or $V_{out} < V_{out,min}$ or $C_{var} < C_{var,min}$ or $f_{c,1/f^3} > \Delta f$, return to *Step 2* and change one or both of the values chosen, otherwise continue.

Step 6: Compute $g_{ds,n}$ and $g_{ds,p}$ and hence, Q with (13). Calculate the phase noise \mathcal{L}_{1/f^2} using (11) at the frequency offset Δf . If it surpasses $\mathcal{L}_{1/f^2,max}$, return to *Step 2*, otherwise the design is finished.

TABLE I
CHARACTERISTICS OF THE CHOSEN DESIGNS IN SI, MI AND WI FOR $f_0=2.4$ GHz

Parameter	P1 (SI)		P2 (MI)		P3 (WI)		P4 (MI)		
	Computed	SpectreRF	Computed	SpectreRF	Computed	SpectreRF	Computed	SpectreRF	Fabricated
I_D (μm)	315	315	215	215	130	130	155	155	165
W_n (μm)	8.8	8.8	37	37	76.2	76.2	45	45	10×4.6
W_p (μm)	23.6	23.6	50.1	50.1	78.6	78.6	53	53	10×5.4
L_{ind} (nH)	8	8	5.5	5.5	10.7	10.7	10.1	10.1	10
C_{var} (fF)	255	255	537	537	60.3	60.3	165	165	175
g_m/I_D (V^{-1})	11.2	9.9	16.1	14.5	19.6	19.3	17.7	17.4	17.6
V_{out} (V)	1.3	1.3	0.77	0.96	0.62	0.74	0.7	0.87	0.8
\mathcal{L} (dBc/Hz@400kHz)	-107.3	-110	-109.4	-110.2	-104	-103.2	-104.8	-104.6	-104.3
$f_T/10$ (GHz)	8.6	8.7	3	1.9	1.1	0.9	1.7	2	1.8
$f_{c,1}/f^3$ (kHz)	179	210	87.3	58	38.2	65	63.2	67	72

A. Design maps

We implemented the design flow in a set of computational routines to graphically study the behavior of the phase noise, the current consumption and the flicker corner frequency when g_m/I_D and L_{ind} change. The 90 nm CMOS technology of the example of Section VI is used.

The relation between I_D and g_m/I_D , for various inductor values, is plotted in Fig. 8 (left axis). We see that I_D decreases if: (a) g_m/I_D rises (i.e. when moving towards weak inversion), and b) if the inductance value increases. The point (a) is explained because g_{ind} is fixed for each L_{ind} so, from (9), g_m is fixed. Thus, when g_m/I_D increases necessarily I_D decreases. The point (b) is deduced from Fig. 4, where an increment in the inductor value means an increment in its parallel resistance. This implies a reduction in g_{ind} , and thus in g_m , due to (9).

Phase noise in the white noise region versus g_m/I_D , considering again four inductor values, is also depicted in Fig. 8 (right axis). Phase noise increases when working in moderate and weak inversion because it is proportional to g_m/I_D as states (11). It also increases for low inductance values, because they have lower R_{ind} , which, due to (13), cause low tank quality factors Q ; finally Q is inversely proportional to \mathcal{L}_1/f^2 .

Figure 9 plots the MOS corner frequency f_c and the flicker corner frequency $f_{c,1}/f^3$ as functions of g_m/I_D , from (30) and (15), with $\Gamma_{av} = 0.2$ (as a sinusoidal V_{out} is considered), $K'_{F,n} = 3.2 \cdot 10^{-23} JHz$ and $K'_{F,p} = 1.3 \cdot 10^{-22} JHz$ [17]. Because MOST corner frequency decreases when moving towards weak

inversion, the flicker corner also decreases in weak inversion. The $f_{c,1}/f^3$ reduction is a good consequence of working in WI and MI.

Finally, the design map of Fig. 10 shows the phase noise behaviour when jointly vary g_m/I_D and L_{ind} . Figures 8 to 10 show the potential of our methodology, as they easily highlight the trade-offs of the VCO characteristics in the different MOST inversion regions.

VI. APPLICATION EXAMPLES

In this section four 2.4 GHz LC-VCOs designed in a 90 nm CMOS technology are presented. The design flow of Section V was followed, performing previously the phase of extracting the technology database. The data of four examples are picked from Fig. 10, where are referred as *P1*, *P2*, *P3* and *P4*. A drain current constraint of $I_{D,max} \leq 400\mu A$ was set and it is shown in the shadowed area of the figure. The phase noise of these design points is limited to $\mathcal{L} < -100\text{dBc/Hz}$ at 400kHz. For the computations, $\Gamma_{av} = 0.2$ and $k_0 = 0.04$, as the V_{out} is supposed very sinusoidal.

In order to verify the validity of the all-inversion-region methodology, each design belongs to a different inversion region. *P1* is in the limits of strong inversion, *P3* is in the limits of weak inversion and, *P2* and *P4* are in moderate inversion. Table I compares the VCO parameters obtained by the design flow formulas with the derived ones through SpectreRF analysis. Let us consider the design points *P1* and *P2*; although they are very similar in terms of phase noise, *P2* consumes 30% less than *P1* and has also a smaller inductor. However *P2* is in the quasistatic-limit frequency whereas *P1* is far beyond it. Analyzing designs *P3* and *P4*, we observe that the first one consumes 16% less and has a phase noise only 1dB higher than the second, but it is far below the quasistatic-limit frequency, therefore it is not recommendable to choose *P3* when $f_0 = 2.4$ GHz. Figure 11 shows the phase noise of the four designs versus the frequency offset Δf , obtained from SpectreRF simulations.

Finally, design *P4* is chosen to validate experimentally the methodology. This point allows us to play with the bias current, to visualize its effect in the phase noise and to experimentally check the relationships discussed in previous sections. Final VCO component sizes and simulated characteristics are listed in the last column of Table I. As the output of the fabricated VCO has an on-chip differential-pair buffer to fix C_{load} , minor components resizing were needed to tune the desired oscillation frequency, condition frequency and phase noise.

The layout and the microphotograph of the fabricated chip is depicted in Fig. 12. The final design occupies an area of $500\mu m \times 350\mu m$.

VII. EXPERIMENTAL RESULTS

The characteristics of the VCO were measured on die using a microprobe station. To measure its spectrum and phase noise the Agilent Spectrum Analyzer E4440A was employed.

A set of phase noise measurements has been done to the fabricated chip. Unfortunately, the buffer does not work properly and interferes with the VCO behaviour, so necessary the measurements were done with the output buffer switched off. Figure 13 displays the variation of f_0 with control voltage $V_{control}$. In the inset of Fig. 13, it is shown the VCO spectrum for a $V_{control} = 0V$. The minimum bias current where a clean spectrum without interferers is obtained was $I_D=220 \mu A$. For this current, the phase noise versus the offset frequency, with the carrier at 2.16 GHz ($V_{control} = 0V$) is shown in Fig. 14. The phase noise at 400 kHz from the carrier is -106.2 dBc/Hz. The measured flicker corner frequency $f_{c,1/f^3}$ is 203 kHz, whereas the simulated flicker corner frequency, shown in Table I, is 72 kHz. This rise in $f_{c,1/f^3}$ respect to the simulated data of *P4*, happens because V_{out} is distorted when the buffer is turned off. Γ_{av} rises to approximately 0.4, and the computed $f_{c,1/f^3}$ is 257 kHz, very near the measured data.

The current I_D was also swept to 310 μA and a set of phase noise measurements at 400 kHz from the carrier were performed (forty measurements of \mathcal{L} were taken for each current value), as depicted in Fig. 15, considering again a carrier frequency around 2.16 GHz. The theoretical curve of (11) is superimposed with experimental data, considering $\alpha = 0.65$, $k_{osc} = 3$ and $\gamma = 0.55$. The fitted model is extended up to the nominal I_D current of 165 μA , obtaining an extrapolated phase noise value of -104.6 dBc/Hz. Good agreement exists between model, simulations and measurements.

The minimum measured I_D where the VCO works, for three samples' average, is 62.5 μA ; 13.5% higher than the expected value of 52 μA obtained from the design flow. The output voltage when the buffer is switched on, for $I_{bias}=440 \mu A$ is 630 mV, a bit lower than expected.

Table II compares the performance of the designed LC-VCO in moderate inversion with that of some prior works, where the well known figure-of-merit (FoM) of the VCO defined in [22] is used. Our VCO is well positioned considering other similar designs, as only the second one has a better FoM. However the later occupies more area than our design because it uses two on-chip inductors, which increases the tank quality factor and reduces the phase noise.

VIII. CONCLUSIONS

In this paper, an RF LC-VCO design methodology for nanometer technologies based on the g_m/I_D technique has been presented. The methodology proposed enables a considerable design time reduction

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED LC-VCOs.

VCO	Tech. (nm)	f_0 (GHz)	Δf (MHz)	Power (mW)	\mathcal{L} (dBc/Hz)	FoM (dB)
[23]	180	2.2	1	5.17	-119	179
[13]	180	2.645	0.4	0.63	-106.4	184.8
[15]	180	2.5	1	1.2	-103.7	171
[22]	180	1.57	1	3.06	-120	180
This work	90	2.16	0.4	0.53	-106.2	183.6

as little re-design is needed. It also shows the VCO trade-offs, providing beforehand a global view of the VCO behaviour when adjusting certain component parameters during the design.

MOST, inductor and varactor data were extracted from SpectreRF simulations to accurately and quickly model these components and include that data in the design flow. VCO modeling equations were modified to introduce I_D and the MOS variable g_m/I_D , in order to easily see the compromises of working in different MOS inversion regions. Specially, Hajimiri phase noise model equations were re-ordered to express them in terms of g_m/I_D . Plots of several variables involved in the VCO design were shown and compromises with the inversion region or the selection of the inductor were highlighted. It has been shown that designing in moderate and weak inversion leads to reduced current while phase noise is increased; on the other hand an increment of the inductor value (and hence a increment in its equivalent parallel resistance) contributes to an improvement in the VCO spectral purity. Four designs were simulated to validate the method. Finally, an application example was implemented to show the usefulness of the method, as well as to prove the validity of the phase noise model. Phase noise results from the calculations of our design routines, electrical simulations and measurements are in agreement.

APPENDIX

DEDUCTION OF PHASE NOISE EXPRESSIONS

A. Expression of phase noise of a LC-VCO in the $1/f^2$ spectrum region.

The expression of phase noise for an arbitrary oscillator in the $1/f^2$ region of the phase noise spectrum expressed by Hajimiri in [20] is

$$\mathcal{L}_{1/f^2}(\Delta f) = 10 \log \left(\frac{\Gamma_{rms}^2 \overline{i_n^2 / \Delta f}}{q_{max}^2 2\Delta f^2} \right) \quad (16)$$

where Γ_{rms} is the rms value of the impulse sensitivity function ISF defined in [20], q_{max} is the maximum charge displacement across the capacitor in the output nodes, Δf is the frequency offset respect to the oscillation frequency f_0 , and $\overline{i_n^2/\Delta f}$ is the power spectral density of the noise source considered at the output nodes.

To evaluate the phase noise expression for our LC-VCO, let's obtain the expressions of each term in (16). Firstly we calculate the most important VCO white noise sources. For simplicity we will consider that no correlation exists between them. Superposition will be applied when substituting their expressions in (16).

The general expression of MOS white noise is [4]

$$\overline{\frac{i_{w,MOS}^2}{\Delta f}} = 4k_B T \gamma g_{do} = 4k_B T \frac{\gamma}{\alpha} g_m. \quad (17)$$

The equivalent power spectral density of the two nMOS and two pMOS is [24]

$$\overline{\frac{i_{w,MOS_{eq}}^2}{\Delta f}} = \frac{1}{2} \left(\overline{\frac{i_{w,n}^2}{\Delta f}} + \overline{\frac{i_{w,p}^2}{\Delta f}} \right) \quad (18)$$

Substituting (17) in (18)

$$\begin{aligned} \overline{\frac{i_{w,MOS_{eq}}^2}{\Delta f}} &\cong 4k_B T \gamma g_m \frac{1}{2} \left(\frac{1}{\alpha_n} + \frac{1}{\alpha_p} \right) \\ &= 4k_B T \frac{\gamma}{\alpha_{eq}}. \end{aligned} \quad (19)$$

The white noise of each cross-coupled transistor block due to its equivalent drain-source conductance is [4] [25]:

$$\overline{\frac{i_{w,g_{ds}}^2}{\Delta f}} = 4k_B T \frac{g_{ds}}{2} = 4k_B T \frac{g_m}{2A_i}. \quad (20)$$

Considering both nMOS and pMOS equivalent conductances,

$$\overline{\frac{i_{w,g_{ds}^{eq}}^2}{\Delta f}} = 4k_B T \frac{g_m}{2} \left(\frac{1}{A_{i,n}} + \frac{1}{A_{i,p}} \right). \quad (21)$$

The white noise of the inductor parallel resistance $R_{ind} = 1/g_{ind}$ is, applying (9),

$$\overline{\frac{i_{w,L_{ind}}^2}{\Delta f}} = 4k_B T g_{ind} = 4k_B T \frac{g_m}{k'_{osc}}. \quad (22)$$

The white noise power spectral density of the varactor has been neglected for this deduction as generally $g_{var} \ll g_{ind}$.

The equivalent white noise power spectral density of the LC-VCO is, from equations, (8), (19), (21) and (22):

$$\begin{aligned}\overline{\frac{i_{w,VCO}^2}{\Delta f}} &= 4k_B T g_m \left(\frac{\gamma}{\alpha_{eq}} + \frac{1}{k'_{osc}} + \frac{1}{2A_{i,n}} + \frac{1}{2A_{i,p}} \right) \\ &= 4k_B T g_m \left(\frac{\gamma}{\alpha_{eq}} + \frac{1}{k'_{osc}} \right) = 4k_B T g_m \lambda.\end{aligned}\quad (23)$$

Besides, $q_{max} = C_{tank} V_{out}$, where C_{tank} is the equivalent capacitance at the output nodes, expressed as:

$$C_{tank} = \frac{1}{4\pi^2 f_0^2 L_{ind}} = \frac{Q}{2\pi f_0 R_{tank}} \quad (24)$$

Then, from (10) and (24), q_{max} is

$$q_{max} = \frac{8}{\pi} \frac{I_D Q}{(2\pi f_0)} = \frac{2I_D R_{tank}}{(\pi^3) f_0^2 L_{ind}}. \quad (25)$$

Finally, substituting (23) and (25) in (16), considering $\Gamma_{rms} \approx 0.5$ due to the symmetry characteristics of this VCO, and reordering the terms, we obtain

$$\mathcal{L}_{1/f^2}(\Delta f) = 10 \log \left(k_B T \frac{\pi^2}{8^2} \lambda \frac{1}{Q^2} \frac{g_m}{I_D} \frac{1}{I_D} \frac{f_0^2}{\Delta f^2} \right) \quad (26)$$

B. Expression of phase noise of a LC-VCO in the $1/f^3$ spectrum region.

From [20], the following is the general expression of the phase noise in the $1/f^3$ portion of the phase noise spectrum

$$\mathcal{L}(\Delta f)_{1/f^3} = 10 \log \left(\frac{\Gamma_{av}^2}{8q_{max}^2} \frac{\overline{i_{1/f}^2}/\Delta f}{\Delta f^2} \right) \quad (27)$$

Considering that only the MOS transistors injects flicker noise, the total power spectral density of the flicker noise sources is

$$\begin{aligned}\overline{\frac{i_{1/f}^2}{\Delta f}} &= \frac{1}{2} \left(\overline{\frac{i_{1/f,n}^2}{\Delta f}} + \overline{\frac{i_{1/f,p}^2}{\Delta f}} \right) \\ &= \frac{1}{2} \left(\frac{K'_{F,n} g_m^2}{W_n L} + \frac{K'_{F,p} g_m^2}{W_p L} \right) \frac{1}{f}\end{aligned}\quad (28)$$

Equations (27) together with (25) and (28) results in the following expression for phase noise in the $1/f^3$ zone in terms of g_m/I_D :

$$\begin{aligned}\mathcal{L}_{1/f^3}(\Delta f) &= 10 \log \left(\frac{\Gamma_{av}^2}{8} \frac{\pi^2}{8^2} \frac{1}{L} \left(\frac{K'_{F,n}}{W_n} + \frac{K'_{F,p}}{W_p} \right) \right. \\ &\quad \left. \frac{1}{Q^2} \left(\frac{g_m}{I_D} \right)^2 \frac{f_0^2}{\Delta f^3} \right)\end{aligned}\quad (29)$$

C. Corner frequency of MOST expressed as a function of g_m/I_D and i .

The corner frequency of a MOST f_c is obtained equaling the expressions of white noise and flicker noise, resulting in:

$$f_c = \frac{K'_F}{4k_B T} \frac{\alpha g_m}{\gamma I_D} \frac{I_D}{W/L} \frac{1}{L^2} = \frac{K'_F}{4k_B T} \frac{\alpha g_m}{\gamma I_D} i \frac{1}{L^2} \quad (30)$$

D. Flicker corner frequency of the VCO phase noise expressed as a function of g_m/I_D and i .

The flicker corner frequency of the VCO phase noise, obtained when making equal the phase noise expressions at white noise and flicker zones -(26) and (29), respectively-, results

$$f_{c,1/f^3} = k_0 \left(\frac{\overline{i_{w,n}^2} f_{c,n} + \overline{i_{w,p}^2} f_{c,p}}{\overline{i_{w,n}^2} + \overline{i_{w,p}^2}} \right) = k_0 f_{c,eq}. \quad (31)$$

where $k_0 = \left(\frac{\Gamma_{av}}{2\Gamma_{rms}} \right)^2$.

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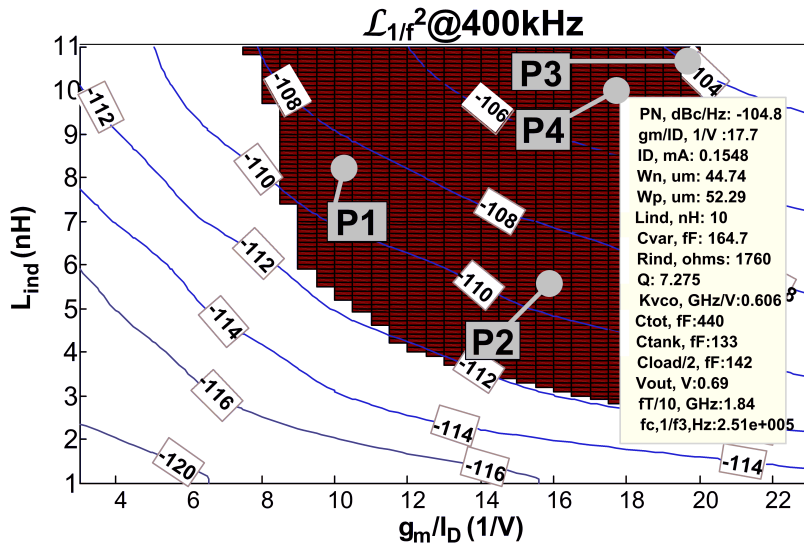


Fig. 10. \mathcal{L}_{1/f^2} in dBc/Hz mapped versus g_m/I_D and L_{ind} . The text-box displays the characteristics and parameters of the LC-VCO associated with the picked point (P4 in this example).

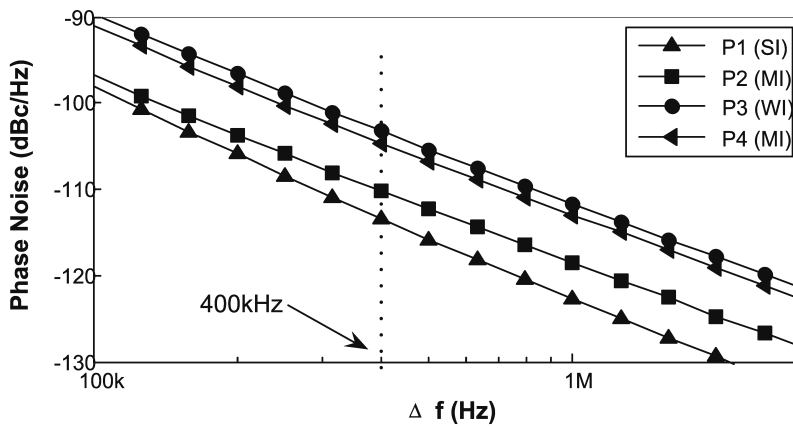


Fig. 11. Phase noise SpectreRF simulations for designs $P1$, $P2$, $P3$ and $P4$.

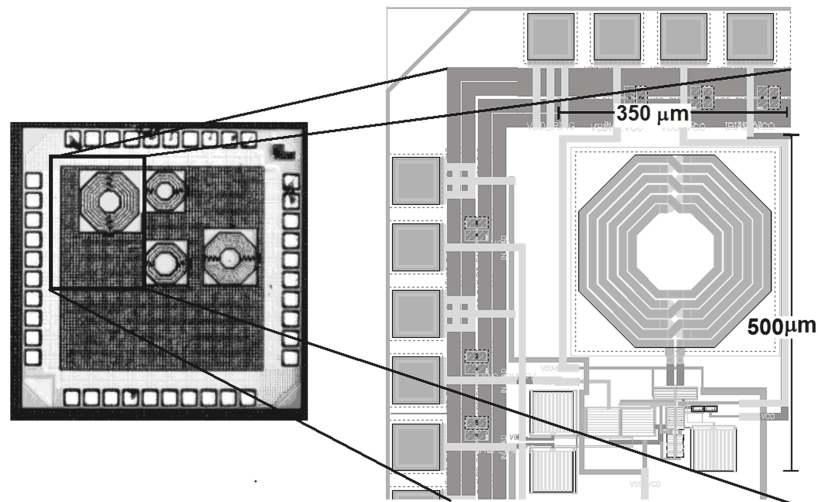


Fig. 12. Layout and microphotograph of the fabricated VCO.

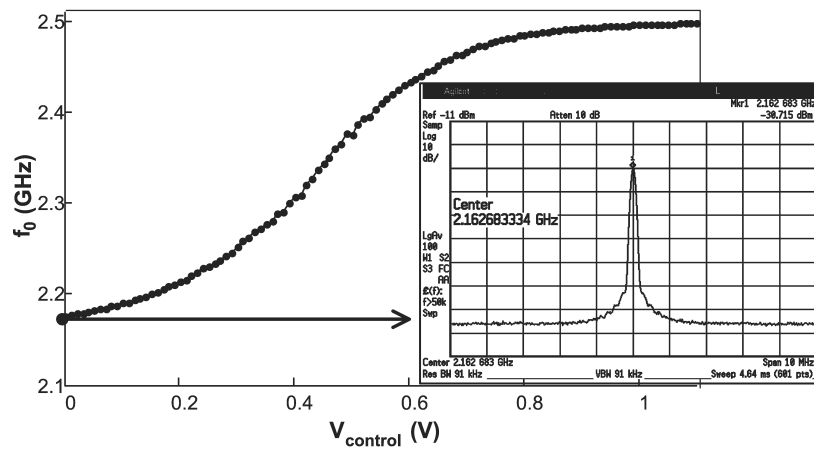


Fig. 13. Carrier frequency f_0 versus $V_{control}$ and output spectrum (inset) at $V_{control} = 0$ with the buffer switched off.

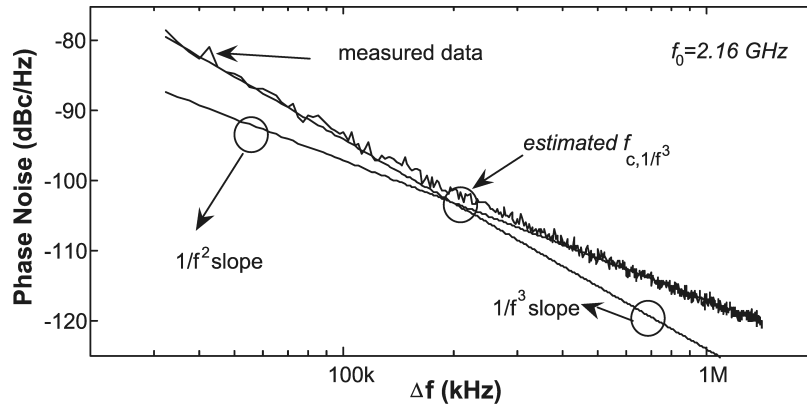


Fig. 14. \mathcal{L} with the VCO biased with $I_{bias} = 2 \cdot I_D = 440\mu A$ and $f_0 = 2.1639GHz$ (buffer switched off). $1/f^2$ and $1/f^3$ slopes are shown as well as the estimated flicker corner $f_{c,1/f^3}$.

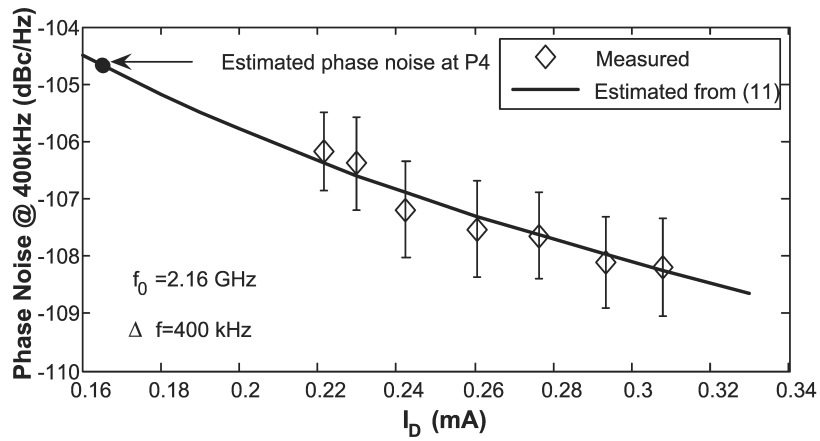


Fig. 15. Phase noise measured and estimated by (11) sweeping only I_D .