Two-Phase RTD-CMOS Pipelined Circuits

Juan Núñez, María J. Avedillo and José M. Quintana

Abstract— **MOBILE networks can be operated in a gate-level pipelined fashion (nanopipeline) allowing high throught-output. RTD-based MOBILE nanopipelined circuits have been reported using different clock schemes including a four phase strategy and a single phase clock scheme. In particular, it has been shown significant power advantages of single phase RTD-CMOS MOBILE circuits over pure CMOS. This paper compares RTD-CMOS realizations using a single clock and a novel two-phase clock solution. Significant superior robustness and performance in terms of power and area are obtained for the two phase implementations.**

Index Terms— **Resonant tunneling diode, Nano-pipeline, Emerging technologies, Logic circuits, Power efficiency.**

I. INTRODUCTION

Resonant Tunneling Diodes (RTD) exhibit a Negative Differential Resistance (NDR) characteristic and many circuits taking advantage of it have been reported, covering different applications (memories, logic, oscillators, A/D converters) and with different goals (high speed, low power) [1] [2]. In particular, their NDR current-voltage characteristic can be exploited in logic design to implement logic networks in which each gate-level is a pipelined stage (nanopipeline) allowing very high through-output. Currently, the realization of tunnel diodes in silicon is a very active research area where progresses are expected. In fact, it has been suggested that the addition of RTDs to CMOS technology (RTD-CMOS) could extend its life and several works have reported advantages of incorporating RTDs to CMOS [3],[4],[5].

Logic circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) [6] which exploits the NDR of their *I-V* characteristic (Fig. 1a). The MOBILE in Fig. 1b is an edge-triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage, V_{CK}. When V_{CK} is low, both RTDs are in the on-state and the circuit is monostable. Increasing to an appropriate maximum value ensures that only the device with the lowest peak current switches from the on-state to the off-state. Output is high if the driver RTD switches and it is low if the load does. Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. Rising and falling edge-triggered inverter
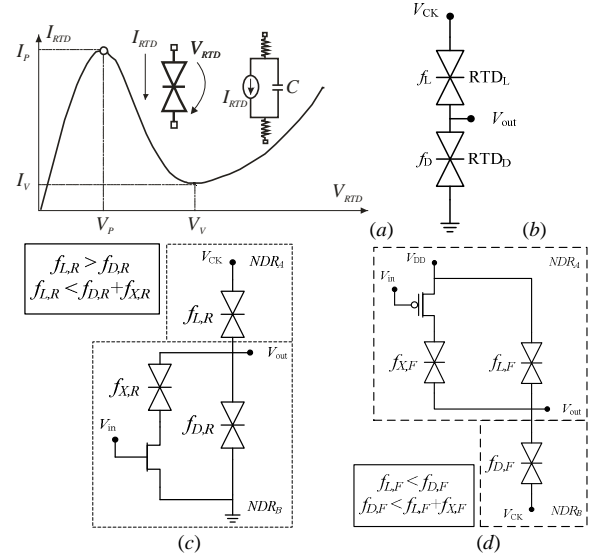
Fig 1. RTD MOBILE circuits. (*a*) RTD *I-V* characteristic and symbol and simulation model. (*b*) Basic MOBILE. (*c*) Rising edge-triggered MOBILE inverter. (*d*) Falling edge-triggered MOBILE inverter.

MOBILEs are shown in Fig. 1c and 1d. The peak current of the driver (load) RTD is modulated using the external input signal V_{in}. Replacing the single transistors in Fig. 1c and 1d by a transistor network, other logic functions are implemented.

Rising (falling) edge-triggered MOBILE logic gates evaluate the inputs with the rising (falling) edge of the bias voltage and hold the logic level of the output while the bias voltage is high (low), even though the inputs change (self-latching operation). The output returns to zero (to one) with the falling (rising) edge of the clock until the next evaluation. Different interconection schemes for fine-grained pipelined MOBILE circuits without latches have been proposed. Originally cascaded rising edge-triggered MOBILE gates were operated in a pipelined fashion using a four-phase overlapping clocking scheme, which implies restrictive timing constraints in clock distribution. Thus, simpler clock schemes are investigated.

A network of MOBILE-based gates can be operated with a single clocked bias signal if rising edge-triggered gates and falling edge-triggered gates are alternated with inter-stage elements to keep the output of each MOBILE stage until it has been evaluated by the next one [7]. Figure 2a depicts chained MOBILE elements implemented with the single-phase architecture. Single-phase RTD-CMOS pipelined architectures have been compared to conventional CMOS fine-grained pipelines [5] and shown to be significantly more power efficient with power ratios over 2 in most of the reported comparison experiments. However, they exhibit poor design robustness.

Very recently a two-phase clock scheme has been proposed to operate MOBILE gate networks [8]. Only simulation results

using transistor circuits to emulate RTDs have been shown to validate the proposal. This paper shows, for the first time, experimental results of MOBILE circuits operating with this interconnection scheme, applies it to RTD-CMOS MOBILE circuits and carries out different experiments to compare RTD-CMOS single-phase and two-phase architectures in terms of design robustness. The study uses PTM 32nm transistor model. The RTD has been modeled using a voltage-dependent current source and a capacitor in parallel (Fig. 1a) and technology parameters from an experimentally validated Si-Ge RTD [9] with peak current density j_p=218KA/cm^2 and capacitor C=6fF/μm^2. Transistor lengths have been set to the minimum value associated to the technology whereas their widths are large enough to allow their operation as switches. RTD* areas (Fig. 1c and 1d) are constrained such that $f_{D,R}=f_{X,R}$ and $f_{L,R}=K \cdot f_{X,R}$ for rising edge-triggered and $f_{L,F}= f_{X,F}$ and $f_{D,F}= K \cdot f_{X,F}$ for falling ones, where K depends on the type of gate.

This paper is organized as follows: in Section II, two-single phase scheme is described and experimentally validated and we analyse its advantages over the single-phase solution. In Section III we present RTD-CMOS adders which have been designed and evaluated and describe the obtained results.

II. TWO-PHASE VS SINGLE-PHASE INTERCONNECTION SCHEMES

The two phase gate-level pipelined MOBILE architecture applies a two-phase overlaping clock scheme as shown in Fig. 2b. Unlike the single-phase one, direct connection in addition to inverting and non-inverting interstage elements is also possible. Main advantages of two-phase scheme with respect to single-phase one are:

1. Only rising-edge triggered MOBILEs are used avoiding p-type transistors. This translates in smaller gate widths and so smaller parasitic improving circuit performance.

2. Larger design robustness. In particular, it exhibits larger clock skew tolerance. When using a single-phase clock scheme, the clock edge-triggering evaluation of one stage causes the return to-reset of its previous ones. Any small skew of the two clocks could result in a stage evaluating the reset value instead of the actual data. For this reason, the inter-stage element is introduced, but still the allowable skew is limited to the inter-stage delay. In the two-phase scheme the clocks of successive stages overlap. The skew tolerance does not rely only in the inter-stage delay which can even being eliminated.

Two-phase clocked chains of MOBILE inverters have been designed and fabricated. These structures have been implemented with MOS-NDR devices (circuits made up of transistors that emulate the NDR I-V characteristic [9]) in a 1.2V/90nm CMOS technology. Figure 3a depicts the block diagram of one of the fabricated circuits, whereas Fig. 3b depicts the measured waveform of V_{OUT} when a sequence alternating 0's and 1's is applied to the ten-stage pipeline. For this circuit, both V_{CK} and V_{IN} have been generated on-chip so that the input frequency is half that of the clock and, thus, V_{OUT} is a periodical signal of the same frequency of the input.

Different two-phase RTD-CMOS pipelined MOBILE circuits have been designed and validated through extensive simulation
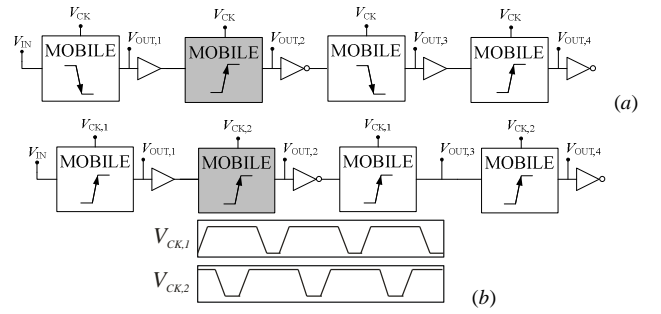
* Minimum RTD area considered is 100nm x 100nm.

Fig 2. (*a*) Block diagram of a single-phase clock scheme interconnection of four MOBILE stages. (*b*) Block diagram and clock waveforms of the two-phase counterpart.
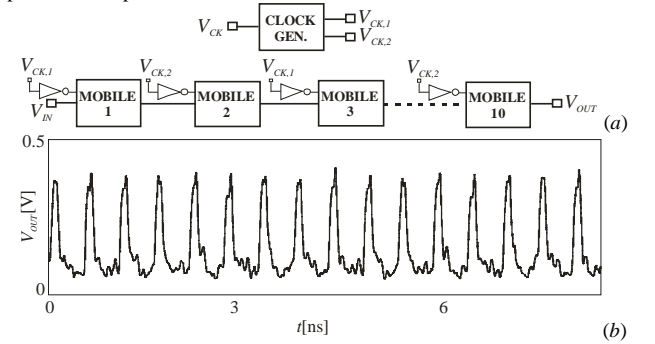

Fig 3. (*a*) Block diagram of the fabricated two-phase chain of inverters. (*b*) Measured waveforms.

and experiments have been carried out to quantitatively evaluate the design robustness improvement achieved by the two-phase clock scheme.

First, simulations to measure clock skew tolerance have been done. For this, chains of pipelined MOBILE inverters operated both with a single clock and with a two-phase scheme have been simulated. A different clock source has been used for each MOBILE stage in the pipeline and a variable controlling the position of its edges have been associated to each of them. Monte Carlo simulations applying uniform distributions to the clock variables within the interval [-*abs*, *abs*] have been carried out. Operating frequencies for different values of *abs* have been evaluated. Up to an *abs* value around 0.5·*FO-4*, single-phase and two-phase circuits are similar in terms of speed. The single-phase circuits (both with inverters and buffers as inter-stage elements) do not work for *abs* over 0.5·*FO-4* even reducing frequency, while the two-phase solution clock skew tolerance is larger and depends on operating frequency (see Fig. 4). Note the extra clock skew tolerance of the circuits with inter-stage elements with respect to the direct connection. Moreover, inter-stage elements can handle large fan-out better than MOBILE elements.

The overlapping of the two clocks also relaxes the constraints on their transition times. There is a minimum allowable value for the transition time of the evaluating clock edge of MOBILE gates. This minimum value is determined by gate sizing and loading conditions. In addition, for a given size and load, there is also a maximum transition time, although in a well designed gate, it is high enough not to limit the circuit operation. However in the single-phase scheme an upper limit appears, related again, with the possibility of a gate evaluating the reset value of its previous one. To illustrate this, we have
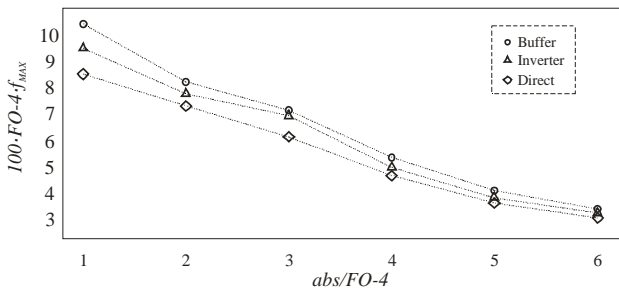
Fig 4. Two-phase scheme. Maximum frequency of operation for different values of *abs*.

carried out the following experiment. Circuits in Fig. 2a and Fig. 2b have been designed and simulated with inverters as MOBILE stages. We have set the transition time of the clocks seen by all stages to a given value ($T_{R,FIX}$), except one (marked in shadow) and we have determined the range of transition times ($T_{R,VAR}$) for this gate which result in correct operation. $T_{R,VAR}$ has been varied from 20ps to 125ps. Table I summarizes obtained results. It can be observed that for single-phase chains, as expected, the allowable range depends on the value fixed for the others clocks ($T_{R,FIX}$) and reduces for smaller values of this parameter. However for the two-phase architecture, bounds do not depend on it and the upper bound is 125ps, the maximum compatible with the period of the simulated clock. This experiment shows that the single-phase scheme is more sensitive to the transition times, which makes the design of its clock network more challenging. This translates in that larger transistors are required in the clock network increasing parasitics and power.

III. CASE STUDY. CLAS

4 bit RTD-CMOS MOBILE Carry Lookahead Adders (CLAs) have been designed with both the single-phase architecture and the two-phase one in order to further illustrates the advantages pointed out for the two-phase scheme in previous Section. Each CLA has been sized to work at a frequency of 0.12/*FO-4* at a supply voltage of 0.9V while minimizing power consumption. MOBILE gates require power clocks with controlled rise (fall) times. Circuitry generating them from external standard clocks has been also included in the designs. In this way input clocks drive transistor gates instead of acting as power clocks. Parasitic capacitances have been added to model drain and source diffusion parasitic (0.25fF), RTD-transistor contacts (0.25fF) and interconnections (1fF).

Table II shows results for both designed CLAs. For each case, we have included average power consumption (considering all feasible combination of the inputs), total RTD area and total transistor area. Significant improvement in power is obtained

with the two-phase clock scheme. Also area savings are observed. Total area of RTDs is larger in single-phase adder due to the presence of falling edge-triggered gates. Their parasitic capacitances associated to the larger p-transistors lead to greater RTDs to account for extra AC currents. Active transistor area is larger due to the p-transistors, but also to differences in clock generation circuit requiring larger transistors due to its smaller robustness and tolerance to clock transition mismatching as it was shown in previous Section.

In addition the two-phase design presents other relevant advantages over the single phase one. Robustness has been investigated through 3-σ Monte Carlo simulations. Gaussian distributions (relative error of ±*E*%) have been associated to the peak voltage, intrinsic capacitance and the peak current density of each RTD device. Variations of the supply voltage (±5%) around its nominal value have been considered. At the target operating frequency, the two-phase design tolerates up to *E*=7% while the single-phase one stands only *E*=2%. Clearly, tolerance can be increased by design enlarging the differences between nominal values of load and driver current to be compared. The important result is the differences observed when using a common design criteria (power minimization in this case).

IV. CONCLUSIONS

This paper compares RTD-CMOS realizations of fine-grained pipelined MOBILE circuits using a single-phase clock scheme and a novel two-phase clock solution for which experimental results are shown. The later presents advantages in terms of clock skew and transition time tolerance, which have been shown through simulations of chained inverters. Carry Lookahead Adders have been designed and evaluated as a case study. Superior robustness is obtained for the two phase implementations as well as significant area and power savings.

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TABLE I. BOUNDARIES FOR $T_{R,VAR}$

$T_{R,FIX}$ (ps)	SINGLE-PHASE		TWO-PHASE	
	$T_{R,VAR,MIN}$ (ps)	$T_{R,VAR,MAX}$ (ps)	$T_{R,VAR,MIN}$ (ps)	$T_{R,VAR,MAX}$ (ps)
40	20	70	20	125
80	40	100	20	125
120	70	125	20	125

TABLE II. NORMALIZED P_{AV} AND AREA COMPARISON

	$P_{AV,NORM}$	Norm. Area RTD	Norm. Area Trans.
SINGLE-PHASE	1.49	1.28	1.31
TWO-PHASE	1	1	1

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