Very Wide Range Tunable CMOS/Bipolar Current Mirrors with Voltage Clamped Input

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Abstract

In low power current mode signal processing circuits it is many times required to use current mirrors to replicate and amplify/attenuate current signals, and to clamp the voltage of nodes with high parasitic capacitances so that the smallest currents do not introduce unacceptable delays. The use of tunable active-input current mirrors would meet both requirements. In conventional active input current mirrors stability compensation is required. Furthermore, once stabilized, input current cannot be made arbitrarily small. In this paper we introduce two new active-input current mirrors that clamp their input node to a given voltage. One of them does not require compensation, while the other may require under some circumstances, but for both input current may take any value. The mirrors can operate with their transistors biased in strong inversion, weak inversion or even as CMOS compatible lateral bipolar devices. If biased in weak inversion or as lateral bipolars, the current mirror gain can be tuned over a very wide range. According to the experimental measurements provided in this paper, input current may spawn beyond nine decades, and current mirror gain can be tuned over 11 decades. As an application example a sinusoidal g_m-C based VCO has been fabricated whose oscillation frequency could be tuned for over 7 decades between 74mHz and 1MHz.

I. Introduction

When using current mode signal processing VLSI circuits it is not unusual that a very wide range of current levels have to be handled. For example, when building low power silicon retinas, light intensity is directly and (approximately) linearly transformed into current [1]-[2]. Silicon retinas can sense up to six decades of light levels, which yields also six decades of current levels at the photoreceptors output. It is impractical to permit that this current would control directly the time constant of the complete system. This would make a silicon retina be fast for high ambient light, but six orders of magnitude slower for low ambient light. This is not realistic, and a way to speed up these delays is by clamping the voltages of those nodes with high parasitic capacitances. Since current mirrors are necessary elements for current mode signal processing circuits, a very compact solution is to use current mirrors that clamp their input voltages. These current mirrors are usually referred to as *active input current mirrors* [3]-[4].

In the next Section the conventional active input current mirror is analyzed and it is shown why it needs compensation, why compensation depends on the mirror input current, and why this current cannot be made arbitrarily small. In Section III two new source driven active input current mirror topologies are introduced and stability is analyzed. One of the mirrors does not require compensation and the other may require under some circumstances. However, for both structures, input current can be made arbitrarily small without rendering unstable behavior. Section IV provides some intuition

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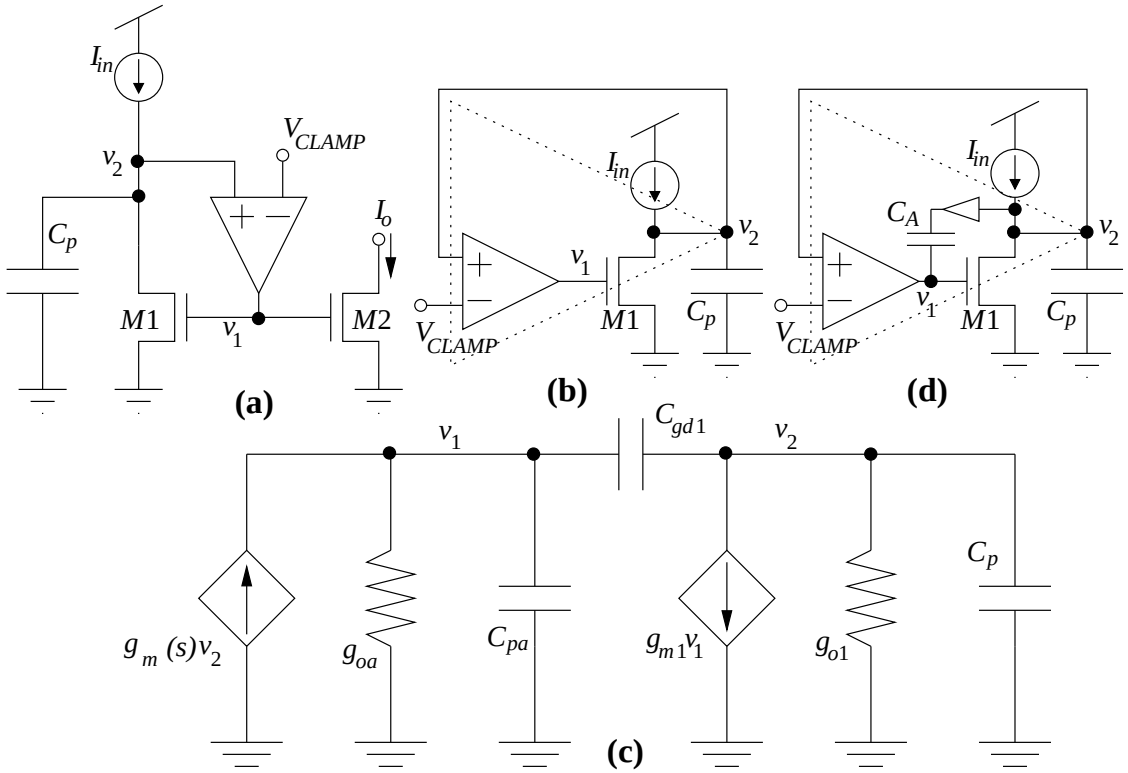


Fig. 1: Conventional active input current mirror, (a) circuit schematic representation, (b) input stage drawn as a 2-stage opamp, (c) small signal equivalent circuit for mirror input stage, (d) compensated circuit.

regarding dynamic behavior of the mirrors. Section V shows how to make the mirrors to have a continuously adjustable gain tunable over a very large range. Section VI studies loading effects. In Section VII it is shown how to extend the mirroring operations to bipolar transistors using the CMOS compatible lateral bipolar transistors, and finally in Section VII experimental measurements are provided that show the input currents spawning beyond six decades and the current mirror gains being adjusted over 11 decades. As an application example, the first mirror is used to make a constant linear input range OTA whose transconductance is tunable for over 7 decades. This OTA is then used in a g_m-C sinusoidal VCO whose oscillating frequency could be tuned from $74mHz$ to $1MHz$.

II. Conventional Active Input Current Mirror

The conventional active-input current mirror [3] is shown in Fig. 1(a). By redrawing its input stage as shown in Fig. 1(b), one recognizes a standard (uncompensated) 2-stage CMOS operational amplifier [5], connected in a unity-gain negative feedback configuration. The first stage of the opamp is the differential input amplifier of Fig. 1(a), and the second (inverting) stage consists of transistor $M1$ and current source I_{in}. It is well known that this structure needs compensation [5], and that the compensation circuitry depends on the value of the second stage bias current I_{in}. Furthermore, it results impractical to compensate when I_{in} has to be varied over many decades and reaches very low values.

For the differential input voltage amplifier the OTA in Fig. 2(a) can be used. OTAs are compensated by their load capacitance C_{pa}. An OTA connected in unity gain feedback configuration (as in Fig. 2(b)) has the small signal equivalent circuit shown in Fig. 2(c), where element $g_m(s)$ models the transconductance gain of the OTA and g_{oa} its output conductance. Transconductance

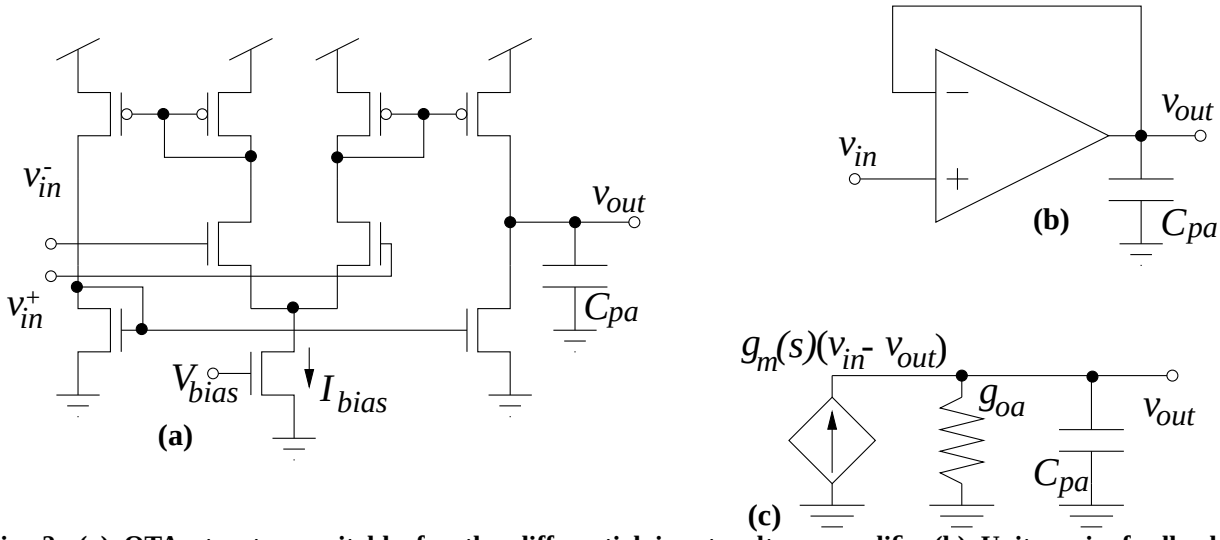


Fig. 2: (a) OTA structure suitable for the differential input voltage amplifier.(b) Unity gain feedback configuration, and (c) small signal equivalent circuit.

$g_m(s)$ is frequency dependent because of the delay introduced by the parasitic capacitances of the OTA internal nodes. This delay can be modeled as [6]

$$g_m(s) = g_{ma}\left(1 - \frac{s}{\omega_a}\right) \tag{1}$$

where g_{ma} is the DC transconductance gain of the OTA and ω_a models its delay. This yields the following stability condition for the circuit in Fig. 2(c)

$$C_{pa} > \frac{g_{ma}}{\omega_a} \tag{2}$$

Using this model for the OTA with the stability condition of eq. (2), it is possible to analyze the stability for the circuit in Fig. 1(b), whose small signal equivalent circuit is shown in Fig. 1(c). Transistor $M1$ is modeled by elements g_{m1}, g_{o1} and C_{gd1}, while the OTA is modeled by $g_m(s) = g_{ma}(1 - s/\omega_a)$, g_{oa} and the node v_1 parasitic capacitance C_{pa}. After straight forward analysis it is easy to see that, if eq. (2) is satisfied, imposing the condition

$$C_{gd1}(g_{m1} - g_{ma}) > \frac{g_{m1}g_{ma}}{\omega_a} \tag{3}$$

guarantees stability. But this requires, at least, that $g_{m1} > g_{ma}$ which imposes a lower bound on the value of g_{m1} (and I_{in}) in Fig. 1(b). In practice, the circuit is usually compensated as shown in Fig. 1(d) [3], by adding a unity gain voltage buffer and a compensation capacitor C_A. Eq. (3) would change to

$$g_{m1}(C_{gd1} + C_A) > \frac{g_{m1}g_{ma}}{\omega_a} + g_{ma}C_{gd1} \tag{4}$$

But again, g_{m1} cannot be made arbitrarily small.

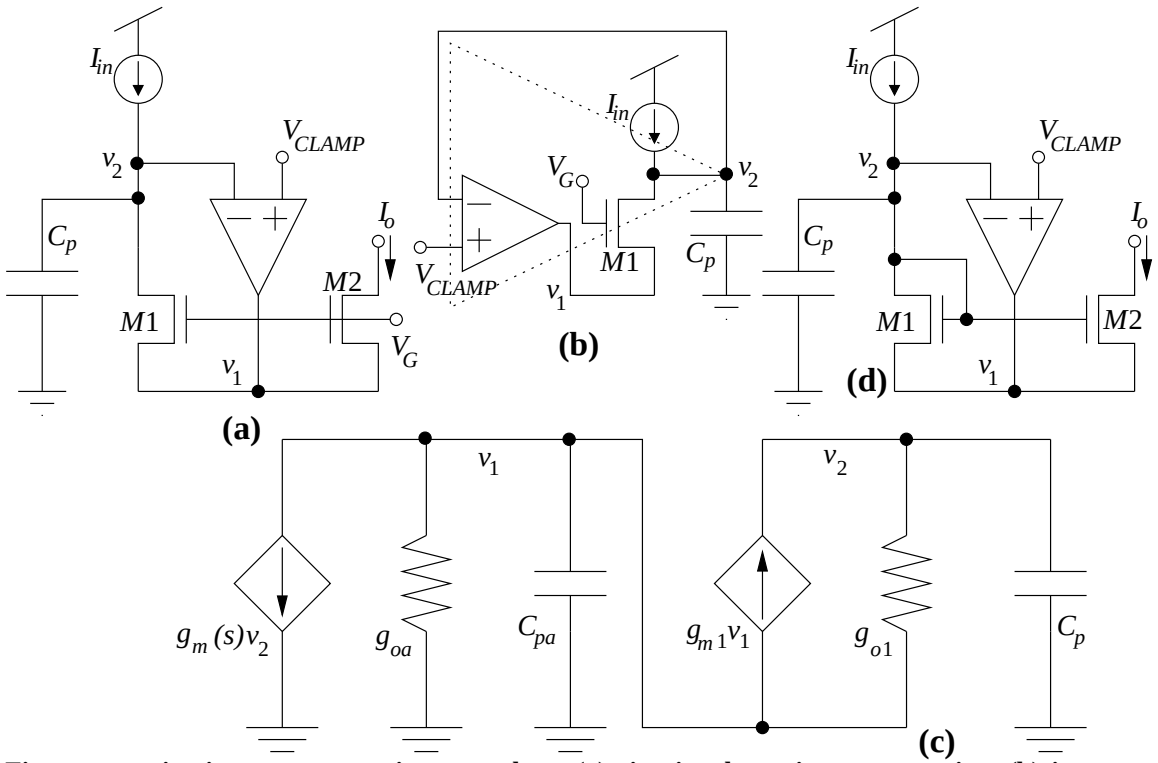


Fig. 3: First new active input current mirror topology, (a) circuit schematic representation, (b) input stage drawn as a 2-stage opamp, (c) small signal equivalent circuit. (d) Second current mirror topology.

The two new active input current mirror topologies introduced in this paper do not have this problem: g_{m1} (and consequently, I_{in}) can be made arbitrarily small. In the next Section these mirrors are introduced and analyzed.

III. Two New Active Input Current Mirrors

A. First Topology

The first alternative circuit to the one in Fig. 1(a) is shown in Fig. 3(a), where the OTA output drives the source of transistor $M1$ instead of its gate. The OTA must be able to sink twice the maximum expected value for I_{in}, which imposes an important design constraint for the OTA: I_{bias} in Fig. 2(a) must be, at least, twice the maximum operation current of the mirror[1]. The mirror input stage can be redrawn as shown in Fig. 3(b), which can be considered to be a special two stage opamp connected in unity gain feedback configuration. Note that the second stage of this opamp is a positive gain voltage amplifier, as opposed to the case of Fig. 1(b). Neglecting body effect of transistor $M1$, the absolute gain value of this second stage would be identical to that of Fig. 1(b). Also note, that the input node of this second stage is the source of transistor $M1$ which is a low impedance node. This makes the circuit of Fig. 1(b) to have a single dominant pole, and consequently its behavior is qualitatively similar to a single stage opamp in unity gain feedback configuration. To analyze the stability conditions for this circuit, let us resort to its small signal equivalent circuit, shown in Fig. 3(c). Its characteristics equation is

1. Eventually, special OTAs that operate in a type of class AB mode [7] could be used to optimize power consumption.

$$as^2 + bs + c = 0 \qquad \begin{cases} a = C_p C_{pa} \\ b = (g_{oa} + g_{m1})\, C_p - \dfrac{g_{m1} g_{ma}}{\omega_a} + g_{o1}\left(C_{pa} - \dfrac{g_{ma}}{\omega_a} \right) \\ c = g_{m1} g_{ma} \end{cases} \tag{5}$$

Since the OTA is assumed to be compensated, eq. (2) is satisfied, and the last term for coefficient *b* in eq. (5) is positive. However, *b* might still become negative. The following condition guarantees a positive *b* coefficient

$$C_p > \frac{g_{ma} g_{m1}}{\omega_a (g_{oa} + g_{m1})} \tag{6}$$

This can be achieved by either adding an extra capacitance at node v_2 or by making the OTA to have a smaller delay (larger ω_a) or lower g_{ma}. Note that the right hand side of eq. (6) is an increasing function of g_{m1}. Consequently, once eq. (6) is satisfied for the maximum possible g_{m1} (maximum I_{in}) stability is guaranteed for any smaller value of g_{m1} (and I_{in}).

If eq. (6) cannot be satisfied, another way to achieve compensation for this topology is by adding a compensation capacitor C_A between nodes v_1 and v_2 in Fig. 3. This yields the following characteristics equation

$$as^2 + bs + c = 0 \qquad \begin{cases} a = C_p C_{pa} + C_A\left(C_p + C_{pa} - \dfrac{g_{ma}}{\omega_a} \right) \\ b = C_p (g_{oa} + g_{m1}) + g_{o1}\left(C_{pa} - \dfrac{g_{ma}}{\omega_a} \right) + g_{ma}\left(C_A - \dfrac{g_{m1}}{\omega_a} \right) \\ c = g_{m1} g_{ma} \end{cases} \tag{7}$$

If eq. (2) is satisfied, coefficient *a* is positive as well as the second term of coefficient *b*. Consequently, stability is guaranteed if

$$C_A > g_{m1}\left(\frac{1}{\omega_a} - \frac{C_p}{g_{ma}} \right) - C_p \frac{g_{oa}}{g_{ma}} \tag{8}$$

If the right hand side of eq. (8) is negative, C_A is not necessary and eq. (6) results. If the right hand side of eq. (8) is positive, then C_A should satisfy eq. (8) for the largest value of g_{m1} (or I_{in}). Once this is assured, eq. (8) remains valid for any smaller value of g_{m1} (or I_{in}).

B. Second Topology

Another alternative active input current mirror is the one shown in Fig. 3(d). Note that in this case transistor $M1$ is connected as a diode around the negative feedback loop of the amplifier, and acts simply as a passive device. Therefore, if the differential voltage amplifier is already compensated for unity gain feedback, the circuit should always be stable. This can be verified by performing a similar analysis to that for the first topology.

C. Discussion

The stability analyses for both topologies are valid whether transistors $M1$ and $M2$ are biased in their weak or strong inversion regions of operation. This allows the current mirrors to operate for a

very wide range of currents: from values equal to junction leakage currents up to the maximum current the OTA might be able to sink. Also, care needs to be taken to avoid that the OTA output voltage reaches its minimum (or maximum, for p-type current mirrors) value by adjusting V_{CLAMP} to a safe enough level.

The stability advantages for these two new topologies with respect to the conventional one of Section II, come from the fact that the differential voltage amplifier is loaded by a low impedance node, which makes the whole circuit to behave similar to a single pole (or one-dominant pole) system. Although the *Topology* 1 current mirror might require stability compensation, it has certain advantages over the *Topology* 2 one, as will be seen throughout the paper: it is faster for very low currents and it can be operated in bipolar mode by simply rebiasing constant global voltages.

IV. Transient Response

A. First Topology

The circumstances under which the current mirror will be slowest is when input current is smallest (in the *nA* to *pA* range). In these cases transistor $M1$ is operating in weak inversion and it is safe to consider the OTA acting as an instantaneous device that does not introduce any delay. If this is the case, the large signal transient response of the circuit in Fig. 3(b) can be computed by modeling the mirror input stage as shown in Fig. 4(a) but with $C_{pa} = 0$. If g_{ma} and g_{oa} model the OTA and $I_{M1} = I_{S1}\exp\{(V_{G1} - v_1)/nU_T\}$ is the current through transistor $M1$, straight forward analysis yields the following state equation

$$I_{in} = I_{M1} + \frac{C_p}{g_{oa}A_v}\dot{I}_{M1} + C_p\frac{nU_T}{A_v}\frac{\dot{I}_{M1}}{I_{M1}} \tag{9}$$

where $A_v = g_{ma}/g_{oa}$ is the OTA voltage gain. If I_{in} changes in a step fashion from rI_c to I_c, the solution for eq. (9) can be written as

$$\frac{I_{M1}(t)}{[I_c - I_{M1}(t)]^{1+\varepsilon}} = \frac{rI_c}{[I_c - rI_c]^{1+\varepsilon}}e^{t/\tau_1} \tag{10}$$

where,

$$\tau_1 = \frac{C_p nU_T}{A_v I_c} \quad , \quad \varepsilon = \frac{I_c}{g_{oa}nU_T} \tag{11}$$

If we define t_{d1} as the delay time it takes for $I_{M1}(t)$ to reach RI_c, then

$$t_{d1} = \tau_1 \ln\left[\frac{R}{r}\left(\frac{1-r}{1-R}\right)^{1+\varepsilon}\right] \tag{12}$$

Note that if A_v is sufficiently large τ_1 can be reasonably small, even for low values of I_c.

As I_c increases the circuit will respond faster and the delay introduced by the OTA will start to be appreciable. In this case, the circuit shown in Fig. 4(a) with $C_{pa} \neq 0$ can be used to analyze its transient response. The resulting state equation does not have an analytical solution, thus in order to obtain an estimation of the delay in the current mirror one can resort to its small signal equivalent circuit, and consider I_{in} makes a "*little*" step. Neglecting the OTA internal delay[1] (characterized by

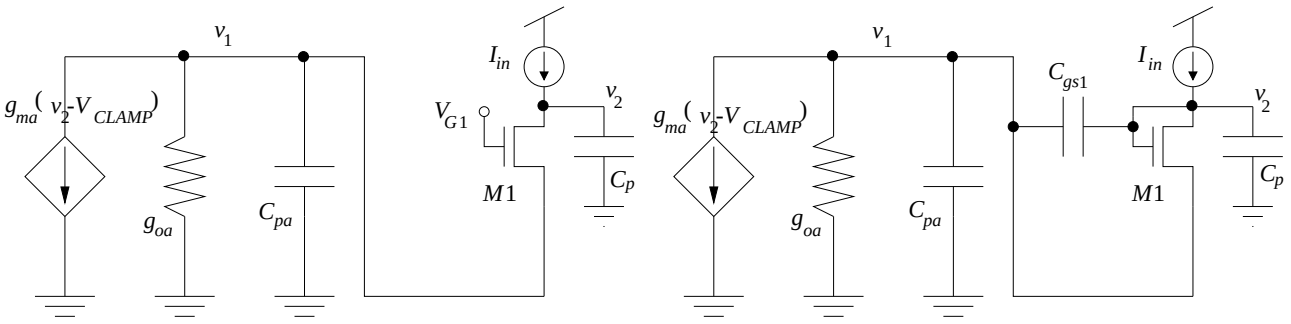


Fig. 4: Equivalent circuits for computing transient analysis if OTA delay cannot be neglected, for (a) first new topology and for (b) second new topology.

ω_a) the following characteristics equation (valid for weak and strong inversion) results for the circuit drawn in Fig. 3(c),

$$s^2 + \frac{s}{\tau_3} + \frac{1}{\tau_1 \tau_a} = 0 \qquad \begin{cases} \frac{1}{\tau_3} = \frac{g_{oa} + g_{m1}}{C_{pa}} + \frac{g_{o1}}{C_p} \\ \frac{1}{\tau_1} = \frac{g_{m1} A_v}{C_p} \\ \frac{1}{\tau_a} = \frac{g_{oa}}{C_{pa}} \end{cases} \tag{13}$$

The roots for this equation are given by

$$s_o = -\frac{1}{2\tau_3}\left[1 \pm \sqrt{1 - 4\frac{\tau_3^2}{\tau_1 \tau_a}}\right] \tag{14}$$

If $\tau_3^2/\tau_1\tau_a > 1/4$ two complex poles result and the transient has an associated time constant of the order of $2\tau_3$. If the poles are real, the dominant time constant may range from $2\tau_3$ (for high values of $\tau_3^2/\tau_1\tau_a$) to $\tau_1\tau_a/\tau_3$ (for small values of $\tau_3^2/\tau_1\tau_a$). Note that for very small values of I_{in} ($g_{m1} \approx 0$ and $g_{o1} \approx 0$) it follows that $\tau_3^2/\tau_1\tau_a \ll 1$ and $\tau_a \approx \tau_3$, and the resulting time constant is τ_1, as derived previously using the large signal first order model. On the other hand, for very large I_{in} (and g_{m1}) values $\tau_3^2/\tau_1\tau_a$ is also small and a dominant first order dynamics results with time constant $\tau_1\tau_a/\tau_3 \approx C_p/g_{ma}$. Consequently, for both very small I_{in} and very large I_{in} there are no complex poles and the dynamics is dominated by a single real pole. The maximum value of $\tau_3^2/\tau_1\tau_a$ is reached for $g_{m1} = g_{oa}$ (assuming $g_{m1}/C_{pa} \gg g_{o1}/C_p$), and is $A_v C_{pa}/4C_p$. Therefore, if $A_v < C_p/C_{pa}$ can be satisfied, no complex poles (and no ringing) will appear for the whole input current range.

If a compensation capacitor C_A is used, the resulting equation would be

1. The effect of ω_a might be included, although the main delay introduced by the OTA is given by g_{ma} loaded by C_{pa} and other loads.

$$s^2 + \frac{s}{\tau_3'} + \left(\frac{1}{\tau_a'}\right)^2 = 0 \tag{15}$$

where $\tau_3' = a/b$ and $(\tau_a')^2 = a/c$ with *a, b* and *c* given by eq. (7). Again, the associated dominant time constant would take a value between $2\tau_3'$ and $\tau_a'^2/\tau_3'$. For very small and very large I_{in} there is a dominant real pole of time constant $\tau_a'^2/\tau_3'$ that produces a first order dynamics. For very small I_{in} it results $\tau_a'^2/\tau_3' \approx \tau_1 + C_A/g_{m1}$, while for very large I_{in} it is $\tau_a'^2/\tau_3' \approx C_p/g_{ma}$. The maximum $(2\tau_3'/\tau_a)^2$ value is reached for $g_{m1} \approx g_{oa} + g_{ma}C_A/C_p$, for which two real poles result both of similar time constants around $1/\tau_3' = 2\,(g_{oa}/C_A + g_{ma}/C_p)$.

B. Second Topology

For the current mirror of Fig. 3(d) similar analyses can be done. For very small input currents, such that the OTA can be considered to respond instantaneously, the following state equation results (assuming $C_{pa} \approx 0$ and $C_{gs1} \approx 0$)

$$I_{in} = I_{M1} + \frac{C_p}{g_{oa}(A_v + 1)}\dot{I}_{M1} + \frac{C_p n U_T}{A_v + 1}\frac{\dot{I}_{M1}}{I_{M1}} \tag{16}$$

Consequently, eqs. (10)-(12) would also be valid for this mirror as long as A_v is substituted by $A_v + 1$.

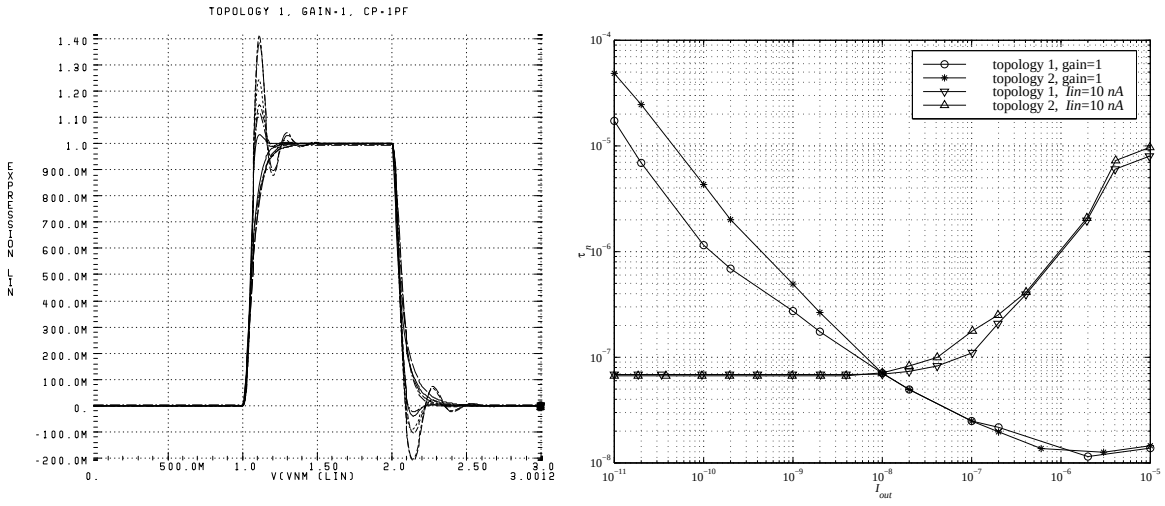
If the OTA might no longer be considered to respond instantaneously, or if C_{gs1} is not negligible with respect to C_p, an estimation of the delays can be obtained from the small signal equivalent circuit of Fig. 3(d) with $\omega_a = 0$. Routine analysis yields the following characteristics equation (valid for weak and strong inversion)

$$s^2 + \frac{s}{\tau_4} + \frac{1}{\tau_5^2} = 0 \qquad \begin{cases} \dfrac{1}{\tau_4} = \dfrac{C_{gs1} + C_p}{C_e^2} g_{oa} + \dfrac{C_{pa} + C_p}{C_e^2} g_{m1} + \dfrac{C_{gs1}}{C_e^2} g_{ma} \\ \dfrac{1}{\tau_5^2} = \dfrac{g_{ma} g_{m1}}{C_e^2} \\ C_e^2 = C_p C_{gs1} + C_p C_{pa} + C_{gs1} C_{pa} \end{cases} \tag{17}$$

Consequently, the settling of the mirror has a dominant time constant that can range between values of the order of $2\tau_4$ and τ_5^2/τ_4. For very small and very large I_{in} values (and assuming $C_p \gg C_{pa}, C_{gs1}$) it follows that $(2\tau_4/\tau_5)^2 \ll 1$ and a dominant first order dynamics results with effective time constant τ_5^2/τ_4. For very small I_{in} this time constant is $\tau_1 + C_{gs1}/g_{m1}$, while for very large I_{in} it is C_p/g_{ma}. The maximum value for $(2\tau_4/\tau_5)^2 = (C_{gs1} + C_{pa})/(C_{gs1} + C_p/A_v)$ is reached for $g_{m1} = g_{oa} + g_{ma}C_{gs1}/C_p$. Therefore, if $A_v C_{pa} < C_p$ can be satisfied no complex poles will appear.

C. Simulations

Extensive Hspice transient response simulations have been performed on both topology current mirrors to confirm the previous analyses. Sizes for transistors $M1$ and $M2$ were set to $150\mu m \times 5\mu m$ and the internal bias current for the OTA was $20\mu A$. An input node capacitance of $C_p = 1pF$ was considered and input current was changed in a step fashion from I_c to $2I_c$. The value



(a) **(b)**

Fig. 5: Transient Analyses Simulation Results. (a) Time and Amplitude Normalized Transient Responses for *Topology* 1 Current Mirror with Unity Gain, (b) Extracted values for τ_n for both Topologies with Unity Gain and Sweeping the Gain.

of I_c was swept logarithmically from $10pA$ to $10\mu A$. The output of the current mirror was connected to a voltage source equal to $V_{CLAMP} = 2.5V$. The current through this voltage source $I_o(t)$ was time-normalized to $I_o(t/\tau_n)$, where τ_n is the time at which I_o has reached 63.2% of its total excursion value (assuming a first-order-like response). Fig. 5(a) shows the simulated output waveforms, where the amplitude has also been normalized with respect to I_c,

$$\frac{I_o(t/\tau_n) - I_c}{I_c} \tag{18}$$

In Fig. 5(b), for the trace with circles, the corresponding values for τ_n as a function of I_c are represented for *Topology* 1 with $C_A = 0$. As discussed previously in Section IV.A, for very small currents the time constant is inversely proportional to current level (see eq. (11)), while for large currents the time constant tends to settle to a constant value (see discussion after eq. (14)). For I_c between $2nA$ and $100nA$ the mirror output current step response showed ringing (presence of complex conjugate poles), while outside this range no ringing is observed (absence of complex conjugate poles). This was also predicted by the theoretical discussion after eq. (14). Eventually, ringing could be reduced or suppressed by improving the circuit phase margin by adding the compensation capacitance C_A mentioned in Section III.A. However, C_A may increase the delays for the complete range of input currents.

The same simulations were repeated for the second topology. The resulting values of τ_n as a function of I_c are represented in Fig. 5(b) using the trace with asterisks. Again for very small currents the time constant is inversely proportional to current and tends to settle for large currents (as predicted in Section IV.B). Presence of complex conjugate poles was observed for I_c between $10nA$ and $100nA$, as anticipated by the discussion after eq. (17). Note that for the lower currents range the resulting values for τ_n are about twice than those for *Topology* 1. This is because for *Topology* 2 the input node capacitance C_p includes now also the subthreshold gate-to-bulk C_{gb} capacitance of transistor $M1$. For gate oxide thickness $t_{ox} = 10nm$ and gate area $A = 150 \times 5\mu m^2$ this capacitance is $C_{gb} = 0.4A\varepsilon_{ox}/t_{ox} = 1.05pF$ [8]. Therefore, in this example, the effective C_p

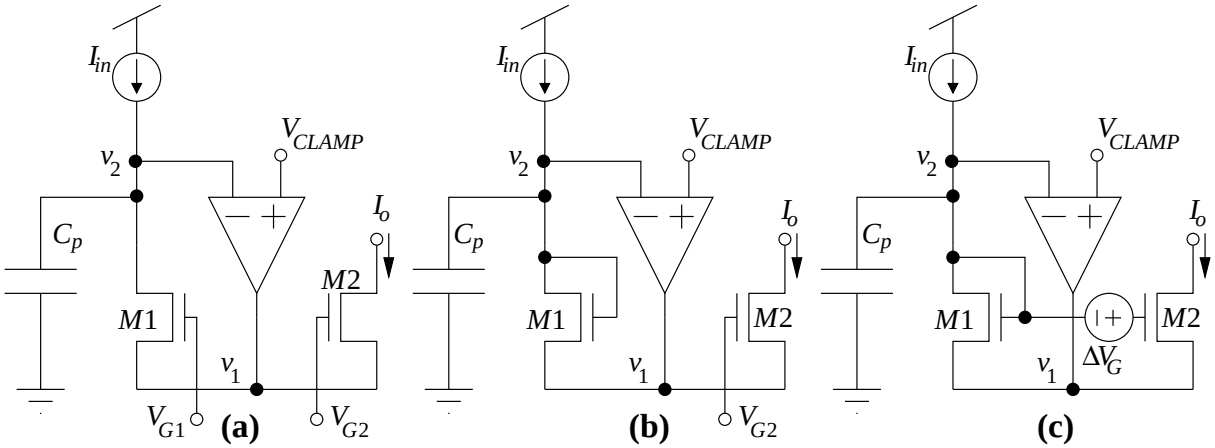


Fig. 6: Continuously adjustable gain current mirror versions for (a) first new topology, (b) second topology with absolute gate bias or (c) relative gate bias.

capacitance is about twice than for *Topology* 1, for the lower current range, which precisely explains the different τ_n values.

V. Continuously Adjustable Gain

The functionality of these current mirrors can be further extended when they operate in weak inversion: the current mirrors gain can be made continuously adjustable through a control voltage, and the adjustment range can be very wide (over 11 decades as shown later in the Section on experimental results). The way this is achieved is very simple. By connecting the gate of transistor $M2$ to an independent bias voltage V_{G2}, the gain of the current mirrors can be continuously controlled through voltage V_{G2}. This is shown in Fig. 6 for the two proposed current mirrors. Under these circumstances the currents through transistors $M1$ and $M2$ are given by

$$I_{in} = I_{s1} e^{\frac{V_G - v_1}{nU_T}}$$
$$I_o = I_{s2} e^{\frac{V_{G2} - v_1}{nU_T}} \tag{19}$$

where U_T is thermal voltage, V_G is the gate voltage of transistor $M1$ ($V_G = V_{G1}$ for Fig. 6(a) and[1] $V_G = V_{CLAMP}$ for Fig. 6(b) and (c)), and I_{s1} and I_{s2} are positive parameters which can be considered to be equal if transistors $M1$ and $M2$ are of equal size and properly well matched. From eq. (19) the current mirror output current is

$$I_o = A_i I_{in} \tag{20}$$

where A_i, which is a function of $V_{G2} - V_G$, is the gain of the current mirror and is equal to

$$A_i = \frac{I_{s2}}{I_{s1}} e^{\frac{V_{G2} - V_G}{nU_T}} \tag{21}$$

1. Strictly speaking, for Fig. 6(b), $V_G = V_{CLAMP} + V_{off} + [I_{in}/g_{oa} + \ln(I_{in}/I_{s1})] / (A_v + 1)$ where V_{off} is the input offset voltage of the OTA.

Since $V_{G2} - V_G$ controls exponentially the current mirror gain, a very wide tuning range is expected.

If there is mismatch between transistors $M1$ and $M2$ it will influence eq. (21) through parameters I_{s1} and I_{s2}. Statistically, the standard quadratic relative deviation of the gain is given by

$$\sigma^2(\Delta A_i/A_i) = \sigma^2(\Delta I_{s1}/I_{s1}) + \sigma^2(\Delta I_{s2}/I_{s2}) + \frac{\sigma^2(\Delta V_{off})}{V_{EA}^2} \tag{22}$$

where V_{EA} is transistors $M1$ and $M2$ Early voltage. Note that eq. (22) is independent of the value of V_{G2} and V_G. For the mirror of Fig. 6(b), the offset introduced by the OTA changes eq. (22) to

$$\sigma^2(\Delta A_i/A_i) = \sigma^2(\Delta I_{s1}/I_{s1}) + \sigma^2(\Delta I_{s2}/I_{s2}) + \frac{\sigma^2(\Delta V_{off})}{n^2 U_T^2} \tag{23}$$

where the V_{off} contribution is much larger, which might render the circuit unacceptable. In this case the mirror gain should be adjusted by controlling the differential voltage between the gates of transistors $M1$ and $M2$, as shown in Fig. 6(c). In this case eq. (22) is valid again.

The relative noise spectral density at the output current I_o is given for Fig. 6(a) and Fig. 6(c) by

$$\frac{\overline{i_o}^2}{I_o^2} = \frac{1+\left(\frac{\omega}{\omega_2}\right)^2}{1+\left(\frac{\omega}{\omega_1}\right)^2}\frac{\overline{i_{n1}}^2}{I_{in}^2} + \frac{1+\left(\frac{\omega}{\omega_3}\right)^2}{1+\left(\frac{\omega}{\omega_1}\right)^2}\frac{\overline{i_{n2}}^2}{I_o^2} + \frac{1+\left(\frac{\omega}{\omega_4}\right)^2}{1+\left(\frac{\omega}{\omega_1}\right)^2}\frac{\overline{v_{na}}^2}{V_{EA}^2} \tag{24}$$

where $\overline{i_{n1}}$ and $\overline{i_{n2}}$ are the noise spectral density currents generated by $M1$ and $M2$ respectively, $\overline{v_{na}}$ is the equivalent input noise spectral density for the OTA and

$$\omega_1^{-1} = C_p\left(\frac{1+A_i}{g_{ma}} + \frac{1}{g_{m1}A_v}\right) \quad \omega_2^{-1} = \frac{C_p}{g_{ma}} \quad \omega_3^{-1} = C_p\left(\frac{1}{g_{ma}} + \frac{1}{g_{m1}A_v}\right) \quad \omega_4^{-1} = \frac{C_p}{g_{o1}} \tag{25}$$

with $A_v = g_{ma}/g_{oa}$ being the OTA voltage gain. Note that, by eq. (24), the output noise is not degraded by the fact that A_i might become extremely large or extremely small. For Fig. 6(b) the output current relative noise spectral density is given by

$$\frac{\overline{i_o}^2}{I_o^2} = \frac{1+\left(\frac{\omega}{\omega_2}\right)^2}{1+\left(\frac{\omega}{\omega_1}\right)^2}\frac{\overline{i_{n1}}^2}{I_{in}^2} + \frac{1+\left(\frac{\omega}{\omega_3}\right)^2}{1+\left(\frac{\omega}{\omega_1}\right)^2}\frac{\overline{i_{n2}}^2}{I_o^2} + \frac{1+\left(\frac{\omega}{\omega_5}\right)^2}{1+\left(\frac{\omega}{\omega_1}\right)^2}\frac{\overline{v_{na}}^2}{n^2 U_T^2} \tag{26}$$

with $\omega_5^{-1} = C_p/g_{m1}$. Note that the OTA noise contribution is here significantly larger than in eq. (24), which might render this topology useless.

VI. Loading Effects

The stability analyses developed in Section III are based on the assumption that stability behavior of the circuit in Fig. 3(a) can be analyzed by using the circuit in Fig. 3(b). However, this is true if the current flowing through transistor $M2$ does not alter the stability conditions derived by using the circuit in Fig. 3(b). Note that if current mirror gain adjustment is used (as in Fig. 6) the current

through transistor $M2$ can be several orders of magnitude larger than the one through transistor $M1$. Furthermore, the load connected at the drain of transistor $M2$ is going to be coupled to the current mirror circuitry through the output conductance of $M2$. On the other hand, since the gate of $M2$ is connected to a fixed voltage, no capacitive coupling (through C_{dg2} and/or C_{gs2}) exists between the load and the current mirror circuitry. Assuming the load at the drain of transistor $M2$ can be approximated by the parallel connection of a resistance and a capacitance, small signal analysis reveals that the stability conditions for both topologies are relaxed. Consequently, the conditions developed in Section III are more stringent and are the ones to be used.

The transient response analyses in Section IV neglect completely the loading effect of transistor $M2$. Strictly speaking, this is only true if, for equal size $M1$ and $M2$ transistors, the gain of the mirror is much less than unity, so that current through $M2$ is negligible with respect to the one through $M1$. However, if the gain is unity or larger a slower response is expected because the OTA has to provide a significantly larger current.

For *Topology* 1, very small currents and neglecting the loads at the drain of $M2$, it is easy to show that eq. (9) changes to

$$I_{in} = I_{M1} + \frac{C_p (1 + A_i)}{g_{oa} A_v} \dot{I}_{M1} + C_p \frac{n U_T}{A_v} \frac{\dot{I}_{M1}}{I_{M1}} \tag{27}$$

where A_i is the gain of the current mirror. This implies that eqs. (10)-(12) remain valid as long as ε is substituted by

$$\varepsilon' = (1 + A_i)\, \varepsilon \tag{28}$$

which reveals that delay t_{d1} in eq. (12) is degraded, at the most, by a factor of A_i. If capacitance C_{pa} cannot be neglected and/or $C_A \neq 0$ small signal analysis can be performed to estimate the time constant degradation. For high current amplification values A_i it can be verified that the resulting time constant is degraded at the most by a factor of the order of A_i.

Hspice simulations were performed using the same circuit than in Section IV.C, *Topology* 1, but with a constant input current step from $I_c = 10nA$ to $2I_c = 20nA$ and sweeping the mirror gain from $A_i = 10^{-3}$ to $A_i = 10^{3}$. The results are shown in Fig. 5(b) using the trace with "*down triangles*". For gains smaller than unity, time response is constant, while for gains larger than unity the time response is degraded as A_i increases. As can be seen the resulting time constant is increased, at the most, by a factor A_i.

For *Topology* 2, and very small currents, a much more complicated differential equation than eq. (24) is obtained which does not have an analytical solution. However, by performing Hspice simulations on this topology with $I_c = 10nA$, shown in Fig. 5(b) with "*up triangles*", it is observed that the time constant degradation is similar to that for *Topology* 1. Again, for high A_i values, time constants are degraded, at the most, by a factor of the order of A_i.

VII. CMOS Compatible Lateral Bipolar Mode

The two new current mirror topologies discussed so far can also be operated by biasing the transistors as CMOS compatible lateral bipolars [8]. The circuits in Fig. 3 and Fig. 6 can be biased to

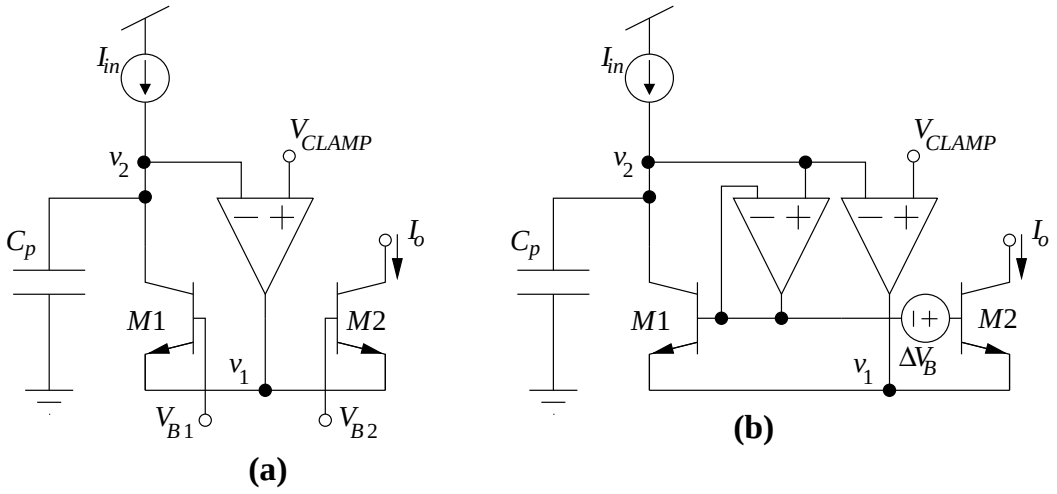


Fig. 7: Bipolar versions of continuously adjustable gain current mirrors, (a) for first topology and (b) second topology

operate transistors $M1$ and $M2$ as lateral bipolars if the process is p-well. For an n-well process p-type current mirrors are the ones that can be biased in lateral bipolar mode. The first topology (Fig. 6(a)) can be used directly by rebiasing gate and well voltages, while the second topology needs the use of an extra differential voltage amplifier or OTA. Fig. 7(a) shows the bipolar version of the current mirror in Fig. 6(a). Physically both circuits are the same. The difference is how the gates and wells of transistors $M1$ and $M2$ are biased. In Fig. 6(a) the wells are connected to ground (or to positive power supply for a PMOS mirror) while V_{G1} and V_{G2} should be connected to intermediate voltage values such that, for the current levels used, the OTA output voltage does not saturate. In Fig. 7(a) both gates have to be connected about $1V$ below ground (or $1V$ above positive power supply for the p-version) [8] and the wells, which are now the Base terminals, to intermediate values. For the bipolar version of the second topology an extra OTA has to be added to decouple the nonzero base currents. The resulting circuit is shown in Fig. 7(b).

VIII. Experimental Results

A set of current mirror prototypes have been fabricated in a 1.2µm n-well CMOS process. Transistors were laid out as square waffle structures with $L = 4.8\mu m$ and effective $W = 1378\mu m$. In this case an OTA able to provide several *milli-amps* of output current was used. Fig. 8 shows measurements of I_o vs. I_{in}, for different gains, for an NMOS, a PMOS, and a lateral bipolar pnp mirrors, corresponding to the Topologies of Fig. 6(a) and Fig. 7(a). In Fig. 8 input currents were swept between $1pA$ and $1mA$. Gain control voltage (V_{G2} or V_{B2}) was swept with $50mV$ steps around V_{G1} or V_{B1}. In these log-log representations, lines of slope '1' represent a linear relationship between input and output currents, while line position accounts for the gain. Circles denote the 1% linearity error region limits. For these regions the maximum and minimum current mirror gains are given in Table 1 as A_{min} and A_{max}. Also shown in Fig. 8 are the maximum size rectangles that could be drawn inside the 1% linearity error regions. Maximum and minimum currents and gains for these boxes are given in Table 2. Note that in Fig. 8, for the unity gain curves, the 1% error interval is significantly larger than for the other curves. These limits are given in Table 1 under I_{min} and I_{max}.

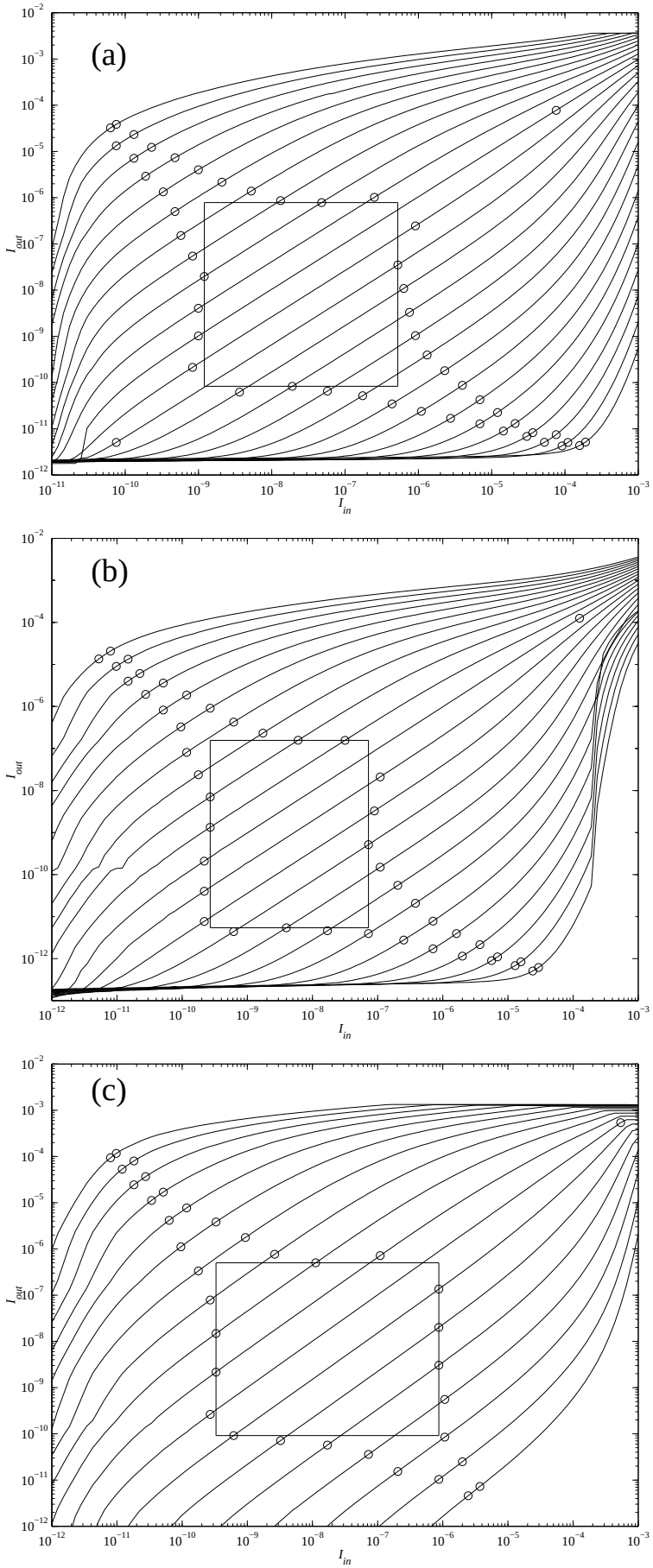


Fig. 8: Experimentally measured Output vs. Input Currents, for different gains, for (a) the NMOS mirror, (b) the PMOS mirror, and (c) the Bipolar mirror versions.

Table 1

	Absolute		Unity Gain	
	A_{min}	A_{max}	I_{min}	I_{max}
NMOS	6.1×10^{-7}	1.8×10^{5}	1.0×10^{-9}	7.7×10^{-5}
PMOS	5.7×10^{-7}	2.6×10^{6}	2.1×10^{-10}	1.2×10^{-4}
Bipolar	1.9×10^{-6}	4.5×10^{6}	2.7×10^{-10}	5.4×10^{-4}

Table 2

	I_{in}^{min}	I_{in}^{max}	I_{out}^{min}	I_{out}^{max}	A_{min}	A_{max}
NMOS	1.2 *nA*	520 *nA*	83 *pA*	780 *nA*	2.9×10^{-4}	2.7×10^{2}
PMOS	0.27 *nA*	72 *nA*	5.4*pA*	160 *nA*	2.7×10^{-4}	1.4×10^{2}
Bipolar	0.33 *nA*	871 *nA*	92 *pA*	500 *nA*	5.1×10^{-4}	3.0×10^{2}

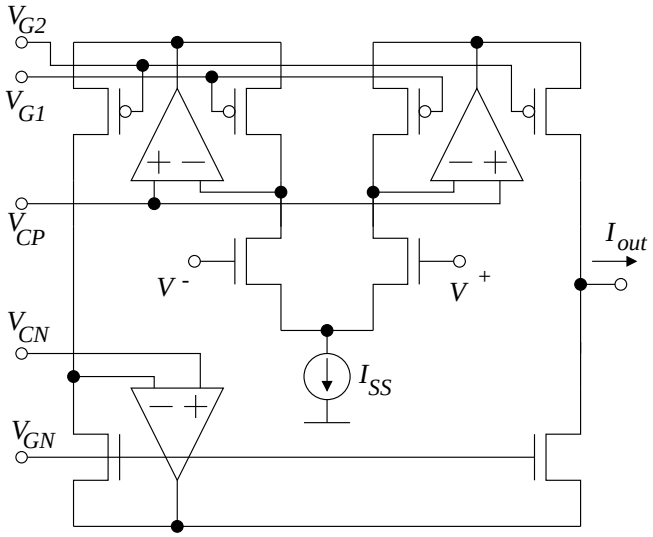


Fig. 9: Constant Linear Input Range OTA using *Topology*-1 Current Mirror

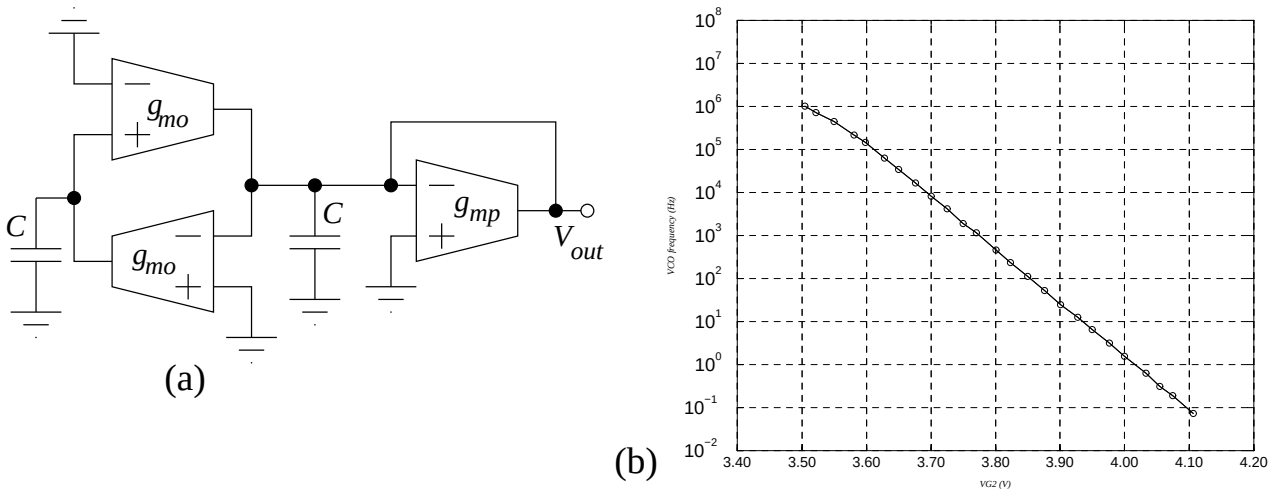


Fig. 10: (a) Sinusoidal g_m-C based VCO, (b) experimentally Measured Relationship between Sinusoidal VCO Frequency and Control Voltage V_{G2}.

As an application example, the *Topology*-1 current mirror was used to design the OTA shown in Fig. 9, which is used in the g_m-C sinusoidal VCO shown in Fig. 10 [6]. The oscillation frequency for this VCO is given by

$$f_{VCO} = \frac{1}{2\pi}\frac{g_{mo}}{C} \tag{29}$$

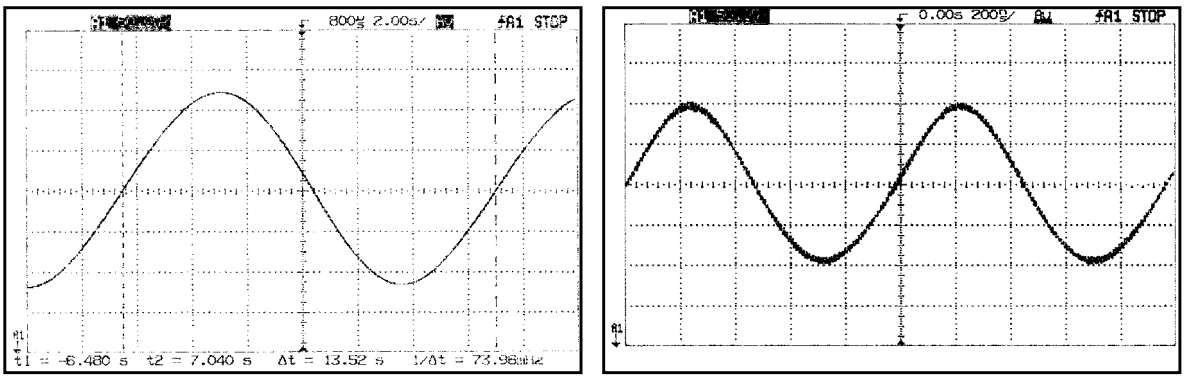


Fig. 11: Measured VCO outputs for minimum (73.94mHz) and maximum (1.015MHz) frequencies. Vertical scale is 50*mV/div* and horizontal scales are 2s/div for left trace and 200ns/div for right trace.

For the fabricated prototype VCO the capacitor value is $C = 10pF$. When using conventional CMOS OTAs for g_m-C sinusoidal VCOs, their frequency tuning range is limited to little more than one decade [6]. The reason is that for tuning the VCO frequency, OTA transconductances have to be changed. If the OTA transconductance is adjusted through its differential pair bias current I_{ss} then the linear range of the OTA is reduced as its transconductance (and I_{ss}) is lowered. If a linear range above $200mV$ is desired, transconductance tuning is limited to little more than one decade. The transconductance of the OTA in Fig. 9 can be tuned while maintaining its I_{ss} current (and linear range) constant. The two top *Topology*-1 PMOS current mirrors are tuned simultaneously through control voltage V_{G2} and are able to change the OTA transconductance for over 7 decades. Fig. 10(b) shows the experimentally obtained relationship between oscillation frequency and control voltage V_{G2} of the sinusoidal VCO. The minimum frequency that could be measured was $f_{min} = 73.96mHz$, while the maximum was $f_{max} = 1.015MHz$. Fig. 11 shows the measured sinusoidal waveforms for these two limit situations.

To show the effect of OTA linear input range degradation, let us resort to Fig. 12. Classically, the OTA transconductance g_m is tuned by changing its differential pair tail bias current I_{SS}. Fig. 12(a) shows the measured curves $I_{out}(V_{in})/I_{SS}$ for the OTA of Fig. 9 ($V_{in} = V^+ - V^-$) when using current I_{SS} for tuning and leaving V_{G2} constant. Fig. 12(b) shows the curves $I'_{out}(V_{in})/g_m$, which are the first derivatives of those in Fig. 12(a) normalized with respect to g_m (defined as the slopes at $V_{in} = 0$ for Fig. 12(a)). The widest bell-shape curve corresponds to the maximum I_{SS} and maximum g_m. As I_{SS} is decreased the bells become narrower (less input range) until the differential pair transistors are fully biased in weak inversion and the linear input range remains constant (between one or two nU_T). In Fig. 12(a) and Fig. 12(b) the largest measured transconductance is $g_m = 30.0\mu A/V$, while the minimum is $g_m = 60.4pA/V$. If instead of using I_{SS} to tune g_m we use V_{G2} then the curves shown in Fig. 12(c) and Fig. 12(d) are measured. Fig. 12(c) shows $I_{out}(V_{in})/\left|I_{out}^{max}\right|$ and Fig. 12(d) shows $I'_{out}(V_{in})/g_m$. In Fig. 12(c) and Fig. 12(d) the largest measured transconductance is $g_m = 30.0\mu A/V$, while the minimum is $g_m = 40.0pA/V$. Note that now the OTA input range is maintained constant. As a result, the OTA behaves almost linearly from $-100mV$ to $+100mV$ which means that low distortion sinusoids of $200mV$ peak-to-peak amplitude can be obtained with the VCO of Fig. 10 for the whole frequency range, as can be seen in Fig. 11.

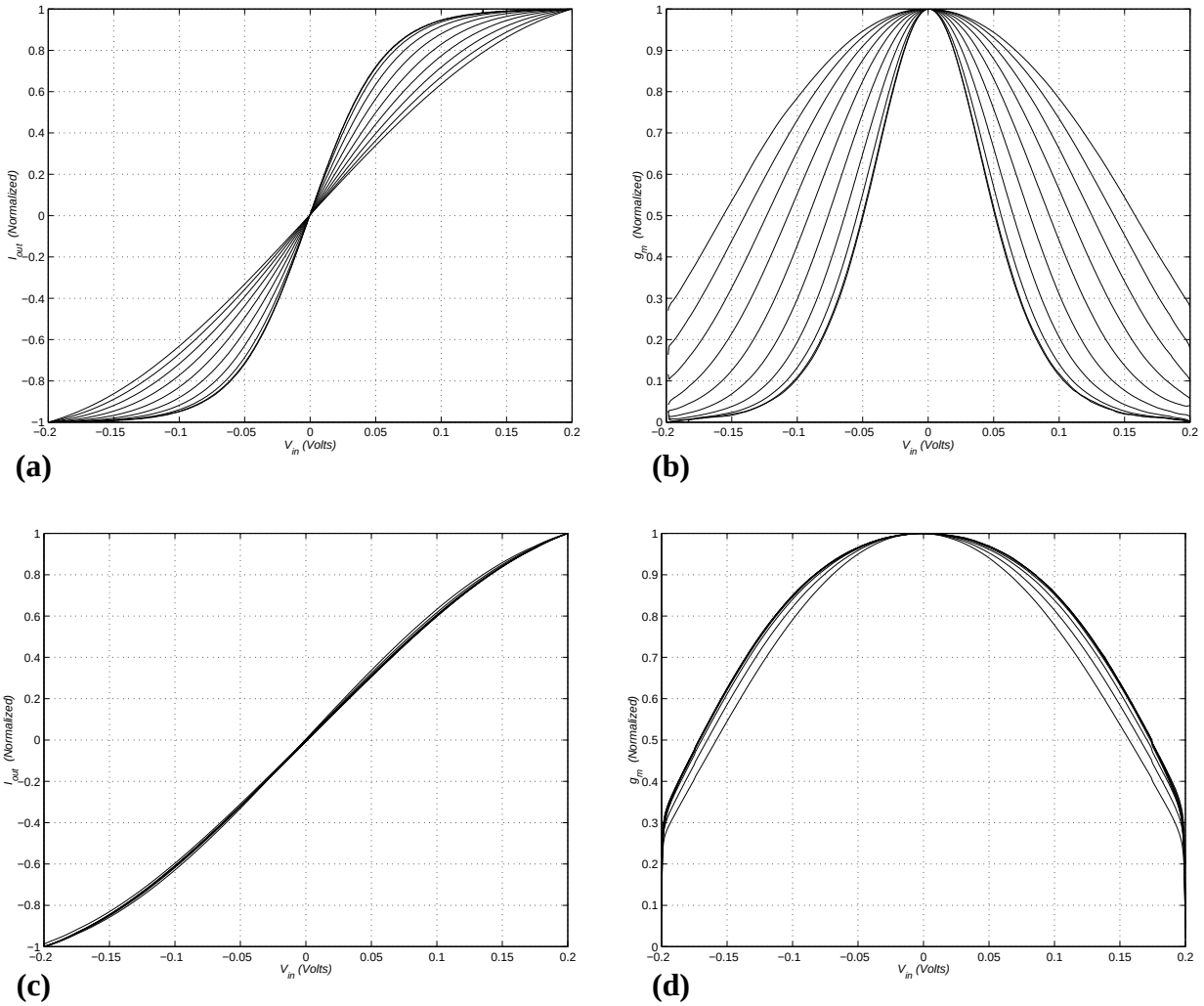


Fig. 12: Experimentally measured dependence of OTA linear input range on transconductance tuning. For differential pair tail bias current (I_{SS}) tuning, linear range decreases as transconductance decreases: (a) normalized OTA output current (I_{out}/I_{SS}) as a function of differential input voltage, (b) normalized first derivative of previous curve. For tuning through the top *Topology*-1 current mirrors: (c) normalized OTA output current, (d) normalized first derivative of previous curve.

IX. Conclusions

Two new active-input current mirror structures are introduced. The novelty resides in that the active amplifier drives transistor sources instead of gates. This allows the amplifier to be connected in a negative feedback loop configuration, instead of positive. The first proposed topology might require compensation, while the second does not need it. Both topologies behave much better from a stability point of view than the conventional active input current mirror. This is because the amplifier output is connected to a low impedance node. The consequence is that the mirrors remain stable for arbitrarily small operation currents, thus allowing current ranges of many decades. Experimental measurements reveal that the currents involved can vary over 9 decades, and that the gain of these current mirrors can be continuously tuned over 11 decades while maintaining 1% linearity error in the mirroring operation. The mirrors can be used either with their transistors biased as MOS or as CMOS compatible lateral bipolar devices. Experimental results have been provided. As an application example a g_m-C sinusoidal VCO has been fabricated and tested. Its frequency could be continuously tuned for over 7 decades through a single control voltage. To our knowledge this has never been achieved before for CMOS sinusoidal VCOs.

X. Acknowledgements

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XI. References

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