## Guest Editorial Special Issue on Neural Networks Hardware Implementations

NCE the very beginning of the neural network era, there has been the belief that to fully exploit the potential of this technology it would be necessary to also develop efficient hardware implementation techniques. In the last two decades, we have witnessed how the neural networks community is managing to acquire a more profound understanding of what neural networks can do and how. Neural networks knowledge has been enriched by developing more solid mathematical frameworks, by elaborating more efficient and powerful algorithms, by unfolding mysteries behind biological neural networks both at the individual neuron level and at different hierarchical levels of neuron ensembles and brain functions.

In the last decade, we have seen how the initial "euphoria" of neural network expectations has settled down to a solid knowledge and research capable of undertaking complex problems and providing powerful solutions. In the field of hardware implementations, progress has been continuing as well. The challenge has been and still is to follow what biology does and how, to be able to build more complicated and larger size systems, to implement efficient hardware learning techniques, to improve speed and/or lower power consumptions, to efficiently exploit or develop new signal/state representation techniques (e.g., continuous-time, pulse based, spiking nature, ...), to exploit noise and statistical properties, etc., and to apply all these ideas in real-world applications where efficient hardware solutions are necessary to provide compactness, high-speed and low-power consumptions.

In recent years significant progress in hardware solutions is being achieved. For this reason we believe it is a good point in time for a Special Issue on Neural Networks Hardware Implementations for the IEEE TRANSACTIONS ON NEURAL NETWORKS. The Special Issue Call for Papers had an overwhelming response. Originally, 70 papers were considered for possible publication. From those, 35 made it finally into the Special Issue. The review process was carried out by splitting the load between the four guest editors. The review process went quite smoothly thanks to the close cooperation between guest editors and the fast efficient response of reviewers. The final set of papers can be grossly classified into two main groups of similar size: the mainly digital papers and the mainly analog papers. Within the analog group are included also the mixed Analog-Digital implementation papers. Besides this main classification the subsequent subgroups are many times fairly arbitrary, because most of the times the possible classifications overlap depending upon different criteria. This reflects the richness of techniques, methodologies, and applications of neural hardware. We finally chose to classify them into the following groups.

## A. Digital Neural Network Hardware

- 1) FPGA-Based Implementations: Quite impressive systems can be implemented using present day very powerful field-programmable gate arrays (FPGAs) commercial chips, as illustrated by the five papers in this category. Mehrtash et al. embrace a very sophisticated project involving Spiking Neurons. Anguita et al. discuss the Implementation of Support Vector Machines using FPGAs. Denby et al. apply FPGAs for very High Speed Pattern Recognition in High Energy Physics Experiments. Hikawa et al. exploit pulse mode techniques on FPGAs. Kim et al. use FPGAs for Blind Signal Separation and Active Noise Cancelling.
- 2) DSP-Based Implementations: Another interesting and powerful digital alternative is the use of commercial digital signal processing (DSP) chips, like in the two papers in this category. Venayagamoorthy *et al.*implement Neurocontrollers for Turbogenerator Power Systems, and Kehtarnavaz *et al.* perform Classification of Analog and Digital Modulation Signals.
- 3) ASIC-Based Implementation: More efficient and challenging tasks may require the design of special purpose application specific integrated circuits (ASICs). This is illustrated by the seven papers in this group. Bracco et al. demonstrate Hierarchical Vector Quantization (HVQ) combining an ASIC with commercial FPGAs. Hendry et al. implement an Intellectual Property (IP) core for a Self-Organizing Neural Network. Bermak et al. implement an impressive 3-D VLSI Classifier. Porrman et al. report on a very powerful implementation of Self-Organizing Feature Maps. Sato et al. implement a Stochastic Logic based Neurochip. Kocak et al. show a Spike based Random Neural Network Implementation. And Yagi et al. provide a Hardware Friendly Image Representation Algorithm for Neuro-Associative-Processor based Recognition Systems.
- 4) Mixed Digital Implementations: In this category, we have put a single paper in which Yang et al. compare FPGA, DSP, and ZISC implementations for Radial Basis Function (RBF) Neural Networks applied to face tracking/identification.

## B. Analog Neural Network Hardware

1) Circuits and Components: In this category, we have those papers that emphasize circuits aspects of specific components. Gopalan *et al.* report on a Wide Range Euclidean

Distance Circuit. Milev *et al.*show a Quadratic Nonlinearity Synapse and its application to a 2176 synapse neural matrix array for finger-print feature extraction. Hirose *et al.* provide a Recurrent Decision Circuit that improves convergence performance. Linares *et al.* report on mini-DACs based Calibrated Weighting Techniques.

- 2) Floating Gate MOS Techniques: Floating Gate MOSFET-based signal processing is a powerful, compact and very attractive technique for neural massive arrays. Beiu et al. provide an excellent overview on this topic applied to digital circuits or "Threshold Logic." Aunet et al. propose a design method based on Real-Time Reconfigurable Threshold Elements. Yamasaki et al. present a Soft-Pattern Matching Classifier using FGMOS technology.
- 3) Spiking Systems: In recent years, important progress has been made in spiking circuits and systems, which are very appealing because of their compactness, computational efficiency, circuit simplicity and biological flavour. Culurciello *et al.* discuss Address Merit Criteria and Tradeoffs for Address-Event Spike Communication Channels. Cosp *et al.* use a Neuromorphic Oscillatory Network for Scene Segmentation. Chicca *et al.*report on a learning network of Integrate-and-Fire Neurons. Asai *et al.* show a Competitive Frequency and Temporal Domain Neurochip of Integrate-and-Fire Neurons.
- 4) Active Waves and Central Pattern Generators: There are three papers in this very biologically inspired topic. Carmona *et al.* report on a complete 2-D Programmable Chip intended for Early Vision Applications. Serrano *et al.* exploit weak inversion MOS operation with Log-domain circuit techniques to reproduce those phenomena. Nakada *et al.* have developed a Central Pattern Generator analog chip for Quadrupled Locomotion.
- 5) Other Mixed Signal Systems: Finally in this category, we have included those papers that do not fit very well in the previous ones. Note that most of the previous papers could

have been classified here as well. Kowalski reports a chip for Weighted Order Statistics Image Processing. Vidal *et al.* present a Neuro-Fuzzy Chip for handling complex tasks. Horio *et al.*introduce an impressive 10 000 Neurons Chaotic-based Chip. Kameda *et al.* present a Retina chip that includes bio-inspired Sustained and Transient Response channels. NG *et al.* show analog and digital implementations of Binary Relation Inference Networks for optimization problems. Finally Genov *et al.* report their Kerneltron chip which is a high speed Support Vector Machine.

We may conclude that present day state-of-the-art in neural network hardware has reached an important level of maturity, where researchers and engineers are able to build very complex systems that can be applied to a variety of real-world problems.

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Dr. Linares-Barranco was corecipient of the 1997 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Best Paper Award for "A Real-Time Clustering Microchip Neural Engine," and of the 2000 IEEE Circuits and Systems Society Darlington Award for the paper "A General Translinear Principle for Subthreshold MOS Transistors." He organized the 1994 Nips Post-Conference Workshop "Neural Hardware Engineering." From July 1997 until July 1999, he was Associate Editor of the IEEE Transactions on Circuits and Systems—Part II, and since January 1998 he is also Associate Editor for IEEE Transactions on Neural Networks. He is Chief Guest Editor of the 2003 IEEE Transactions on Neural Networks Special Issue on Neural Hardware Implementations.



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