A study of the sensitivity of switched-current wave analog filters to mismatching and clock-feedthrough errors

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ABSTRACT

The influence of the main source of errors in Switched-Current (SI) filters over the performance of Wave Analog Filters (WAF) is evaluated. Models of mismatching and clock-feedthrough (CF) are deduced for basic building blocks, and applied to study the sensitivity of a third-order filter. Monte Carlo simulations performed using a behavior simulator prove that CF are dominant over mismatching effects.

INTRODUCTION

Two different approaches have been explored for switched-current (SI) low-sensitivity filter realizations; both simulate passive LC ladder structures. One follows the well-known synthesis methodologies applied for switched-capacitor filters, hence requiring SI integrators as building blocks [1-3]. The other is based on simulating Wave Digital Filter (WDF) structures [4-6].

In addition to excellent passband sensitivity properties, WAFs have two inherent advantages. They are based on the bilinear mapping and involve very regular and simple circuit elements. We have already proved the feasibility of this approach, obtaining SI WAF prototypes [4-6].

An important property of SI WAF is that the range of current gain values in any adaptor does not greatly differ between one filter function and other.

This paper deals with the study of mismatching and CF induced errors, that, will allow us to derive design rules for minimizing their influence in WAF. A statistic model is proposed for the study of random mismatching errors in SI implementations of WAF (systematic mismatching errors are assumed cancelled by an appropriated design of the basic cells), and a statistic sensitivity measure is carried out for a low-pass filter using this model and Monte Carlo simulations. On the other hand, the sensitivity to CF induced error is studied using a simple model for charge injection in the basic memory cell. All is made at a behavioral level oriented to a rapid design validation before going to the physical realization, but with models which are related to this physical realization. The developed models have been introduced in WAVER, an in-house program we use to design SI wave analog filters. The simulation results obtained for a low-pass third-order filter will be presented.

REALIZATION OF SWITCHED-CURRENT WAF

Let us consider the implementation of a third order low-pass filter. The Wave Model shown in Figure 1 is one of the models we can use to realize the filter. The signals A_{ij} and B_{ij} represent the incident and reflected wave signals in the j
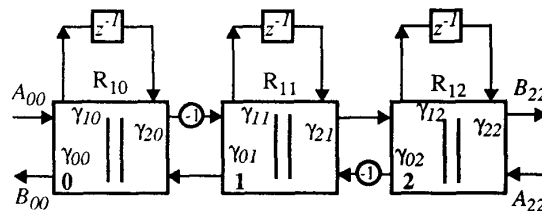

Figure 1: Third order low-pass wave filter.

adaptor. The coefficients γ_{ij} must be determined taking into account the following relationships

$$\sum_{i=0}^{2} \gamma_{ij} = 2 \quad , \quad R_{0j}\gamma_{0j} = R_{1j}\gamma_{1j} = R_{2j}\gamma_{2j} \quad (1)$$

where the port resistance R_{20} and R_{21} can have any value and the other resistances are obtained from the LC reference filter and the sampling frequency [4].

Equations for the 3-port parallel adaptor operation are

$$B_j = A_N - A_j \quad , A_N = \gamma_0 A_0 + \gamma_1 A_1 + \gamma_2 A_2 \quad (2)$$

with $j=0,1,2$. Switched-current implementation of the filter consists of the interconnection of current mode adaptors and unit delay cells. Note that any reflection coefficient γ_{ij} is realized as a current mirror gain. The schematic in Figure 2 is

a simplified version. Using high-swing cascode current mirror (Fig. 3) input-output coupling impedances effects can be reduced.
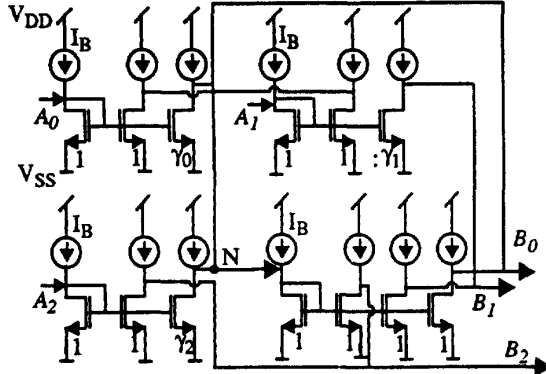

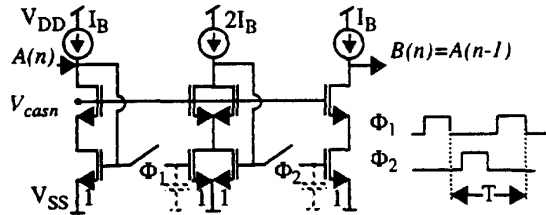Figure 2: Simplified schematic for a 3-port parallel adaptor.

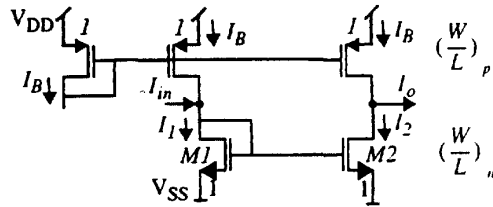Figure 3: Simplified schematic for a delay cell.

Figure 4: Basic current mirror. .

MODEL FOR MISMATCHING ERRORS

To study transistor mismatch effects in the operation of the proposed adaptors we have used the model given in [7] for the random variations in current mirror gains produced by the variations in the fabrication process. For the simple current mirror in Figure 4, the relative variance in the error between the current I_2 and the input I_1 is calculated. If unit transistor cells are used, systematic error due to ΔW and ΔL can be reduced, leading to the expression for random mismatching errors

$$\frac{\sigma_n^2(I_2)}{I_2^2} = \frac{K_{In}}{2W_nL_n} \cdot (\frac{1}{N_1} + \frac{1}{N_2}) \qquad (3)$$

where N_1 and N_2 are the number of unit cells in $M1$ and $M2$ [8]. From the technology parameters in [7], and using (W/L)₁=(60μm/10μm) and $(V_{GSn}-V_{Tn})=0.6V$, the error evaluated by (3) is about 0.28%. To obtain the variance in the out-

put currents of any adaptor, we define the relative variance in the unit-gain current mirror as

$$\sigma_n'^2(1) = \frac{\sigma^2(I_2)}{I_2^2} = \frac{K_{In}}{W_nL_nN_1} \qquad (4)$$

Regarding the ratio I_o/I_{in}, mismatching in the NMOS mirrors lead to offset and gain errors, given by

$$\sigma_{n,off}'^2(I_o) = \sigma'_n(1) \cdot I_B^2 \qquad (5)$$

$$\sigma_{n,gain}'^2(I_o) = \sigma'^2_n(1) \qquad (6)$$

Errors from the PMOS bias transistor generate only offset in I_o,

$$\sigma_{p,off}'^2(I_o) = 2\sigma'^2_p(1)I_B^2 \qquad (7)$$

where $\sigma'_p(1)$ has been define as (4) for a PMOS current mirror. Taking (W/L)ₚ=(100μm/10μm) and $(V_{GSp}-V_{Tp})=0.5V$, the error evaluated by (5) for PMOS transistor is about 0.3%. Global mismatching error contribution can be obtained adding equations (5) to (7).

The variance associated to the actual realization of each filter component (delay cells and adaptors) can be evaluated as follows. First, determine the number of current mirrors and their respective gains in the path from each input to one output. Second, assuming the mismatching error in each mirror modelled as a gaussian distributions which is not correlated with the error in other mirror, add all errors in each input-output path.

Using this procedure, the gain and offset variance in the cascade of two unity-gain current mirrors are given by

$$\sigma_{gain}'^2(2) = 2\sigma'^2_n(1) \qquad (8)$$

$$\sigma_{off}^2(2) = (4\sigma_p'^2(1) + 2\sigma_n'^2(1)) \cdot I_B^2 \qquad (9)$$

which can be used to evaluate the error in unit delay cells, $\sigma^2(z^{-1}) = \sigma^2(2)$. For the case above (8) and (9) give a 0.4% gain error and 73nA random offset.

The statistic model corresponding to the 3-port parallel in Fig 2 is obtained in the same way, resulting in a gain variance matrix error with entries given as,

$$[\sigma'^2_{ij}]_{gain} = \frac{\sigma'^2_n(1)}{2} \cdot \begin{cases} 5 + 1/\gamma_i & if \quad i = j \\ 3 + 1/\gamma_j & if \quad i \neq j \end{cases} \qquad (10)$$

From (10) it can be seen that mismatching errors are more important when γ approaches zero. This effect can be taken into account in the design phase by implementing low-valued coefficients with an arrangement of current mirrors whose total gain is given by $(1+\gamma)-1$. Thus, alternative matrix entries of $(9+1/(1+\gamma))$ or $(7+1/(1+\gamma))$ appear. This solutions means a penalty area. As illustration, let us consider the matrix variance corresponding to the first adaptor in Figure 1(b), for the particular values γ₀=0.3 γ₁=1.187 and γ₂=0.513, form (10) we obtain

$$[\sigma'^2_{ij}]_{gain} = \begin{bmatrix} 0.57 & 0.39 & 0.44 \\ 0.50 & 0.48 & 0.44 \\ 0.50 & 0.39 & 0.52 \end{bmatrix} \qquad (11)$$

which means that the maximum standard deviation corresponds to the (γ_0-1) gain, and it is equal to 0.57%. The matrix for output offset errors is given by,

$$[\sigma'^2_j]_{off} = \frac{4\sigma'^2_p(1) + 2\sigma'^2_n(1)}{2} I^2_B \left(7 + \sum_{j=0}^{2} \frac{1}{\gamma_j}\right), \forall j \quad (12)$$

As before, for small coefficients realized as $(1+\gamma)$-1, the number 7 and γ in (12) must be changed for (7+4) and $(1+\gamma)$, respectively. The offset for the example presented is 186nA. The same can be done for all adaptors in the filter.

CLOCK-FEEDTHROUGH INDUCED ERRORS

Clock-feedthrough in current track-and-hold (T/H) can be modelled by an error voltage on the data holding node. It causes DC offset, gain error and distortion. Although additional circuitry for cancellation of the CF errors is always used, total cancellation is not reached in practice. We have introduced a simple analytical model to study the effects of this error in the global performance of the filter. Assuming a voltage error Δv_f in the holding node, the equation including CF effects will be for the unit delay cells

$$\Delta I_o = \Theta \left(\sqrt{I_B + I_{in}} - \sqrt{(I_B - I_{in}) - \frac{\Theta^2}{4} - \Theta\sqrt{I_B + I_{i}}}\right) (13)$$

where ΔI_o represents the output current error evaluated at the nT instant, I_{in} the input current at the $(n-1)T$ instant and $\Theta = \sqrt{\beta_n}\Delta v_f$. In order to find a linear model for CF error, (13) can be approximated as

$$I_o = b_0 + b_1 \cdot I_{in} + b_2 \cdot I^2_{in} + ... \quad (14)$$

where only the two first terms in RHS are taking into account for a linear model.

SIMULATION RESULTS

Errors can be introduced in numerical simulations performed by WAVER using the computation expressed as $I_o = I_{in}(\gamma^p + \Delta \gamma^p) + I_{off}$, in which the ideal output, $\gamma^p I_{in}$, is modified by an error gain $\Delta \gamma^p$ and added to an offset term, I_{off}. We have performed a Monte Carlo analysis of the filter in Figure 1 with the nominal adaptor coefficients given in Table I corresponding to a normalized cutoff-frequency of 0.09577 and a passband ripple of 0.2 dB, using $I_B=10\mu A$ and 10μm/10μm unit transistors. Mismatching errors are randomly generated using the standard deviations derived from (8) and (9) for the delay cells, and from (10) and (12) for the parallel adaptors. CF errors are included given a value to Δv_f. For the characterization of the filter, we have measured the parameters defined in Table II.

Table I: Three-port adaptor coefficients

γ_{00},γ_{22}	γ_{10},γ_{12}	γ_{20},γ_{02}	γ_{01},γ_{21}	γ_{11}
0.3	1.187	0.513	0.239	1.521

Table II: Statistical filter parameters definition. (ε) ripple, (ω_0) cutoff-frequency, (H(0)) DC level and (H(0.5)) Niquist level.

ε_{mean}	$\frac{1}{N}\sum_{n=1,...,N}(H_{max}-H_{min})_n$
ε_{std}	$\frac{1}{N}\sum_{n=1,...,N}(\varepsilon^2_n - \varepsilon^2_{mean}))^{1/2} \times \frac{100}{\varepsilon_{mean}}$
$\omega_{o_{mean}}$	$\frac{1}{N}\sum_{n=1,...,N}\omega_{o_n}$
$\omega_{o_{std}}$	$\frac{1}{N}\sum_{n=1,...,N}(\omega^2_n - \omega^2_{o_{mean}}))^{1/2} \times \frac{100}{\omega_{o_{mean}}}$
$H(0)_{mean}$	$\frac{1}{N}\sum_{n=1,...,N}H(0)_n$
$H(0.5)_{mean}$	$\frac{1}{N}\sum_{n=1,...,N}H(0.5)$

Figure 5 shows the ideal, mean and mean±σ frequency responses obtained with N=100 and Δv_f=5mV. The results obtained for Δv_f = 0, 1 and 5mV are summarized in Table III. It can be note that the errors in the ripple and cutoff-frequency mean values due to mismatching (Δv_f = 0) are 12.2% and 0.15%, respectively, while the CF induced errors increase strongly these percentages (66.1% and 4.41% for Δv_f = 1mV, 467.2% and 16.2% for Δv_f = 5mV).

Table III: Three-port adaptor coefficients.

Δv_f [mV]	0	1	5
ε_{mean} [dB]	0.2244	0.3322	1.1344
ε_{std} [%]	11.69	16.27	8.40
$\omega_{o_{mean}}$	0.09566	0.10000	0.111291
$\omega_{o_{std}}$ [%]	1.8443	1.5434	0.8075
$H(0)_{mean}$ [dB]	0.0109	0.26169	1.3061
$H(0.5)_{mean}$ [dB]	-149.9	-149.7	-125.2

Figure 6(a) shows the effects of positive and negative gate voltage increment in the T/H cells. The corresponding experimental results are shown in Figure 6(b), which were obtained modifying the clock signal level. The displacement in the experimental filter function correspond to be the effects of the CF of opposite sign.

To exploit the freedom in the choice of adaptor coefficients inherent to WAF [6], we have also measured the effects of the ratio $k=\gamma_{20}/\gamma_{00}$ values on the error in the ripple and the cutoff frequency relative to the nominal ones. The obtained results are illustrated in Figures 7 (a) and (b), Note that there exist values of k which produce low deviations in the filter characteristics.
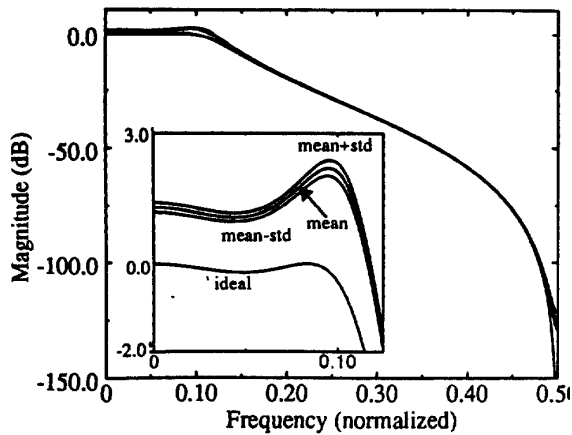
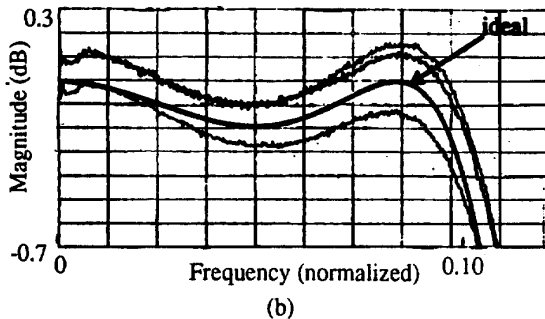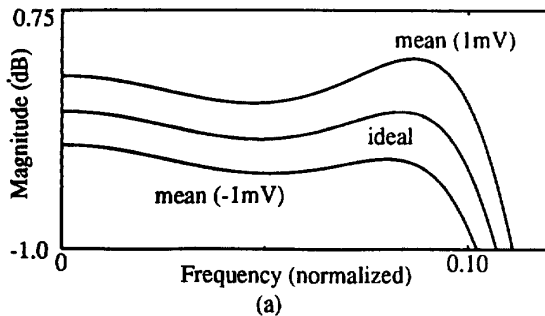Figure 5: Magnitude response obtained from Monte Carlo simulation for $\Delta v_f = 5mV$.

(a)

(b)

Figure 6: (a) Pass-Band magnitude response obtained from Monte Carlo simulation with $\Delta v_f = \pm 1mV$. (b) Experimental results for different clock signal levels.

(a)

(b)

Figure 7: Evolution of (a) ripple and (b) cutoff frequency errors for different values of $k = \gamma_{20}/\gamma_{00}$ and $\Delta v_f = 1mV$.

CONCLUSIONS

The sensitivity of SI WAF filters to the main sources of errors has been evaluated using operational models and Monte Carlo simulations. The results are close to the experimental measurements and prove that CF effects are dominants. Future work would be focused on including non-linear terms in order to obtain a whole filter characterization.
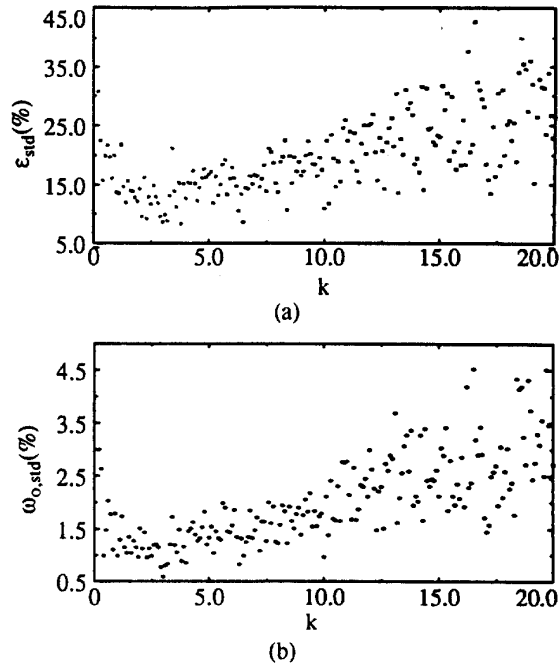
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