A 1.25V FGMOS Filter Using Translinear Circuits

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Abstract

This paper presents a new low voltage/low power filter design based on Floating-Gate *MOS* (*FGMOS*) transistors. *FGMOS* transistors are used as primitives to design linear and non-linear ($\sqrt{x}$) circuits. This technique enables a voltage reduction in strong inversion mode, and gives a new vision of the translinear principle, suitable for low voltage applications. Experimental results for a *0.8μm* Low-Pass and Band-Pass filter prototype are reported.

1. Introduction

Low Power (*LP*) and Low Voltage (*LV*) circuits are nowadays widely demanded by the market of portable applications. Filters are building blocks appearing on demanded *LP/LV* products. The general interest existing now on *LV/LP* filters is leading this field towards large-signal processing to increase linearity and dynamic range [1-7]. This paper presents a *LV/LP* filter design technique that uses state-space description and *FGMOS* [8] circuits. This technique has a promising future in the *LV* analog design because of the possibility of compressing input signal levels and implementing a weighted sum of voltages in a simple form [9-11]. We will describe the design and test of a second-order filter for audio frequency applications working at *1.25V*. The paper is organized as follows: Section 2 illustrates the modifications over the state-space equations, which lead to the filter implementation. The modified TransLinear (*TL*) principle when *FGMOS* transistors are used and the equations realization are introduced in Section 3. The developed theory will be applied to second-order filters in Section 4, reporting experimental results.

2. The State-Space Filter Equations

The time-dependent equations of any linear filter can be reduced to a set of first-order differential equations of the type,

$$\dot{x} + \alpha x = \eta x_i \qquad (1)$$

where x is a state variable, x_i is the external excitation which can be an independent signal, other state-variable or any combination of both, and parameters α and η are related with the filter specifications. For fully-differential operation, all signals (v_d) must be considered as the difference of a positive, x_p and a negative, x_n signal defined as: $x_p = x_{cm}+v_d/2$ and $x_n = x_{cm}-v_d/2$, respectively. The x_{cm} value is the common-mode level. Hence eq. (1) can be written as,

$$(\dot{x}_p - \dot{x}_n) + \alpha(x_p - x_n) = \eta(x_{ip} - x_{in}) \qquad (2)$$

For voltage signals, we introduce the variable change,

$$V_p - V_n = \frac{I_p - I_n}{K\sqrt{I_c}} \qquad (3)$$

where I_c, I_p, I_n are currents and K is a constant. By multiplying both sides in eq. (2) by C (physically an integrating capacitor), and using eq. (3), the LHS in eq. (2) can be identify as the current I through capacitor C,

$$I = C(\dot{V}_p - \dot{V}_n) \qquad (4)$$

This equation is symbolized in Fig. 1 with ideal elements.

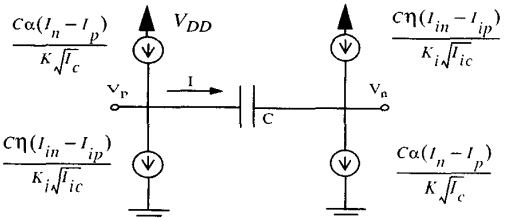

Fig.1: Ideal circuit schematic implementing the first-order state-space equations (3-4).

3. FGMOS Implementation

Here we describe the required circuits to implement the elements in Fig. 1 using *FGMOS* transistors [8]. A *FGMOS* transistor is a *MOS* transistor with isolated gate capacitively coupled to the inputs in a way that it is possible to have a weighted sum of these inputs at the floating gate (Fig. 2). In strong inversion, the drain-to-source current in saturation is,

$$I_D = \beta_n\left(\sum_{i=1,\ldots,n} w_i V_i + w_B V_B - w_S V_S - w_T V_{th}\right)^2 \qquad (5)$$

where β_n is the transconductance, V_{th} is the threshold voltage,

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and the V_i are the input-voltage for the *FGMOS* transistor. The weights in eq. (5) are defined as: $w_i=C_i/C_T$, $w_B=C_{FB}/C_T$, $w_S=[1-(C_{FB}/C_T)-2/3(C_{ox}/C_T)]$, $w_T=[1-2/3(C_{ox}/C_T)]$, being C_T the total capacitance seen from the floating gate.

In weak inversion operation, the drain-to-source current in saturation region can be written as,

$$I_D = I_s exp\left(\sum_i \frac{w_i V_i}{nU_t}\right) \tag{6}$$

where I_s is a current which depends on both technological and design parameters, U_t is the thermal voltage, n is the slope factor, and the weights are defined in the same way as in eq. (5). Equation (6) allows the use of *FGMOS* transistors in TransLinear circuits.

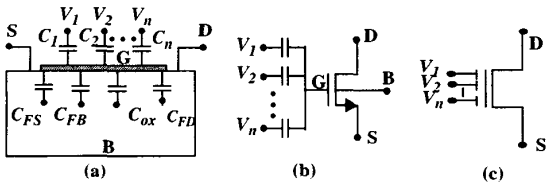

Fig.2: *FGMOS*: (a) Capacitors model. (b) Equivalent circuit. (c) Schematic.

A: Circuit for variable change.

Let's consider the circuit in Fig. 3a with three equal *FGMOS* transistors in saturation strong inversion region. The drain-to-source currents of transistors *M1* and *M2* are,

$$I_{p,n} = \beta(w_{DD}V_{DD} + wV_{p,n} - V_{th})^2 \tag{7}$$

where subscripts p and n apply to *M1* and *M2* respectively. Taking the difference between I_p and I_n gives,

$$(V_p - V_n) = \frac{(I_p - I_n)}{2w\sqrt{\beta I_c}} \tag{8}$$

representing the variable change performed over the state-space equation as defined in eq. (3). I_c is defined as the *common-mode current* derived from V_p and V_n. It senses the common-mode voltage, V_{cm}, of both voltage signals. Circuit in Fig. 3a generates, from V_p and V_n voltages, three currents I_p, I_n and I_c involved in the variable change in eq. (3). As eq. (8) represents a non-linear relationship between voltages and currents, we will refer to this circuit as a transconductor or *NG-circuit*. Its symbol is shown in Fig. 3b. Each *NG-circuit* has a large-signal differential input-voltage to differential output-current transconductance given by, $G = 2w\sqrt{\beta I_c}$, where I_c is the common-mode current. As it is demanded by eq. (8), the circuit required is an $y/\sqrt{x}$ -type operator, and can be derived using the translinear principle.

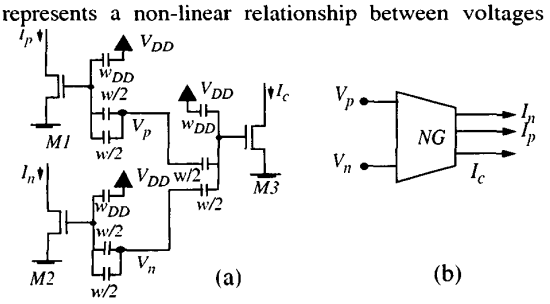

Fig.3: (a) *FGMOS* circuit for variable-change. (b) Symbol.

B: FGMOS Translinear Principle.

Let's consider two *FGMOS* transistors *M0* and *M1* with grounded source and a common input V_{0i} at *M0* and V_{1j} at *M1* (Fig. 4). The Kirchoff's voltage law in this trivial loop is:

$$-V_{0i} + V_{1j} = 0 \tag{9}$$

Expressing voltages in the *TL* loop as functions of the currents flowing through the transistors gives:

$$\begin{aligned} V_{0i} &= nU_T \ln\left(\frac{I_0}{I_s}\right)^{1/w_{0i}} - \frac{1}{w_{0i}} \cdot \sum_{k\neq i} \frac{w_{0k}V_{0k}}{nU_T} \\ V_{1j} &= nU_T \ln\left(\frac{I_1}{I_s}\right)^{1/w_{1j}} - \frac{1}{w_{1j}} \cdot \sum_{k\neq j} \frac{w_{1k}V_{1k}}{nU_T} \end{aligned} \tag{10}$$

Substituting them into equation (9) and solving, it results

$$\left(\frac{I_0}{I_s}\right)^{1/w_{0i}} e^{-\sum_{k\neq i}\frac{w_{0k}V_{0k}}{w_{0i}nU_T}} = \left(\frac{I_1}{I_s}\right)^{1/w_{1j}} e^{-\sum_{k\neq i}\frac{w_{1k}V_{1k}}{w_{1j}nU_T}} \tag{11}$$

This is a non-linear relationship between currents which is the objective of the *TL* principle. The advantage of designing *TL* loops with *FGMOS* devices is that it is possible to implement the exponents in (11) through capacitance ratios. This fact makes this transistor very useful for *LV* purposes.

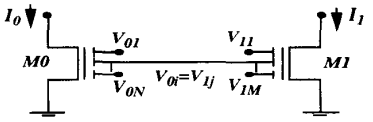

Fig.4: *FGMOS* Translinear Loop.

C: The $y/\sqrt{x}$ circuit.

The currents added in the integrating capacitor must be divided by the squared-root of I_c, or common-mode current for each pair of differential voltages. This operator can be also implemented by means of *TL* circuits [8]. In eq. (3), each RHS term follows the general form,

$$\frac{1}{K\tau} \cdot \frac{I_d}{\sqrt{I_c}} \tag{12}$$

with $\tau=\alpha^{-1}$ or η^{-1}, $K=2w\sqrt{\beta}$, and $I_d=I_p-I_n$. Multiplying eq. (2) by an integrating capacitor, and using eq.(3), gives a dimensionally correct equality,

$$\frac{C}{K\tau} = \frac{C}{2w\sqrt{\beta\tau}} \equiv A_j\sqrt{I_{Aj}} \tag{13}$$

being A_j a non-dimensional factor and I_{Aj} an independent

current. An alternative form of eq. (4) is thus obtained,

$$C(\dot{V}_p - \dot{V}_n) = -A_j\sqrt{I_{Aj}}\frac{I_d}{\sqrt{I_c}} + A_i\sqrt{I_{Ai}}\frac{I_{di}}{\sqrt{I_{ci}}} \quad (14)$$

For the implementation of this equation, two I_{Aj} currents are required, for coefficients α and η. The proposed circuit is shown in Fig. 5a. Voltage sources are employed at *FGMOS* inputs for shifting the threshold voltage and controlling the circuit gain. The corresponding output current for the circuit are now given by the equation,

$$I_{on/op} = A_j\sqrt{I_{Aj}}\cdot\frac{I_{n/p}}{\sqrt{I_c}} \quad (15)$$

where A_j depends on the constant reference voltage sources placed at the input of the transistors. For equal total capacitance for any *FGMOS* transistor, and for all voltages sources equal to V_{DD}, (except V_{Aj}), the A_j constant is given by,

$$A_j = e^{(V_{Aj}-V_{DD})/4nU_t} \quad (16)$$

where the independent voltages are chosen to ensure weak inversion operation and V_{Aj} is selected for A_j-tuning. This gives us a design relationship between the state-space equation coefficients, the selected integrating capacitor, and the floating-gate circuits:

$$\frac{C}{2w\sqrt{I_{Aj}}\sqrt{\beta}}\cdot e^{-(V_{Aj}-V_{DD})/4nU_t} = \tau \quad (17)$$

Negative $I_{on/op}$ values are implemented with current mirrors.

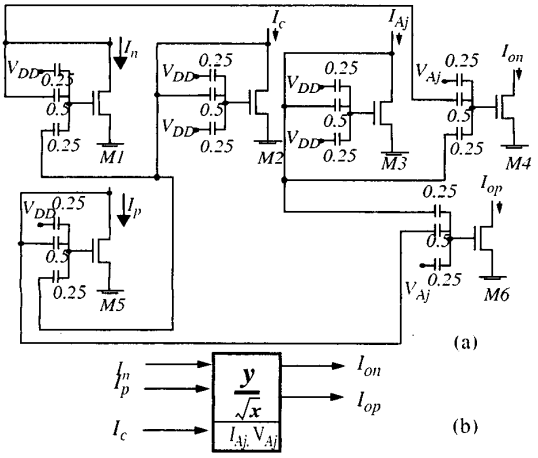

Fig.5: (a)$y/\sqrt{x}$ circuit based on *FGMOS TL* loops.(b) Symbol.

D: The transconductor

The circuit for implementing each term in the state-space equation is shown in Fig. 6. It realizes a linear relationship between the output current I_{on}-I_{op} and the differential voltage V_p-V_n, so it fits to a linear transconductor description. Its transconductance is given by:

$$g_m = C/\tau = 2wA_j\sqrt{\beta I_{Aj}} \quad (18)$$

The value of g_m can be adjusted by mean of an external current or external voltages through A_j and I_{Aj} values.

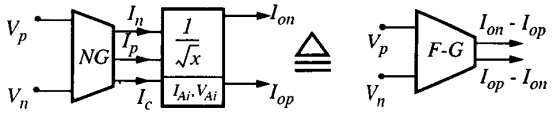

Fig.6: The *FGMOS* transconductor (*F-G*).

4. A Second-Order Filter

The design procedure exposed in section 3 has been used to implement a second order filter. The specifications of the filter are in the audio frequency range. The power supply is below *1.25V*, in a *0.8*μm *CMOS* process with threshold voltages of V_{tn}=*0.8V* and V_{tp}=*-0.82V*. The starting point for the design are the equations,

$$\dot{x}_1 = -\omega_{o1}x_1 - \omega_{o2}x_2 + \omega_{o3}x_i \quad (19)$$

$$\dot{x}_2 = \omega_{o2}x_1 \quad (20)$$

Three parameters have been taken in order to increase filter programmability. The ω_o and Q of the second-order filter are given by,

$$\omega_o = \omega_{o2},\ Q = \omega_{o2}/\omega_{o1} \quad (21)$$

and the maximum gains,

$$H_{LP}(0) = \omega_{o3}/\omega_{o2},\ H_{BP}(\omega_o) = \omega_{o3}/\omega_{o1} \quad (22)$$

The circuit implementing equations (19-20) is shown in Fig. 7, where,

$$H_{LP}(0) = H_{BP}(\omega_o) = \sqrt{\frac{I_{A3}}{I_{A2}}}\cdot\frac{A_3}{A_2} \quad (23)$$

$$\omega_o = \frac{2w\sqrt{\beta}}{C}\cdot A_2\cdot\sqrt{I_{A2}} \quad (24)$$

$$Q = \sqrt{\frac{I_{A2}}{I_{A1}}}\cdot\frac{A_2}{A_1} \quad (25)$$

Tuning of ω_o and Q can be performed through either the reference voltages or the independent current sources, the ω_o frequency will be constant if V_{A2} is not changed, while Q can take some values depending on I_{A1} or V_{A1} values. Outputs of this circuit can be currents I_1 and I_2 through both capacitors or the differential voltage across them.

Filter parameters in eqs. (21-22) can be controlled by design equations (23-25). A value of *3.4pF* for capacitors has been used. For the *NG-circuits* we have chosen β=*30.7*μ*A/V*^{2}, for *M1-M3 FGMOS* transistors in Fig. 3, and *50fF* and *100fF* for input capacitors with weight *0.25* and *0.5*, respectively. Fig. 8 (illustrates the obtained *LP* and *BP* transfer functions. Fig. 9 shows the Q and gain programming for both transfer functions. The distortion for the *LP*-function with a cut-off frequency of *2KHz* can be observed in Fig. 10, for a sinusoidal input signal of *200Hz*. The maximum value is *41dB* for half range of the power supply. The *IM3* parameter for the *BPF* is below *40dB* when both input signals have amplitudes smaller

than *0.5V*. It has been also measured the performance of the filter when the input common-mode change. The *CMR* measured is of *0.6V*. Performance results are summarized in Table1.

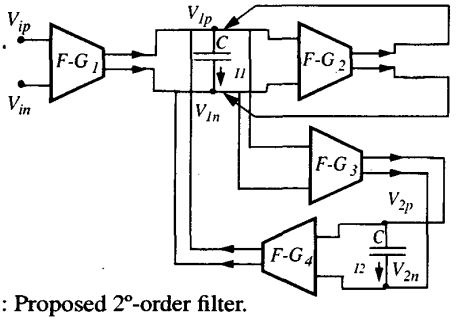

Fig.7: Proposed 2°-order filter.

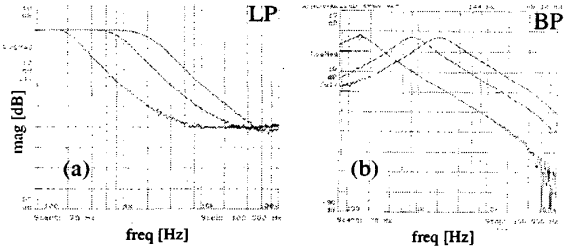

Fig.8: Experimental *LP* and *BP* filter responses.

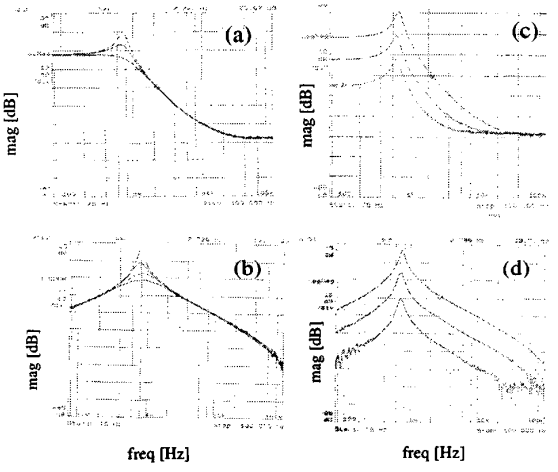

Fig.9: *Q*-tuning. for *LP* (a) and *BP* (b) functions. *Gain*-tuning. for *LP* (c) and *BP* (d) functions for f_o= *0.75KHz*.

5. Conclusions

A new *LV/LP* band pass/low pass biquad realization has been proposed. The design shows the feasibility of the *FGMOS* devices to scale down the power supply either in weak inversion or in strong inversion operation modes. A *1.25V* filter prototype have been tested which exhibits a quite large dynamic range, more than one decade tuning rate and a power consumption of a few microwatts.

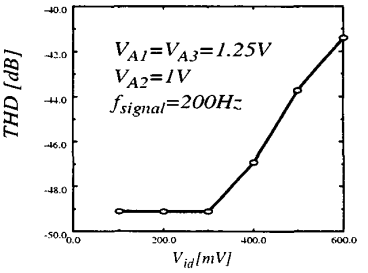

Fig.10: *THD* versus differential input amplitude.

Table 1: Summary of the 2°-order filter performance.

Power Supply	*1.25V*
Area	*0.23mm²*
f_o	*100Hz - 2KHz*
Q	*0.75 - 7*
THD_{max} (V_{pp}<*1V@200Hz*, *Q=1*, $H_{LP}(0)=1$, f_o=*900Hz*)	*< 40dB*
IM3 ($V_{pp1}=V_{pp2}$<*0.5V@200Hz*, *Q=1*, $H_{LP}(0)=1$, f_o=*900Hz*)	*< 40dB*
Noise in band	*-75dB*
DR (@1%THD)	*78 - 62 dB*
Power	*2.5 µW*

6. References

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