Four-channel self-compensating single-slope ADC for space environments

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A multichannel high-resolution single-slope analogue-to-digital converter (SS ADC) is presented that automatically compensates for process, voltage and temperature variations, as well as for radiation effects, in order to be used in extreme environmental conditions. The design combines an efficient implementation by using a feedback loop that ensures an inherently monotonic and very accurate ramp generation, with high levels of configurability in terms of resolution and conversion rate, as well as input voltage range. The SS ADC was designed in a standard 0.35 μm CMOS technology. Experimental measurements of the performance and stability against radiation and temperature are presented to verify the proposed approach.

Introduction: Single-slope analogue-to-digital converters (SS ADCs) are widely used in many multichannel data acquisition applications by implementing parallel readout architectures. The ramp generator is a key element in this conversion scheme, given the direct relationship between its performance and the ADC transfer characteristic. When medium to high resolutions are the aim, process, voltage and temperature (PVT) and ageing variations can limit the accuracy of the SS ADC. Moreover, in space environments, circuits are required to operate in an extended temperature range and also to deal with the total ionising dose (TID) radiation effects that degrade the DC and AC performance characteristics with a gradual change with time [1]. All of these effects can produce variations in the slope of the ramp, which critically affects the performance of the overall SS ADC. This is illustrated in Fig. 1.

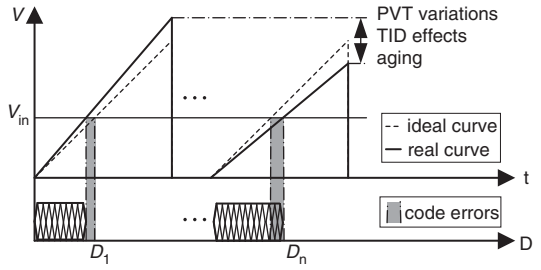

Fig. 1 *Output code errors due to variations in slope of ramp*

Several approaches, mostly based on calibration techniques, are reported in the literature [2–4] in order to improve the stability of the SS ADC. This Letter proposes a simpler alternative based on an adaptive feedback loop that provides an inherently monotonic ramp generation with high levels of stability as well as high levels of scalability in terms of resolution and input voltage range. A four-channel SS ADC following this approach has been designed in a 0.35 μm CMOS technology, in order to be applied for space applications, more specifically for payload sensors' temperature measurements for missions to Mars.

Proposed architecture: The circuit description of the proposed SS ADC is shown in Fig. 2. The resolution is configurable between 10 and 15 bit. The input voltage range is also configurable by independently setting both the initial and final reference voltages of the ramp excursion with values between 0 and 2.8 V with increments of 200 mV. The architecture consists of a ramp generator shared by four self-biased comparators, a finite state machine (FSM) that controls the operation of the ADC and a reference voltage generator to set the input voltage range. An integrator driven by an NMOS transistor acting as a voltage-controlled current source implements the ramp generator. The generation of the ramp is controlled by a feedback loop composed of a capacitor (C_f) and two pairs of switches. The feedback loop modifies the end value of the ramp, towards the reference voltage (V_{ref_last}), by regulating the input voltage of the current source, in turn modified according to the difference (V_ε) between the actual final value of the ramp and V_{ref_last}. Thus, after starting up the ADC, several cycles of adaption are needed until the ramp is fully adapted and reaches the reference end value. This is illustrated in Fig. 3.

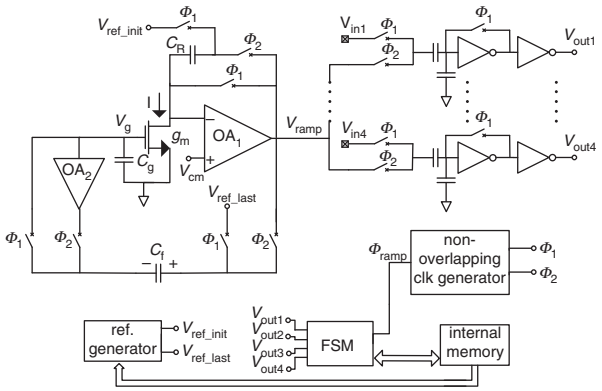

Fig. 2 *Circuit description of proposed SS ADC*

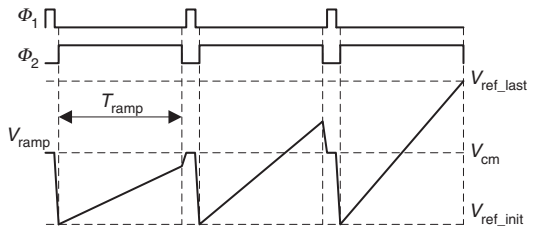

Fig. 3 *Time diagram of operation of ramp generator with feedback loop until ramp is adapted*

The generation of the ramp is divided into two phases. During the first phase, ϕ_1, the feedback network determines the error voltage (V_ε), used to adapt the value of the gate voltage of the current source (V_g) for the next phase, the capacitance of the integrator (C_R) is reset, the comparators are in the reset phase and the output of the ramp generator is driven to an intermediate reference (V_{cm}). During the second phase, ϕ_2, the comparators are in the active phase and the integrator generates the ramp signal starting from V_{ref_init} with a driving current value that depends on the voltage V_g used in the previous phase. An opamp in a follower configuration (OA_2) is used to prevent the discharge of capacitor C_g during this phase. After several cycles of adaption, the error voltage V_ε is ideally zero and the range of the ramp signal is established between V_{ref_init} and V_{ref_last}.

For each cycle, the increments of voltage in the final value of the ramp can be expressed as

$$\delta V_{ramp\_end} = \frac{g_m \cdot T_{ramp}}{C_R} \cdot \frac{C_f}{C_f + C_g} \cdot (V_{off\,2} - V_\varepsilon) \tag{1}$$

where $V_{off\,2}$ is the offset voltage of the opamp OA_2. A constant transconductance g_m is assumed for simplicity. When the ramp generator is fully adapted, δV_{ramp_end} becomes zero, and using (1) shows that the error in the final value of the ramp voltage with respect to its goal value is reduced to the offset voltage of the opamp OA_2. This fixed minor error is generally acceptable, but offset correction schemes are possible and may be implemented when required. The stability of the feedback loop can be analysed in the Z domain. System poles are independent of the specific output or input considered, allowing us to consider the following transfer function [5]:

$$\frac{V_\varepsilon(z)}{V_{off\,2}} = \frac{\alpha \cdot z}{z - (1 - \alpha)}; \quad \text{with } \alpha = \frac{g_m \cdot T_{ramp}}{C_R} \cdot \frac{C_f}{C_f + C_g} \tag{2}$$

Equation (2) shows that the feedback loop will be stable if $|1 - \alpha| < 1$. This condition implies a design compromise between adaptation speed and loop stability, as usual. Weak inversion is a good choice for the operation of the current-source transistor, given the proportionality between transconductance and current in that region, which yields the condition independent of T_{ramp} and therefore invariant with the programmed resolution of the ADC. Temperature and ramp excursion do have an effect on the stability condition and must be considered in the design process. A close to optimal design of the ramp generator, with

a sufficient margin of stability while ensuring a short adaptation-time of few cycles, has been obtained with a capacitors ratio of $C_g \simeq C_R \simeq 150 \times C_f \simeq 20$ pF. The current-source transistor operates in moderate inversion, close to weak inversion ($W = 11$ μm, $L = 20$ μm). The adaptive nature of this ramp generation provides high levels of stability, limited only by the reference voltages that define the ramp excursions, as usual in most conversion circuits. A low drop-out internal voltage regulator, driven by a bandgap circuit, is used to generate the internal supply voltage (3 V) and the ramp reference voltages, making them independent of the external power supply (3.3–5.5 V).

The resolution of the ADC is determined by the time duration of phase $\phi_2(T_{ramp})$. This signal is easily generated in the FSM including a digital counter. This provides a good level of scalability with resolution, as the only hardware that must be scaled is the digital counter. The internal clock frequency, generated by a simple relaxation oscillator, is also configurable between 25 and 100 MHz.

Experimental results: A four-channel SS ADC following this approach has been designed and fabricated in a 0.35 μm CMOS technology. As the ASIC has been designed for on-board space applications using a standard CMOS technology, previous technology characterisation was required [6]. The area of the full ADC is 590×3400 μm^2, and the power consumption is 7.8 mW. Area and power consumption restrictions were not severe. Reliability is the first goal, and therefore radiation hardened by design techniques were used. These included the use of ringed-source layouts for every NMOS transistor for TID effects improvements. PMOS devices use a standard layout. Concerning single event latchup, complete guard-rings have been used around every transistor. All registers are redundant and one-hot encoding was used to implement the FSM. Table 1 shows the experimental performance of the SS ADC at room temperature, for a clock frequency of 100 MHz, and for the maximum input voltage range (0–2.8 V).

Table 1: Experimental performance summary

Resolution	10 bit	11 bit	12 bit	13 bit	14 bit	15 bit
Conv. time (μs)	13	23	43	84	166	330
INL	+0.42	+0.20	+0.28	+0.99	+3.90	+14
	−0.48	−0.33	−0.34	−0.92	−3.10	−9.6
DNL	+0.05	+0.13	+0.18	+0.27	+0.36	+0.49
	−0.04	−0.08	−0.23	−0.24	−0.28	−0.40
Root-mean-square noise	0.01	0.5	0.5	0.5	0.88	1.82

Results in LSBs

Temperature tests have been performed in order to check the stability of the slope of the transfer characteristic of the SS ADC. Fig. 4 shows the percentage deviation of the slope against temperature with respect to the nominal case at 25°C. The percentage deviation of the internal bandgap voltage is also shown. As can be seen, the total deviation of the transfer characteristic is $< 0.8\%$ and correlates with the variation of the reference voltage of the bandgap, meaning that the adaptive loop is working correctly.

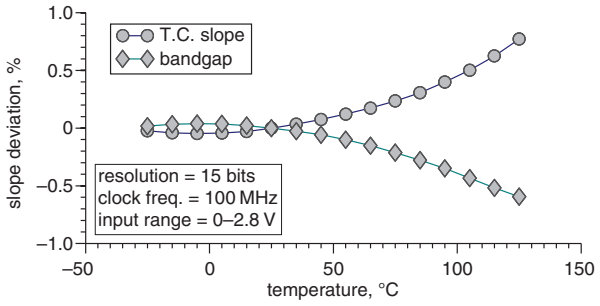

Fig. 4 *Slope deviation of transfer characteristic with temperature*

To check the robustness and stability against TID effects, irradiation tests were performed using a Co-60 gamma-ray source in the facilities of the Centro Nacional de Aceleradores (CNA-CSIC, Spain). The dose rate was 215 rad/h, with a final total dose of 100 krad. After irradiation tests, there was no significant change in the performance with respect to the results in Table 1. Fig. 5 shows the slight deviation of the slope of the transfer characteristic of the SS ADC against TID with respect to the non-irradiated nominal case.

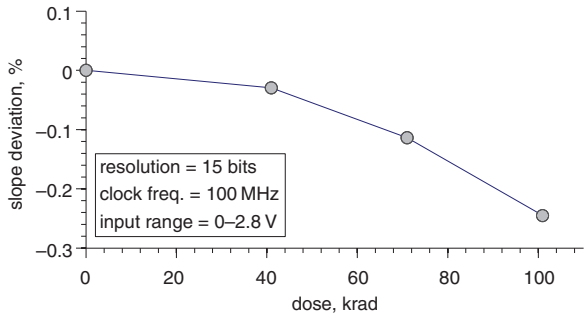

Fig. 5 *Slope deviation of transfer characteristic with TID*

Conclusion: A four-channel SS ADC with a self-compensating scheme, based on an adaptive feedback loop for the ramp generation, is proposed for space environments as a simpler alternative to calibration techniques. The performance of the loop is independent of the programmed resolution, which allows a better scaling with resolution, as the only hardware that must be scaled is the digital counter. Besides the resolution, the input voltage range is also configurable up to the widest range (0–2.8 V). Experimental results show that the proposed SS ADC is always monotonic with high levels of linearity and stability against temperature and TID variations. The stability of the transfer characteristic of the proposed SS ADC is limited only by variations in the bandgap reference voltage that defines ramp excursions.

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One or more of the Figures in this Letter are available in colour online.

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