Review of ADCs for imaging

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ABSTRACT

The aim of this article is to guide image sensors designers to optimize the analog-to-digital conversion of pixel outputs. The most common ADCs topologies for image sensors are presented and discussed. The ADCs specific requirements for these sensors are analyzed and quantified. Finally, we present relevant recent contributions of specific ADCs for image sensors and we compare them using a novel FOM.

Keywords: ADC, image sensors, analog-to-digital conversion, read-out topologies for image sensors, ADC review.

1. INTRODUCTION

The analog-to-digital conversion of pixels outputs is a very important process that affects the image quality, the frame rate, or it can even impose restrictions to the imager layout. Vision sensor designers are not usually experts in the design of analog-to-digital converters. On the other hand, ADCs designers are sometimes not aware of the special requirements than ADCs have to satisfy for pixel output digitization. General purpose ADCs are not suitable for commercial image sensors. Some of their specifications can be oversized leading to unnecessary power or area consumption. On the contrary, if they do not achieve some of the imager requirements for the signal digitalization, they will degrade the image quality. This document is organized as follows: Section.2 compares the different read-out topologies usually employed with image sensors. The special requirements of ADCs are presented and qualified in Section.3. Finally, an overview and a comparison of the performance of recent relevant ADCs for image sensors is provided.

2. ADCS TOPOLOGIES

In this section we are going to discuss the different topologies[1] to digitize pixel outputs. We will study how the conversion speed can be increased by adding more than one ADC per pixel array.

2.1 Global ADCs

The traditional approach was to use a single ADC per sensor. All the pixels outputs were time multiplexed to the input of a global ADC to provide a digital output. The analog-to-digital frequency conversion of an entire frame, f_{conv}, is given by the following equation:[1]

$$f_{conv} = \left[M \cdot N \cdot \left(\tau_{ADC} + \tau_{RO} \cdot \frac{n_{bits}}{n_{parallel}}\right)\right]^{-1} \quad (1)$$

where M and N are the number of pixels per row and column respectively, τ_{ADC} is the ADC sampling time ($\tau_{ADC} = 1/f_s$), τ_{RO} is the time required to send one bit out of the chip, which depends of the master clock frequency, n_{bits} is the number of bits per sample, and $n_{parallel}$ is the number of parallel digital outputs. The ADC usually was integrated on chip to maximize the frame rate and reduce the FPN.

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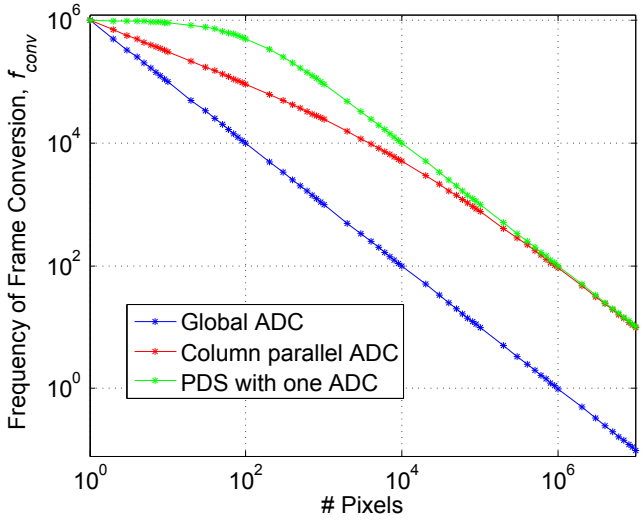

Figure 1. Frequency of conversion for different ADC topologies: global ADC, column parallel ADCs, and pixel level ADCs.

2.2 Column parallel ADCs

The demand of commercial sensors with high resolution and high frame rates requires to reduce significantly the time dedicated to read out the pixel outputs. Under these requirements, global ADCs are not practical and have been deprecated during the last years. Obviously, by increasing the number of ADCs working in parallel with different groups of pixels, the frame read-out time will be reduced.

For simplicity, by placing one ADC per column, all the pixels of one row can be sampled and read out simultaneously. This approach has a twofold benefit: the frame read-out speed is increased significantly and the requirements for the conversion time are less restrictive. The frequency of the frame analog-to-digital conversion is almost M times faster:

$$f_{conv} = \left[M \cdot N \cdot \left(\frac{\tau_{ADC}}{M} + \tau_{RO} \cdot \frac{n_{bits}}{n_{parallel}} \right) \right]^{-1} \tag{2}$$

The main challenges are the area requirements for the ADC. The ADC width should be lower than the pixels pitch. The power consumption should be low because the number of ADCs will be increased significantly. Another issue to take into account with multiple ADCs per sensor is the output data flow. We should have circuitry to store and send out all the ADCs outputs. External devices connected to our sensor should also be able to digest the output bit stream.

2.3 Pixel-level Analog-to-digital Conversion

Some authors[2–4] propose digital pixel sensors (DPS) with integrated ADCs into each pixel. The DPS performance takes advantage of the CMOS scaling-down properties. The idea is simple: each pixel has a dedicated ADC and provides an independent digital output, increasing considerably the read-out speed. In this case, the conversion frequency is given by

$$f_{conv} = \left[\tau_{ADC} + \tau_{RO} \cdot M \cdot N \cdot \frac{n_{bits}}{n_{parallel}} \right]^{-1} \tag{3}$$

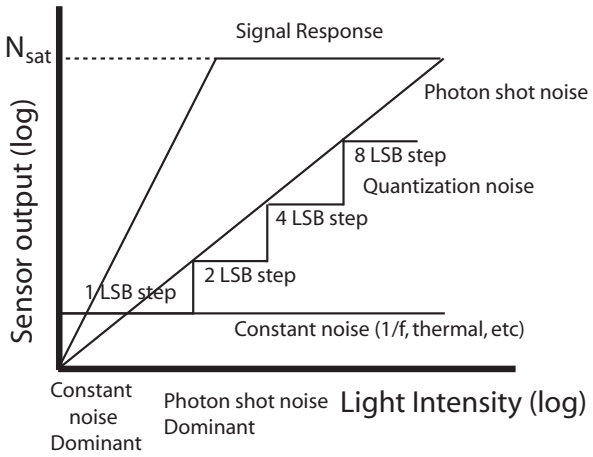

Figure 2. Illustration of how shot-noise can be exploited to relax the ADC quantization noise specifications.[5]

Although the conversion speed is higher, there are important drawbacks. This method reduces the pixels fill factor. It also requires massive parallel circuitry capable of reading the large amounts of data.

Fig.1 compares f_{conv} for the three different read-out topologies for different array sizes ($M \cdot N$). We assume for the computation that, $M = N$, $\tau_{ADC} = 1\mu$s, $\tau_{RO} = 10$ns, and $n_{bits} = n_{parallel} = 12$. These values correspond to standard modern ADC features (see Section.4 for more details). The value of f_{conv} is always higher using multiple ADCs. For arrays with a low number of pixels, the DPS topologies achieve the highest speed. However, for large pixel arrays, this topology offers the same performance that the column parallel topology. For this reason, DPS are usually aimed for high speed image sensors applications with low resolution arrays.

2.4 Future integrations

The development of 3D technologies with stacked and interconnected dies opens new possibilities to increase the read-out speed without reducing the fill factor. One entire die (tier) could be dedicated for the ADCs design. Ideally, the photo-active area could be placed on the top or the bottom (backside illumination) level and ADCs could be placed below/above it. In such topology, f_{conv} is given by,

$$f_{conv} = \left[M \cdot N \cdot \left(\frac{\tau_{ADC}}{N_{adc}} + \tau_{RO} \cdot \frac{n_{bits}}{n_{parallel}} \right) \right]^{-1} \quad (4)$$

where N_{adc} is the number of ADCs on the bottom tier.

3. ADC REQUIREMENTS FOR IMAGE SENSORS

ADC designers are usually concerned about resolution, speed, and power. As we will discuss, an ADC for image sensors does not need to satisfy strict requirements, but it is desirable to optimize its design to save area and power consumption while maximizing the conversion speed.

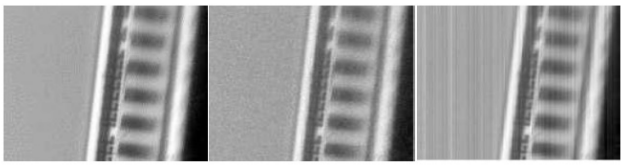

Figure 3. FPN effect on image quality.

3.1 ADC resolution

The first question that we can try to answer is how many grey levels can our eye visualize. The DICOM standard sets a maximum of 450 grey levels for display representation. This means that 9 effective bits resolution is enough for an ADC conversion of the pixel outputs. This is not a very restrictive ADC resolution requirement, taking into account the average bit resolution of the reported ADCs currently. ADCs for image sensors usually employ 10 or more effective bits. The photon shot-noise of image sensors can even be exploited to relax the requirements of quantization noise introduced by ADCs depending on illumination values,[5] as is shown in Fig.2.

3.2 Random noise

Another feature to take into account is the random noise introduced by the converter. It can be expressed in volts, but image sensor designers usually express it in e^- related to the full well capacity of the vision sensor. Random noise provokes column fixed-pattern noise (FPN). This is a mismatch introduced by the different column ADCs in a column parallel read-out topology. If the different ADCs connected to each column introduce mismatch, we will perceive column variations of the grey levels when the array is illuminated with uniform illumination. As previously mentioned, humans can detect 0.5% change in mean intensity.[6] Fig.3 illustrates the effect of FPN in a column parallel read-out topology.

3.3 Area

The area requirements are restrictive for image sensors. If we employ one ADC per column, the ADCs pitch must be equal or lower than the pixel pitch. This limits in many cases the type of ADC that we can use. Nowadays we can find very fine pixel pitches below 1µm in commercial image sensors.

3.4 Speed

The speed of the analog-to-digital conversion is an important parameter to consider. The ADC sampling frequency, $f_s = 1/\tau_{ADC}$, should be higher than:

$$f_s \quad > \quad \frac{1}{N_{ADC}\left(\frac{FR}{N_{pixels}} - \tau_{RO}\cdot\frac{n_{bits}}{n_{parallel}}\right)} \tag{5}$$

Where FR is the target frame rate, N_{ADC} is the number of ADCs shared by all the pixels, τ_{RO} is the amount of time to send one bit out the chip, and $n_{parallel}$ is the number of digital outputs. Nowadays, for high resolution image sensors usually $N_{ADC} > 1$. The maximum speed can be achieved when an ADC per pixel is implemented. Therefore, there is a trade-off between read-out speed, pixel complexity, and output sensor throughput.

3.5 Power Consumption

Since most of image sensors are used in mobile devices, power consumption has become an important drawback. Nowadays the dominant component of energy dissipation in CMOS image sensors with column-parallel ADCs is ADC conversion followed by output read-out.[7,8] Hence, there is a trade-off between conversion speed and consumption. Power consumption in CMOS image sensors increases at least linearly in resolution and frame rate.

Reference	ADC type	Resolution	Random Noise	Pixel Pitch	Power Consumption	f_s	FOM
[9]	SAR	14b	$2.8e^-$ (100µV)	4.2µm	41µW (DC)	3.5MS/s	$1.2e^{-6}$
[7]	Cyclic	13b	$2.5e^-$ (153µV)	5.6µm	300µW	19.2MS/s	$9.15e^{-6}$
[10]	Cyclic	17b	$1.17e^-$ (21µV)	7.1µm	ND	31.15KS/s	$1e^{-4}$
[11]	SAR	10b	ND	2.25µm	41µW	0.56MS/s	$2e^{-4}$
[12]	S. Slope	12b	$1.1e^-$ (121µV)	1.4µm	100µW	31.7KS/s	$2e^{-4}$
[13]	Cyclic	13b-19b	$1.2e^-$ (80µV)	7.5µm	436µW	1.5-2.3MS/s	$2e^{-4}$
[14]	SAR	11b	527µV	7µm	209µW	0.83MS/s	$3.2e^{-4}$
[15]	SAR	10b	240µV	10µm	35.46µW	240KS/s	$3.5e^{-4}$
[8]	ΣΔ	12b	$1.9e^-$	2.25µm	148µW	0.14MS/s	$7e^{-4}$
[16]	ΣΔ + cyclic	14b	ND	3.9µm	ND	0.125MS/s	0.0017
[17]	S. Slope	12b	ND	2.97µm	ND	0.13MS/s	0.0038
[18]	S. Slope	13b	ND	2.5µm	ND	6.6KS/s	0.027
[5]	M. Slope	10b	Adaptive	7.5µm	130µW	0.8MS/s	0.047
[19]	S/M Slope	10b	Adaptive	10µm	ND	0.43MS/s	0.0522
[20]	Cyclic	12b	1800µV	10µm	430µW	0.17MS/s	0.1512
[21]	SAR	9b	335µV	100µm (3D)	381µW	4.4MS/s	0.57

Table 1. Relevant ADCs for image sensors recently published

4. STATE-OF-THE-ART

We summarize in Table.1 some relevant ADCs recently reported. All of them are targeted for image sensors with column parallel read-out. In order to compare them, we defined a new FOM for ADCs for imagers:

$$FOM = \frac{N_s \cdot Pitch^2 \cdot P}{2^{N_{bits}} \cdot f_s} \quad (6)$$

The FOM was written in the "lower-is-better" form to simplify comparison. It rewards the number of bits, N_{bits}, and the speed sampling frequency, f_s. It penalties the random noise, N_s, of the ADC (expressed in V_{rms}), the power, P, and the minimum pixel width that can read out, $Pitch$. Comparing the FOM values, SAR and cyclic ADCs offer very good performance. Slope ADCs perform worse, but are still frequently used due to their simplicity and the possibility of implementing them using very low pitches. ΣΔ converters and hybrid architectures with them also offer good performance.

5. CONCLUSIONS

Some guidelines to optimize the pixel analog-to-digital conversion are given. The document address how the read-out speed is increased by placing different number of ADCs operating in parallel. Moreover, the requirements that an ADCs for image sensors must satisfy have been described and quantified. Furthermore, a FOM to compare different ADCs for image sensors has been defined. Finally, the performance of recent relevant ADCs for image sensors have been compared using this FOM.

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REFERENCES

[1] El-Desouki, M., Deen, M. J., Fang, Q., Liu, L., Tse, F., and Armstrong, D., "CMOS image sensors for high speed applications," *Sensors* , 430–444 (2009).

[2] Yang, D. X. D., Fowler, B., and Gamal, A. E., "A nyquist-rate pixel-level ADC for CMOS image sensors," *IEEE Journal of Solid-state Circuits* **34** (March 1999).

[3] Kleinfelder, S., Lim, S., Liu, X., and Gamal, A. E., "A 10,000 Frames/s CMOS digital pixel sensor," *IEEE Journal of Solid-state Circuits* **36** (December 2001).

[4] Kitchen, A., Bermak, A., and Bouzerdoum, A., "A digital pixel sensor array with programmable dynamic range," *IEEE Transactions on Electron Devices* **52** (December 2005).

[5] Snoeij, M. F., Theuwissen, A. J. P., Makinwa, K. A. A., and Huijsing, J. H., "Multiple-ramp column-parallel ADC architectures for CMOS image sensors," *IEEE Journal of Solid-state Circuits* **42**(12) (2007).

[6] Blackwell, H. R., "Contrast threshold of the human eye," *Journal of the Optical Society of America* **36** (November 1946).

[7] Park, J.-H., Aoyama, S., Watanabe, T., Isobe, K., and Kawahito, S., "A high-speed low-noise CMOS image sensor with 13-b column-parallel single-ended cyclic ADCs," *IEEE Transactions on Electron Devices* **56**(11) (2009).

[8] Chae, Y. and et al., "A 2.1Mpixel 120frame/s CMOS image sensor with column-parallel ADC architecture," *International Solid-state Circuits Conference, ISSCC* **46**(1), 236–247 (2010).

[9] Matsuo, S., Bales, T., M.Shoda, S.Osawa, Almond, B., Mo, Y., Gleason, J., Chow, T., and Takayanagi, I., "A very low column FPN and row temporal noise 8.9 M-pixel, 60 fps CMOS image sensor with 14bit column parallel SA-ADC," *Symp. VLSI Circuits Dig. Tech. Papers* , 138–139 (2008).

[10] Seo, M. W. and et al., "A low noise wide dynamic range CMOS image sensor with low-noise transistors and 17b column-parallel ADCs," *IEEE Sensors Journal* **13** (August 2013).

[11] Shin, M. S., Kim, J.-B., Kim, M.-K., Jo, Y.-R., and Kwon, O.-K., "A 1.92-Megapixel CMOS image sensor with column-parallel low-power and area-efficient SA-ADCs," *IEEE Transactions on Electron Devices* **59** (June 2012).

[12] Lim, Y., Koh, K., Kim, K., Yang, H., Kim, J., Jeong, Y., Lee, S., Lee, H., Lim, S.-H., Han, Y., Kim, J., Yun, J., Ham, S., and Lee, Y.-T., "A 1.1e- temporal noise 1/3.2-inch 8Mpixel CMOS image sensor using pseudo-multiple sampling," *International Solid-state Circuits Conference, ISSCC* (2010).

[13] Seo, M.-W., Suh, S.-H., Iida, T., Takasawa, T., Isobe, K., Watanabe, T., Itoh, S., Yasutomi, K., and Kawahito, S., "A low-noise high intrascene dynamic range CMOS image sensor with a 13 to 19b variable-resolution column-parallel folding-integration/cyclic ADC," *IEEE Journal of Solid State Circuits* **47**(1) (2012).

[14] Chen, D. G., Tang, F., and Bermak, A., "A low-power pilot-DAC based column parallel 8b SAR ADC with forward error correction for CMOS image sensors," *IEEE Transactions on Circuits and SystemsI* **60** (October 2013).

[15] Tsai, S.-J., Chen, Y.-C., Hsieh, C.-C., Chang, W.-H., Tsai, H.-H., and Chiu, C.-F., "A column-parallel SAR ADC with linearity calibration for CMOS imagers," *IEEE Sensors Conference* , 14 (October 2012).

[16] Kim, J.-H. and et al., "A 14b extended counting ADC implemented in a 24Mpixel APS-C CMOS image sensor," *International Solid-state Circuits Conference, ISSCC* , 390–392 (February 2012).

[17] Takayuki and et al., "A 17.7Mpixel 120fps CMOS image sensor with 34.8Gb/s readout," *International Solid-state Circuits Conference, ISSCC* (2011).

[18] Yoshihara, S. and et al, "A 1/1.8-inch 6.4 Mpixel 60 frames/s CMOS image sensor with seamless mode change," *IEEE Journal of Solid State Circuits* **41**(12) (2006).

[19] Sasaki, M., Mase, M., Kawahito, S., and Tadokoro, Y., "A wide-dynamic-range CMOS image sensor based on multiple short exposure-time readout with multiple-resolution column-parallel ADC," *IEEE Sensors Journal* **7**(1) (2007).

[20] Furuta, M., Nishikawa, Y., Inoue, T., and Kawahito, S., "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters," *IEEE Journal of Solid-state Circuits* **43**, 766 – 774 (April 2007).

[21] Kiyoyama, K., Lee, K., Fukushima, H., T., Naganuma, Kobayashi, H., Tanaka, T., and Koyanagi, M., "A very low area ADC for 3D stacked CMOS image processing system," *IEEE International 3D Systems Integration Conference, 3DIC* , 1–4 (2011).