Efficient Hybrid Continuous-Time/Discrete-Time Cascade ΣΔ Modulators for Wideband Applications

J. Gerardo García-Sánchez and José M. de la Rosa*

Instituto de Microelectrónica de Sevilla, IMSE-CNM, (CSIC/Universidad de Sevilla)
C/Américo Vespucio, 41092 Sevilla, SPAIN
Phone: +34954466666, E-mail: [jggarcia,jrosa]@imse-cnm.csic.es

Abstract

This paper analyses the use of hybrid continuous-time/discrete-time cascade ΣΔ modulators for the implementation of power-efficient analog-to-digital converters in broadband wireless communication systems. Two alternative implementations of multi-rate cascade architectures are studied and compared with conventional single-rate continuous-time topologies, taking into account the impact of main circuit-level error mechanisms, namely: mismatch, finite dc gain and gain-bandwidth product. In all cases, closed-form design equations are derived for the nonideal in-band noise power of all ΣΔ modulators under study, providing analytical relationships between their system-level performance and the corresponding circuit-level error parameters. Theoretical predictions match simulation results, showing that the lowest performance degradation is obtained by a new kind of multi-rate hybrid ΣΔ modulator, in which the front-end (continuous-time) stage operates at a higher rate than the back-end (discrete-time) stages. As a case study, the design of a hybrid GmC/switched-capacitor fourth-order (two-stage, 4-bit) cascade ΣΔ modulator is discussed to illustrate the potential benefits of the presented approach[1].

Keywords: Analog-to-Digital Converters, sigma-delta modulators, hybrid continuous-time/discrete-time circuit techniques, multi-rate signal processing.

*Corresponding author: José M. de la Rosa, e-mail: jrosa@imse-cnm.csic.es

[1]This work has been supported by the Spanish Ministry of Economy and Competitiveness (with support from the European Regional Development Fund) under contract TEC2010-14825/MIC.

1. Introduction

The need of increasingly higher data rates in mobile telecom systems demands for power-efficient wideband Analog-to-Digital Converters (ADCs). Among other ADC techniques, Sigma-Delta Modulators ($\Sigma\Delta$Ms) implemented with Continuous-Time (CT) circuits have demonstrated to be a suited solution in these applications. Compared with Discrete-Time (DT) $\Sigma\Delta$Ms – usually implemented with Switched-Capacitor (SC) circuits – CT-$\Sigma\Delta$Ms achieve faster rates with less power consumption. However, they present a higher sensitivity than DT-$\Sigma\Delta$Ms to some critical circuit nonidealities, mainly: clock jitter error and circuit element tolerances [1]. This has motivated the exploration of other alternatives like the so-called Hybrid CT/DT $\Sigma\Delta$Ms (H-$\Sigma\Delta$Ms) [2, 3, 4, 5, 6], in which the front-end part of the $\Sigma\Delta$M is implemented with CT circuits, thus benefiting from their faster operation, embedded anti-aliasing filtering and reduced power dissipation, while keeping a higher robustness than *pure* CT-$\Sigma\Delta$Ms against circuit errors.

The main drawback of H-$\Sigma\Delta$Ms is that their sampling rate is indeed limited by the DT part of the system. This is the main reason why reported silicon implementations of H-$\Sigma\Delta$Ms do not really exploit the speed advantages of using CT circuits. A possible solution to palliate this limitation might be using a different sampling frequency for each part (either CT or DT) of the H-$\Sigma\Delta$M, i.e. using a *multi-rate* system [7]. This approach has been applied to both cascade DT- [8] and CT-$\Sigma\Delta$Ms [9]. In both cases, the strategy was based on using a lower OverSampling Ratio (OSR) in the front-end parts of the modulator – where most of the power is consumed – and a higher OSR in the subsequent stages or blocks – where the dynamic requirements can be

relaxed. These limitations can be palliated in cascade H-ΣΔMs if the signal is *downsampled* across the cascade, so that the CT front-end operates at a higher clock rate than the DT back-end, thus relaxing its dynamic requirements, and achieving the targeted specifications by properly combining the different OverSampling Ratios (OSRs) in a *multi-rate* operation [10].

In spite of the potential benefits of the combination of multi-rate signal processing and hybrid CT/DT circuit techniques, an in-depth study of the influence of their main circuit nonideal effects on the performance of H-ΣΔMs is required to get optimized designs in terms of power consumption and silicon area. Based on the design equations derived from such a study, a systematic top-down/bottomp-up design procedure can be established to reach the required ΣΔM specifications with minimized power dissipation and silicon area. This procedure has been applied to both CT-ΣΔMs [1] and SC-ΣΔMs [11]. However, to the best of the authors' knowledge, H-ΣΔMs have not been analyzed taking into account the impact of their building-block errors.

This paper contributes to this topic and analyses the impact of main circuit nonidealities on the performance of two different types of cascade Multi-Rate (MR) H-ΣΔMs. The first one, named *UpSampling* MR H-ΣΔM (US MR H-ΣΔM), increases the OSR in the back-end stages in the cascade. The second one, referred to as *DownSampling* MR H-ΣΔM (DS MR H-ΣΔM), decreases the OSR in the back-end stages. Both architectures are compared with conventional Single-Rate (SR) cascade CT-ΣΔMs. All the architectures under study are analyzed in order to obtain closed-form design equations that relate main ΣΔM performance metrics with circuit-error model parameters.

These equations, which are also valid for SR H-ΣΔMs, are compared with time-domain behavioral simulations, considering diverse cases of signal bandwidths and target effective resolutions, showing a good agreement between theory and simulated performance. As a case study, the design of a fourth-order 2-stage cascade DS MR Gm-C/SC ΣΔM with 4-bit quantization is presented to demonstrate the feasibility of the presented approach to digitize signals with a 44- to-92dB peak signal-to-(noise+distortion) ratio within a programmable 5-to-60MHz bandwidth.

The paper is organized as follows. Section 2 gives a background on MR H-ΣΔMs, overviewing the conceptual topologies and basic principles behind *upsampling* and *downsampling* strategies. Section 3 describes the modulator architectures under study, analyzing their main performance figures from an ideal point of view. The impact of main error mechanisms is analyzed in Section 4, validating the theoretical predictions with time-domain simulations. As an application, the presented study is applied to the systematic high-level design of a cascade GmC/SC MR H-ΣΔMs, described in Section 5.

2. Background on Multi-Rate Hybrid ΣΔMs

Fig. 1(a) shows the conceptual implementation of a conventional cascade (two-stage) MR-ΣΔM.[2] For the sake of generality, multibit quantization will be assumed in all stages of the cascade, with B_i being the number of bits of the internal quantizer in the ith stage. The sampling frequency f_{si} of the different modulator blocks is depicted in the figure. The most common

[2]Two-stage cascade ΣΔMs will be considered in this paper without loss of generality.

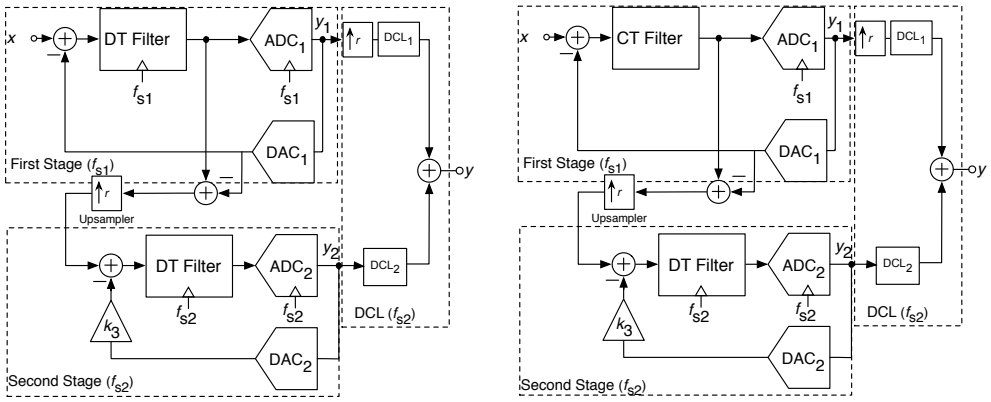


Figure 1: Conceptual block diagram of a upsampling cascade MR-ΣΔM: (a) DT scheme. (b) Hybrid CT/DT scheme.

situation in conventional MR-ΣΔMs is that the front-end stage operates at f_{s1}, whereas the remaining ith stages are sampled at $f_{si} > f_{s1}$. This approach – also referred to as *upsampling* MR-ΣΔM [10] – benefits from increasing values of OSR in the back-end stages – where the dynamic requirements are less demanding than in the front-end stages [7, 9].

The operation behind the modulator in Fig. 1(a) is conceptually the same as in a conventional SR cascade ΣΔM. All stage outputs are combined by the Digital Cancellation Logic (DCL) – clocked at f_{s2} –, so that ideally only the quantization error of the last stage remains and it is shaped by a Noise Transfer Function (NTF) whose order (L) is the sum of the orders of all stages in the cascade (L_i). However, as a consequence of using several sampling frequencies, additional *upsampler* blocks – represented conceptually in Fig. 1(a) – are required, where $r \equiv f_{s2}/f_{s1}$ denotes the *upsampling ratio*, with $r > 1$ [10].

2.1. Upsampling MR H-ΣΔMs

The concept of MR-ΣΔMs can be extended to hybrid CT/DT implementations as conceptually depicted in Fig. 1(b), that represents a cascade two-stage MR H-ΣΔM. The circuit nature (either CT or DT) of the different modulator blocks as well as their corresponding sampling frequencies are highlighted. The analysis of Fig. 1(b) can be carried out by applying a DT–CT transformation to the front-end stage of Figure 1(b). The resulting MR H-ΣΔM is equivalent to the original MR DT-ΣΔM. This CT–DT equivalence can be guaranteed because of the DT nature of the (open) loop transfer function from the front-end quantizer output to the sampled quantizer input [12, 13].

2.2. Downsampling MR H-ΣΔMs

Fig. 2 shows a conceptual block diagram of a *downsampling* (two-stage) cascade MR H-ΣΔM architecture proposed in [10]. In contrast to conventional (*upsampling*) MR H-ΣΔMs, the back-end (DT) stage operates at a rate lower than that of the front-end (CT) stage; i.e. $f_{s1} = p \cdot f_{s2}$, with $p > 1$ being the *downsampling ratio*. The main drawback of this approach is the aliasing caused by the downsampling processing, what requires using an interstage Anti-Aliasing Filtering (AAF). However, as shown in [10], the operation of the AAF can be completely translated to digital domain, by using two additional digital blocks, whose transfer functions are named $H_1(z)$ and $H_2(z)$.

Therefore, the operation behind the modulator in Fig. 2 is essentially the same as in conventional cascade ΣΔMs. The main difference is that the DCL

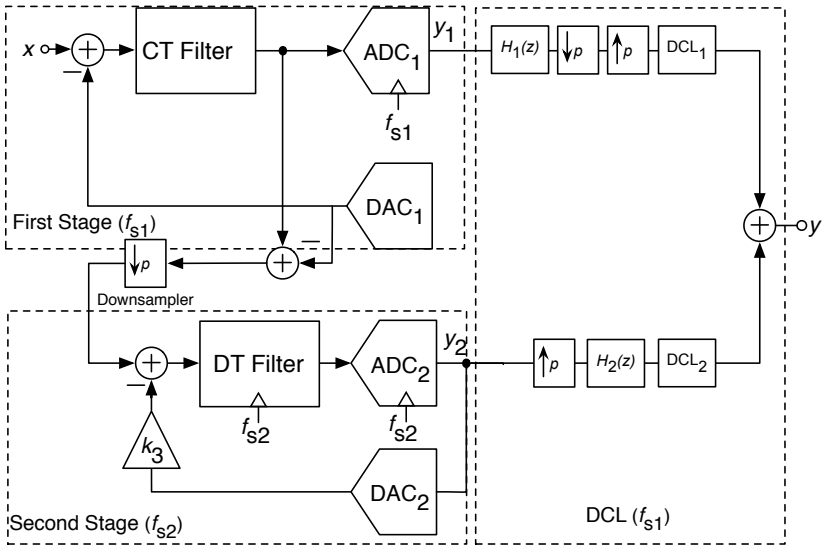


Figure 2: Conceptual block diagram of a downsampling cascade MR H-ΣΔM [10].

transfer functions are designed so that they must remove not only the quantization error of the front-end stage $E_1(z)$, but also its aliased components. To this purpose, $H_1(z)$ and $H_2(z)$ must be reconfigurable and programmable according to the value of p [10]. These functions are completely implemented in the digital domain, without any extra analog hardware required, and can be synthesized for different values of p as detailed below.

3. ΣΔM Architectures Under Study

Fig. 3 shows the block diagram of the MR H-ΣΔMs under study, where $H(s) = 1/s$ and $H(z) = z^{-1}/(1 - z^{-1})$, denote the transfer functions of the CT and DT integrators, respectively. The same loop-filter topology is used in all cases, consisting of a fourth-order cascade 2-stage (2-2) architecture, where the front-end stage includes feed-forward paths to implement a Unity Signal

Transfer Function (USTF). Embedded multi-bit quantization is considered in both stages of the modulators. Two different topologies are considered attending to the sampling rate of each stage and its circuit nature, either CT or DT. Fig. 3(a) is a conventional US MR H-ΣΔM, where the back-end stage operates at a higher sampling frequency than the front-end stage [7], i.e. $f_{s2} = r \cdot f_{s1}$. The opposite operation is carried out in Fig. 3(b), which corresponds to a DS MR H-ΣΔM, in which the front-end stage operates at the highest sampling rate, i.e. $f_{s1} = p \cdot f_{s2}$.

Both MR H-ΣΔMs in Fig. 3 are compared with the conventional cascade SR CT-ΣΔM shown in Fig. 4, where both stages are implemented using CT circuits and operate at the same sampling frequency, f_s.

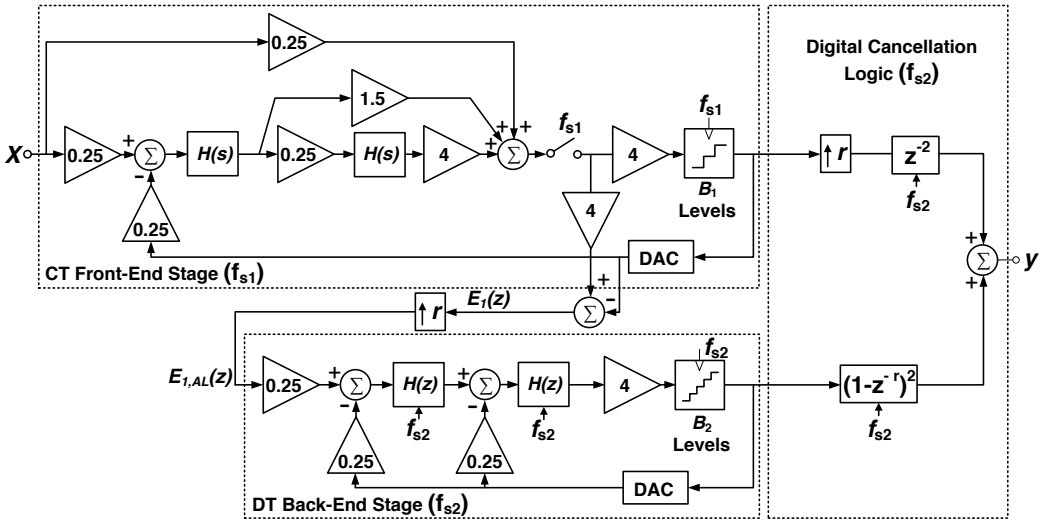
3.1. Ideal Noise Transfer Function

The analysis of the modulators in Fig. 3 can be carried out in the Z-domain by applying a CT-to-DT transformation to the CT stages, so that the resulting DT-ΣΔMs are equivalent to the original ΣΔMs [14]. Thus, assuming a linear model for the quantizers in Fig. 3(a) and Fig. 4(a) and Non-Return-to-Zero (NRZ) feedback DACs in the CT stages, it can be shown that the quantization NTF at the output of both modulators are respectively given by [9, 10]:

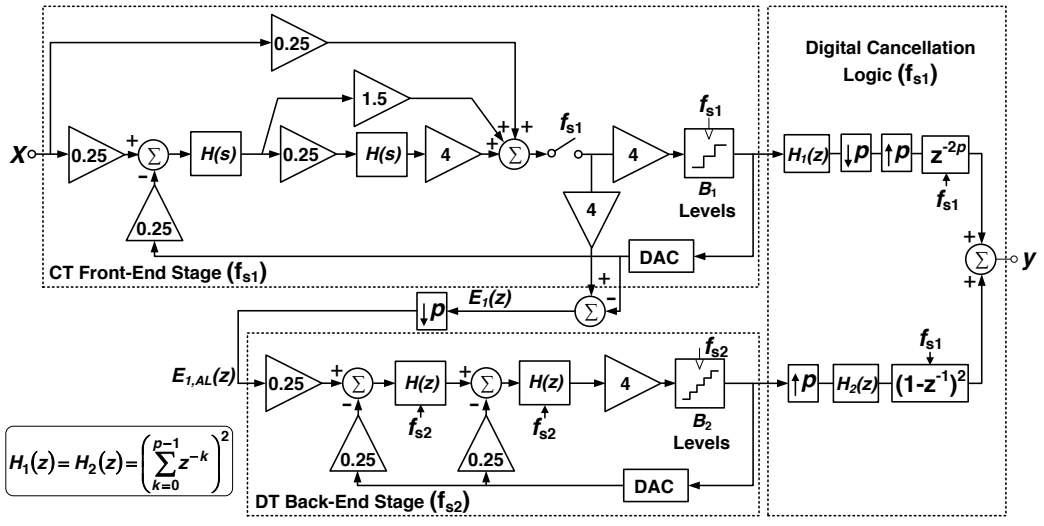
$$\mathrm{NTF}_{\mathrm{SR}}(z) = (1 - z^{-1})^{(L_1+L_2)} \tag{1}$$

$$\mathrm{NTF}_{\mathrm{US}}(z) = (1 - z^{-r})^{L_1}(1 - z^{-1})^{L_2} \tag{2}$$

where $L_1 = 2$ and $L_2 = 2$ stand for the order of the front-end and the back-end stages of the modulators, respectively.



(a)



(b)

Figure 3: Cascade 2-2 MR H-ΣΔMs: (a) US MR H-ΣΔM. (b) DS MR H-ΣΔM.

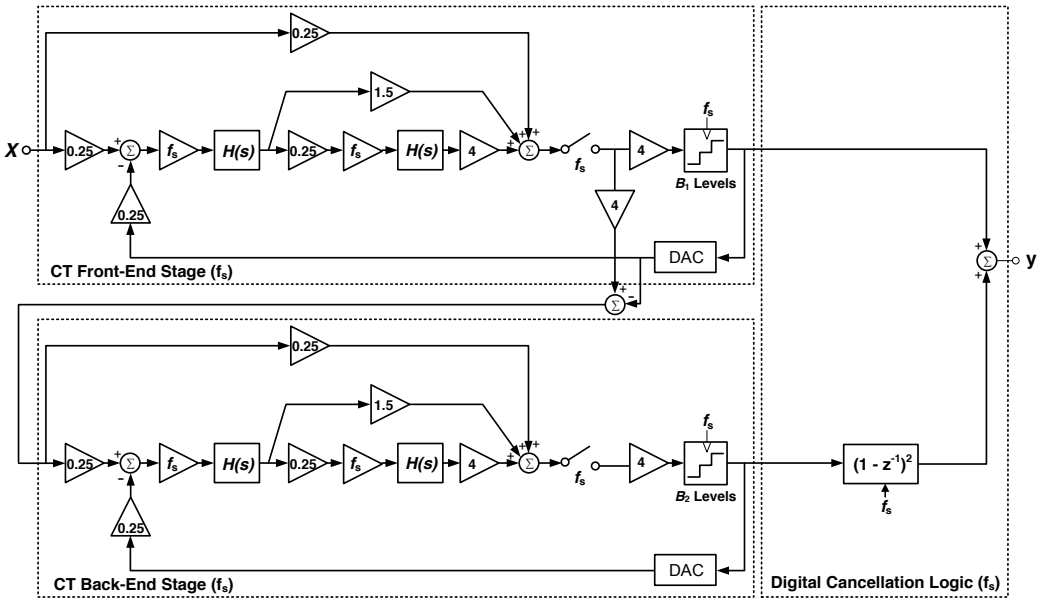


Figure 4: Block diagram of a cascade 2-2 SR CT-ΣΔM.

Note that the back-end (DT) stage of the DS MR H-ΣΔM shown in Fig. 3(b) operates at a lower rate than the front-end (CT) stage. Therefore, the quantization error signal, $E_1(z)$, that is fed to the back-end stage, is *downsampled*, thus containing aliased components at multiples of f_{s2}. This can be expressed in the Z-domain as:

$$E_{1,\mathrm{AL}}(z) = \frac{1}{p}\sum_{k=0}^{p-1} E_1(z^{1/p}e^{j(2\pi k/p)}) \tag{3}$$

Assuming a linear model for the quantizers in Fig. 3(b), it can be shown that both $E_1(z)$ and its aliased error components can be completely cancelled out if $H_1(z)$ and $H_2(z)$ are given by the following expression [10]:

$$H_1(z) = H_2(z) = \left(\sum_{k=0}^{p-1} z^{-k}\right)^{L_1} \tag{4}$$

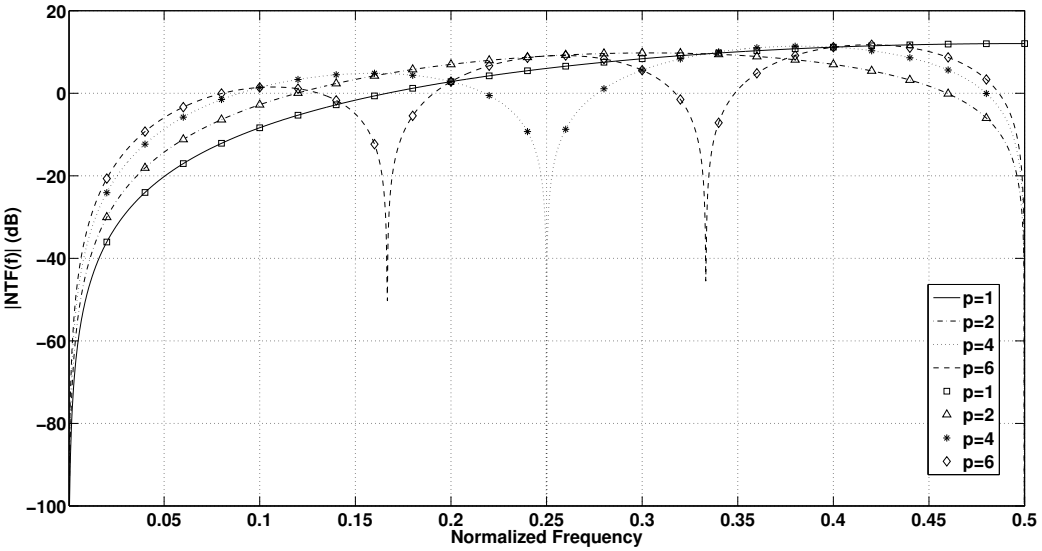


Figure 5: $|\mathrm{NTF}_{\mathrm{DS}}(f)|$ versus normalized frequency (f/f_s).

Taking into account the above expression, it can be shown that the NTF of Fig. 3(b) can be written as:

$$\mathrm{NTF}_{\mathrm{DS}}(z) = (1 - z^{-1})^{L_1}(1 - z^{-p})^{L_2} \tag{5}$$

Note from (2)-(5) that both MR H-$\Sigma\Delta$Ms in Fig. 3 provide identical noise-shaping provided that $p = r$. As an illustration, Fig. 5 plots $|\mathrm{NTF}_{\mathrm{DS}}(f)|$ versus the normalized frequency for different cases of p, highlighting the variation of the notch frequency caused by the multi-rate operation.

3.2. Ideal In-Band Noise Power

Integrating the expressions (1), (2) and (5) within the signal bandwidth, B_w, it can be shown that the In-Band Noise (IBN) power at the output of

the modulators in Fig. 3 and Fig. 4 are respectively given by [1, 10]:

$$\mathrm{IBN}_{\mathrm{US}}^{\mathrm{ideal}} \simeq \frac{\Delta^2 \pi^{2L} r^{2L_1}}{12(2L+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{2L+1}} \tag{6}$$

$$\mathrm{IBN}_{\mathrm{DS}}^{\mathrm{ideal}} \simeq \frac{\Delta^2 \pi^{2L} p^{2L_2}}{12(2L+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{2L+1}} \tag{7}$$

$$\mathrm{IBN}_{\mathrm{SR}}^{\mathrm{ideal}} \simeq \frac{\Delta^2 \pi^{2L}}{12(2L+1)\mathrm{OSR}^{2L+1}} \tag{8}$$

where Δ stands for the quantization step of the last quantizer; $L \equiv L_1 + L_2 = 4$ is the loop-filter order of the $\Sigma\Delta$Ms; $\mathrm{OSR}_{\mathrm{SR}} \equiv f_s/(2B_w)$ is the OSR of the SR CT-$\Sigma\Delta$M, and $\mathrm{OSR}_{2_{\mathrm{US}}} \equiv f_{s2}/(2B_w)$ and $\mathrm{OSR}_{1_{\mathrm{DS}}} \equiv f_{s1}/(2B_w)$ denote the value of the largest OSR in the US MR H-$\Sigma\Delta$M and DS MR H-$\Sigma\Delta$M, respectively. It can be noted that the expressions in (6) and (7) reduce to the one obtained by conventional SR CT-$\Sigma\Delta$Ms, shown in (8), provided that $r = p = 1$ and $\mathrm{OSR}_{2_{\mathrm{US}}} = \mathrm{OSR}_{1_{\mathrm{DS}}} = \mathrm{OSR}_{\mathrm{SR}}$. Note also that the same ideal IBN can be achieved by all $\Sigma\Delta$Ms in Fig. 3, by properly choosing the values of r, p, $\mathrm{OSR}_{\mathrm{SR}}$, $\mathrm{OSR}_{2_{\mathrm{US}}}$ and $\mathrm{OSR}_{1_{\mathrm{DS}}}$. As an illustration, Fig. 6 depicts the Signal-to-Noise Ratio (SNR) versus $\mathrm{OSR}_{1_{\mathrm{DS}}}$ for different values of r and p, showing a good agreement between theory and simulations within a wide resolution range.

4. Analysis of Nonideal Performance

The performance described above assumed that the $\Sigma\Delta$Ms in Fig. 3 and Fig. 4 were implemented with ideal building blocks. However, in practice, the noise shaping (and consequently the effective resolution) of these modulators is degraded by the action of circuit-level errors. This section analyses the IBN degradation caused by three of the most critical nonideal effects,

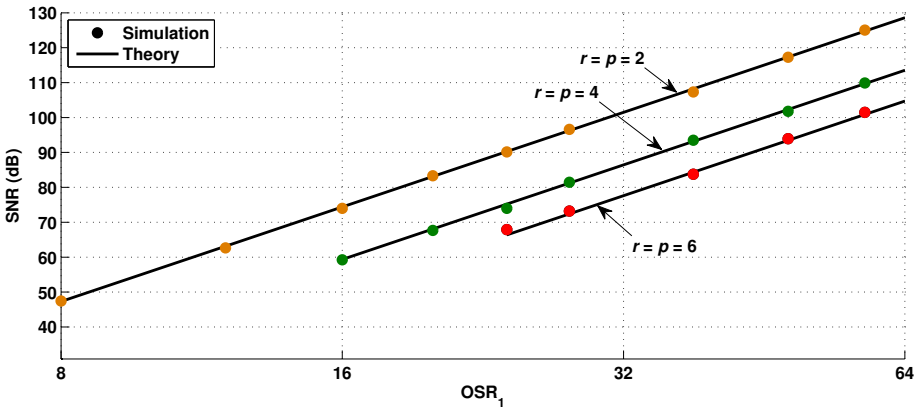


Figure 6: SNR vs. $\mathrm{OSR}_{1_{\mathrm{DS}}}$ for different values of r and p.

namely: mismatch error, finite OTA dc gain and Gain-BandWidth (GBW) product. In order to perform this analysis, Forward-Euler (FE) SC integrators, conceptually modeled as shown in Fig. 7(a), will be used for the DT stages, while Gm-C integrators, considering the 1-pole OTA model depicted in Fig. 7(b), will be used for the CT blocks.

In order to analyse the impact of a given circuit error, generically denoted as ϵ, a systematic procedure similar to the one used for SC $\Sigma\Delta$Ms [11] and CT $\Sigma\Delta$Ms [1] is followed, but in this case taking into account that different circuit dynamics are involved in H-$\Sigma\Delta$Ms. This way, the integrator transfer functions, $H(s)$ and $H(z)$ in Fig. 3 and Fig. 4, are replaced by the corresponding nonideal functions degraded by errors, $H(z,\vec{\epsilon})$ and $H(s,\vec{\epsilon})$, where $\vec{\epsilon}$ denotes a generic vector that includes all different model parameters for a given error. Thus, using a linear model for the quantizers and applying the CT-to-DT equivalence described in previous section, the effect of circuit errors can be propagated through the modulator in order to obtain the non-

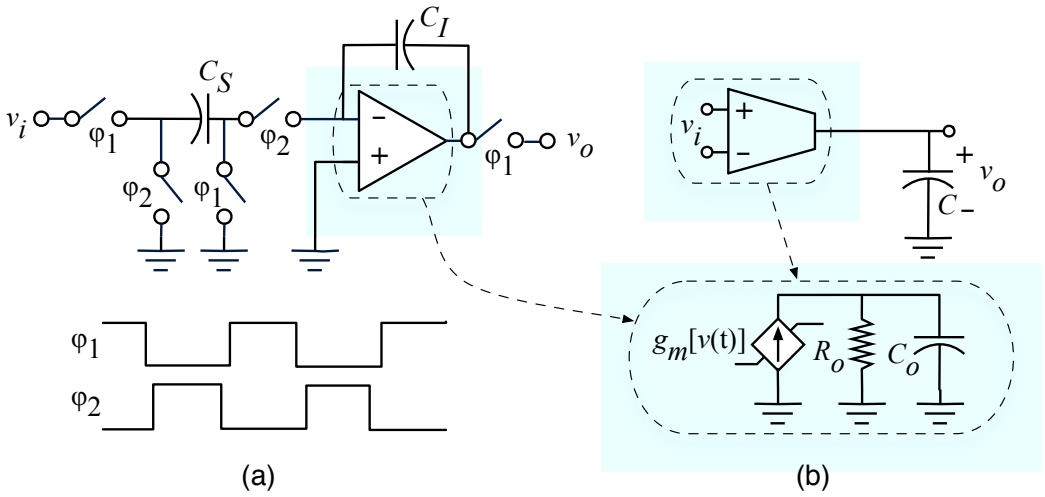


Figure 7: Models used for the (a) SC Integrator, (b) Gm-C Integrator.

ideal expressions for NTF and IBN. This procedure, that can be conceptually formulated as:

$$H(z,\vec{\epsilon}), H(s,\vec{\epsilon}) \rightarrow \mathrm{NTF}(z,\vec{\epsilon}) \rightarrow \mathrm{IBN}(\mathrm{OSR}, B_i, L, p, \vec{\epsilon}) \tag{9}$$

has been followed to find out the nonideal expressions of the IBN degraded by different errors described below.

4.1. Capacitor Mismatch and Time-Constant Error

Let us assume that the integrators in Fig. 7 have a *weight error* caused by technology process variations. In the case of SC FE integrators, this gain error – due to capacitor mismatch and denoted as ϵ_{DT} – is modeled as a random deviation of the integrator's weight, i.e. the ratio between the sampling capacitor C_S and the integrator capacitor C_I [11]. In the case of Gm-C realizations, integrator's weight error, ϵ_{CT}, is due to random variations of the

time constant, i.e. the transconductance-capacitor product [1]. Considering the effect of ϵ_{DT} and ϵ_{CT}, $H(s)$ and $H(z)$ become modified as [1, 11]:

$$H(z,\epsilon_{\mathrm{DT}}) = \frac{(1-\epsilon_{\mathrm{DT}})z^{-1}}{1-z^{-1}}; H(s,\epsilon_{\mathrm{CT}}) = \frac{(1-\epsilon_{\mathrm{CT}})\cdot f_s}{s} \tag{10}$$

Replacing the above transfer functions in Fig. 3 and Fig. 4, and propagating the impact of mismatch errors according to the procedure formulated in (9), it can be shown that the IBN power at the output of the ΣΔMs under study can be approximated by:

$$\begin{aligned}
&\mathrm{IBN}_{\mathrm{SR}}^{\mathrm{mis}} \simeq (1+\epsilon_{\mathrm{CT}})^2 \cdot \mathrm{IBN}_{\mathrm{SR}}^{\mathrm{ideal}} + \frac{\Delta_1^2 \pi^{2L_1} \epsilon_{\mathrm{CT1}}^2}{12(2L_1+1)\mathrm{OSR}_{\mathrm{SR}}^{2L_1+1}} \\
&\mathrm{IBN}_{\mathrm{USMR}}^{\mathrm{mis}} \simeq (1+\epsilon_{\mathrm{DT}})^2 \cdot \mathrm{IBN}_{\mathrm{USMR}}^{\mathrm{ideal}} + \frac{\Delta_1^2 \pi^{2L_1} \epsilon_{\mathrm{CT1}}^2 r^{2L_1+1}}{12(2L_1+1)\mathrm{OSR}_{2_{\mathrm{US}}}^{2L_1+1}} \\
&\mathrm{IBN}_{\mathrm{DSMR}}^{\mathrm{mis}} \simeq (1+\epsilon_{\mathrm{DT}})^2 \cdot \mathrm{IBN}_{\mathrm{DSMR}}^{\mathrm{ideal}} + \\
&+ \frac{\Delta_1^2 \pi^{2L_1}}{12(2L_1+1)\mathrm{OSR}_{1_{\mathrm{DS}}}^{2L_1+1}} \cdot \sum_{k=0}^{p-1} \left| \alpha(k)\epsilon_{\mathrm{CT11}} + \frac{\beta(k)}{2}\epsilon_{\mathrm{CT12}} \right|^2
\end{aligned} \tag{11}$$

where Δ_1 stands for the quantization step of the front-end quantizer; $\epsilon_{\mathrm{CT}ij}$ denote the weight error of the j-th Gm-C integrator in the i-th stage ($i, j = 1, 2$); and $\alpha(k) = (2e^{-j2\pi k/p} - e^{-j4\pi k/p})$ and $\beta(k) = (e^{-j2\pi k/p} + e^{-j4\pi k/p})$.

4.2. Finite OTA dc Gain

Let us consider now that the integrators in Fig. 7 have a finite OTA dc gain. This effect can be modeled as a deviation of the integrator transfer functions given by [1, 11]:

$$H(z,\mu) \simeq \frac{z^{-1}}{1-z^{-1}(1-g\cdot\mu)}; H(s,\mu) = \frac{f_s}{\mu f_s + s} \tag{12}$$

where $g \equiv C_S/C_I$ stands for the weight of the SC integrator; $\mu \equiv 1/A_{\mathrm{dc}}$, and $A_{\mathrm{dc}} = g_m \cdot R_o$ denotes the finite OTA dc gain of both SC and Gm-C integrators in Fig. 7.

Thus, taking into account this effect on the integrators transfer functions, it can be demonstrated that the IBN at the output of the modulators in Fig. 3 and Fig. 4 is given by:

$$\begin{aligned}
\mathrm{IBN}_{\mathrm{SR}}^{\mathrm{gain}} &\simeq \left[1 + \frac{2L+1}{2L-1} \cdot \left(\frac{\mu_2 \cdot \mathrm{OSR}_{\mathrm{SR}}}{\pi}\right)^2\right] \cdot \mathrm{IBN}_{\mathrm{SR}}^{\mathrm{ideal}} + \\
&\quad + \frac{\Delta_1^2 \pi^{2L_1-2} \mu_1^2}{12 \cdot (2L_1-1) \cdot \mathrm{OSR}_{\mathrm{SR}}^{2L_1-1}} \\
\mathrm{IBN}_{\mathrm{USMR}}^{\mathrm{gain}} &\simeq \left[1 + \frac{2L+1}{2L-1} \cdot \left(\frac{\mu_2 \cdot \mathrm{OSR}_{2_{\mathrm{US}}}}{\pi}\right)^2\right] \cdot \mathrm{IBN}_{\mathrm{USMR}}^{\mathrm{ideal}} + \\
&\quad + \frac{\Delta_1^2 \pi^{2L_1-2} \mu_1^2 r^{2L_1-1}}{12 \cdot (2L_1-1) \cdot \mathrm{OSR}_{2_{\mathrm{US}}}^{2L_1-1}} \\
\mathrm{IBN}_{\mathrm{DSMR}}^{\mathrm{gain}} &\simeq \left[1 + \frac{2L+1}{2L-1} \cdot \left(\frac{\mu_2 \cdot \mathrm{OSR}_{1_{\mathrm{DS}}}}{\pi p}\right)^2\right] \cdot \mathrm{IBN}_{\mathrm{DSMR}}^{\mathrm{ideal}} + \\
&\quad + \frac{\Delta_1^2 \pi^{2L_1-2} \mu_1^2 p^{2L_1-1}}{12 \cdot (2L_1-1) \cdot \mathrm{OSR}_{1_{\mathrm{DS}}}^{2L_1-1}}
\end{aligned} \tag{13}$$

where $\mu_i \equiv 1/A_{\mathrm{dc}i1} + 1/A_{\mathrm{dc}i2}$ and $A_{\mathrm{dc}ij}$ is the dc gain of the j-th integrator in the i-th stage.

4.3. Gain-BandWidth Product

Following the same procedure as in previous sections, it can be found that the IBN degradation caused by the effect of the integrators' GBW can be modeled by replacing the expressions of $\epsilon_{\mathrm{CT}ij}$ and $\epsilon_{\mathrm{DT}ij}$ in (11) by the following expressions:

$$\epsilon_{\mathrm{CT}ij} \equiv \frac{f_s}{\mathrm{GBW}_{ij}}; \epsilon_{\mathrm{DT}ij} \equiv e^{\frac{-\pi \mathrm{GBW}_{ij}}{f_s}} \tag{14}$$

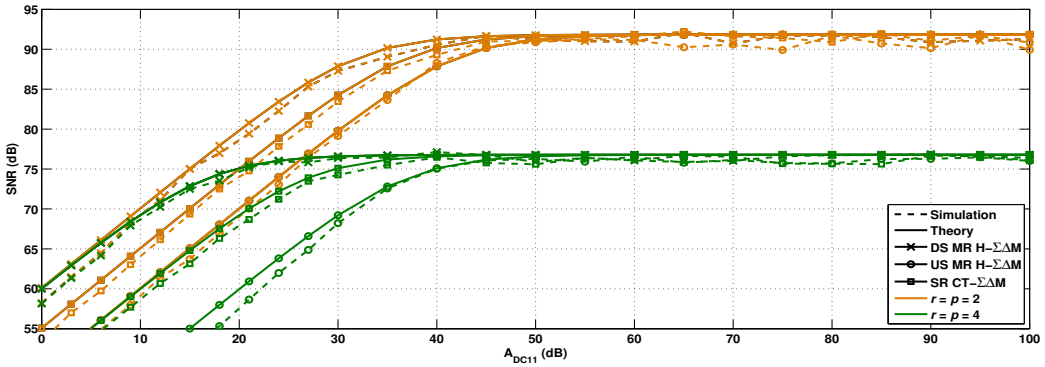
where GBW_{ij} is the value of GBW for the j-th integrator in the i-th stage.

4.4. Comparative Study and Verification by Simulations

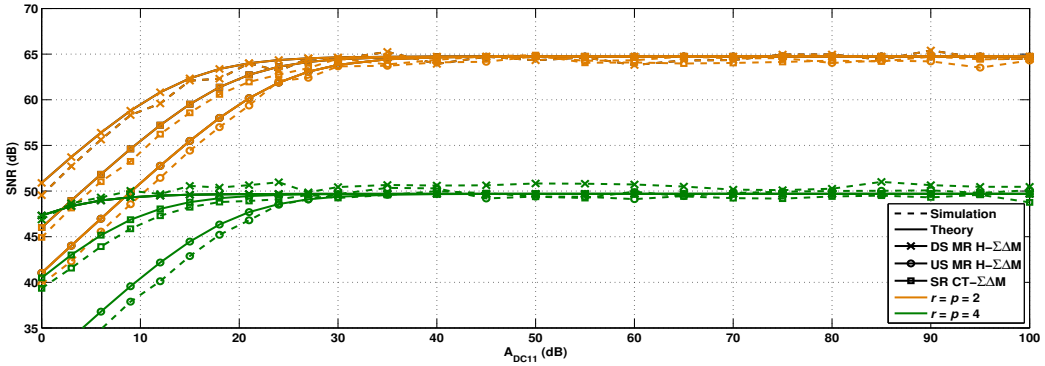
In order to verify the theoretical expressions derived in previous section, the ΣΔMs under study were compared and simulated using SIMSIDES – a time-domain behavioral simulator for ΣΔMs [15]. To make a fair comparison, the same ideal conditions, i.e. $r = p$ were assumed, and the values of OSR for each modulator were computed from (6), (7) and (8), so that the same ideal IBN is achieved in all cases. The same embedded quantizers were used in all ΣΔMs under study, considering 4-bit quantization in both stages. Two values of signal bandwidths were simulated, $B_w = 20, 40$MHz and a 1-MHz input tone with amplitude −7dB below quantization full-scale range was applied in all cases. For the sake of simplicity, only the effect of errors associated to the front-end (CT) integrators – which are common in all the ΣΔM architectures in Fig. 3 and Fig. 4 – have been taken into account in the simulations.

Fig. 8 shows the impact of finite dc gain error of the first Gm-C integrator for the ΣΔMs under study. Note that both theoretical predictions and simulation results are in good agreement, showing that the DS MR H-ΣΔM is less sensitive to the impact of this error, regardless the value of r, p and B_w.

The impact of GBW is illustrated in Fig. 9, highlighting a good matching between theory and simulations. The worst performance is obtained by the US MR H-ΣΔM, while a similar degradation is roughly achieved by both DS



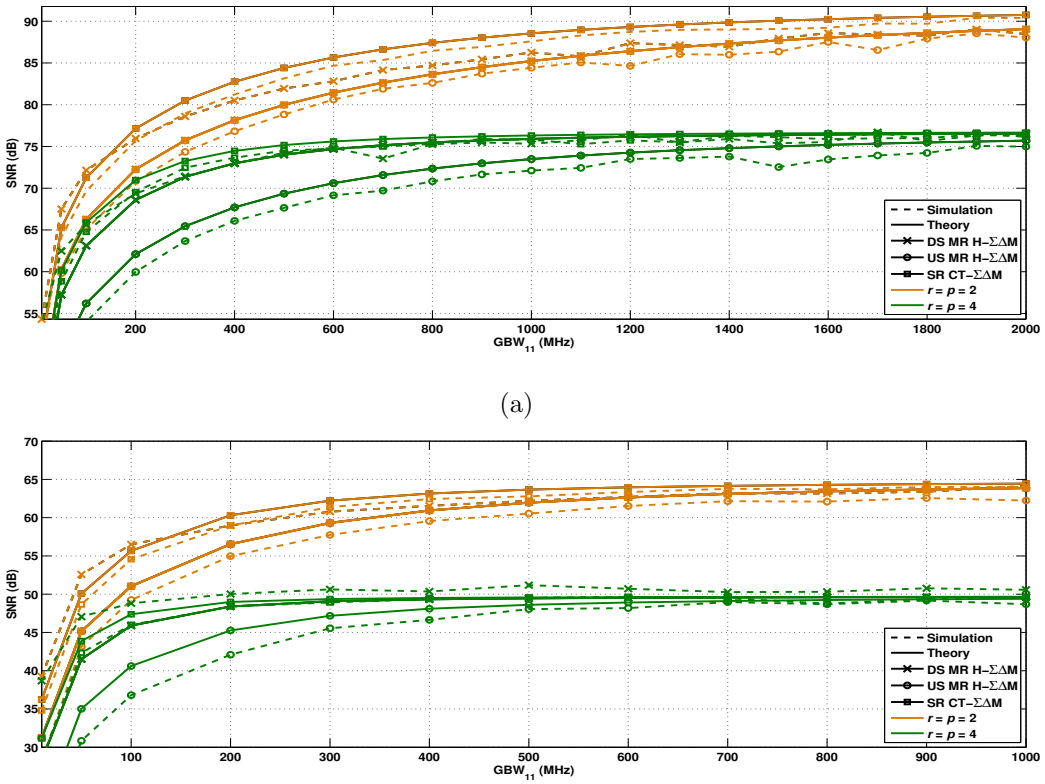
(a)



(b)

Figure 8: SNR vs. finite dc gain error for different values of r, p and: (a) B_w=20MHz. (b) B_w=40MHz.

MR H-ΣΔM and SR CT-ΣΔM. Indeed, the latter features a higher robustness against the impact of GBW in the first integrator. Finally, Fig. 10 shows the effect of circuit element tolerances in the time constant of the front-end Gm-C integrator. It can be noted how both theoretical calculations and simulations demonstrate that the DS MR H-ΣΔM achieves the largest robustness against mismatches, getting better as both p and B_w increase.



(a)

(b)

Figure 9: SNR vs. GBW for different values of r, p and: (a) B_w=20MHz. (b) B_w=40MHz.

5. Case study: A Gm-C/SC Cascade 2-2 DS MR H-ΣΔM

As a case study, Fig. 11 shows a conceptual schematic of the modulator in Fig. 3(b). The front-end (CT) stage is realized using Gm-C integrators. All transconductors can be tuned in order to keep the time constants, C/g_m, unchanged over C variations. Table 1 shows the values of nominal loop filter transconductances, g_{mi} (expressed in terms of the unitary transconductance, g_{mu}) as well as the capacitances, C_i, used to realize both Gm-C and SC integrators. Note that an extra feedback branch between the output and the

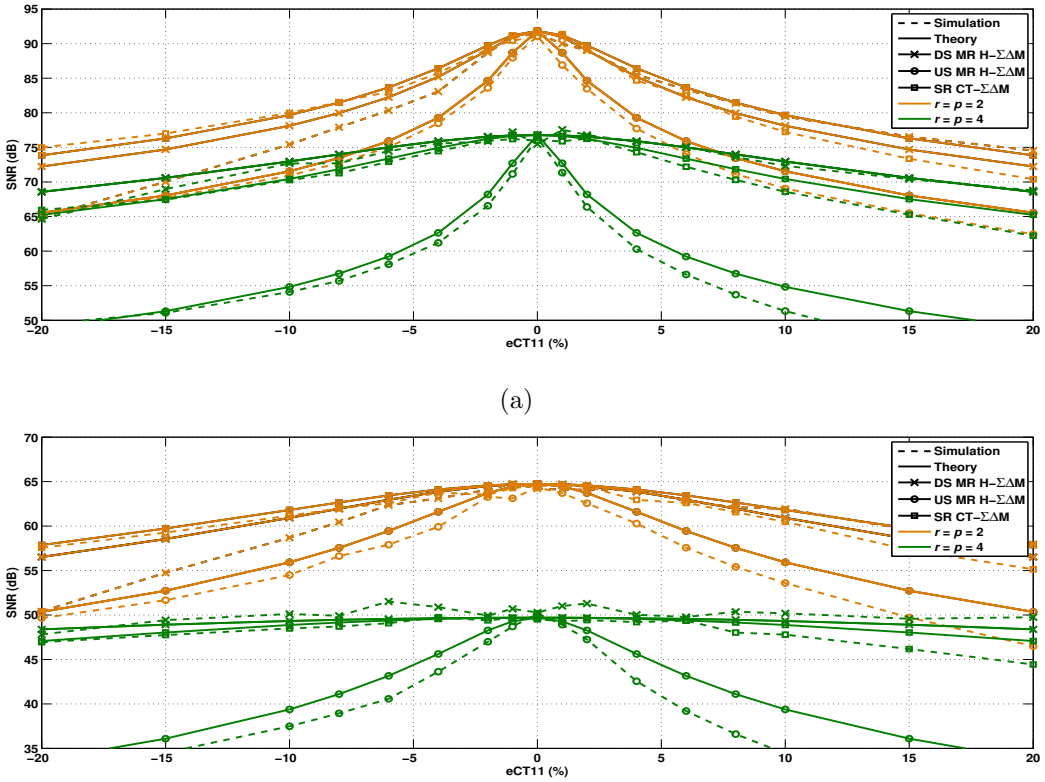


Figure 10: Effect of mismatch on SNR considering different values of r, p and: (a) B_w=20MHz. (b) B_w=40MHz.

input of the front-end quantizer and two additional D-latches are included in order to compensate for the excess loop delay [1]. This extra branch forces modifying the loop filter coefficients in order to obtain the ideal NTF given in (5). The back-end (DT) stage – realized with SC circuits – is a conventional second-order topology based on two feedback paths. Both stages include multi-level quantizers – 3-level in the front-end stage and 5-level in the back-end stage – in order to benefit from the extra level provided by fully differential implementation of the embedded flash ADCs.

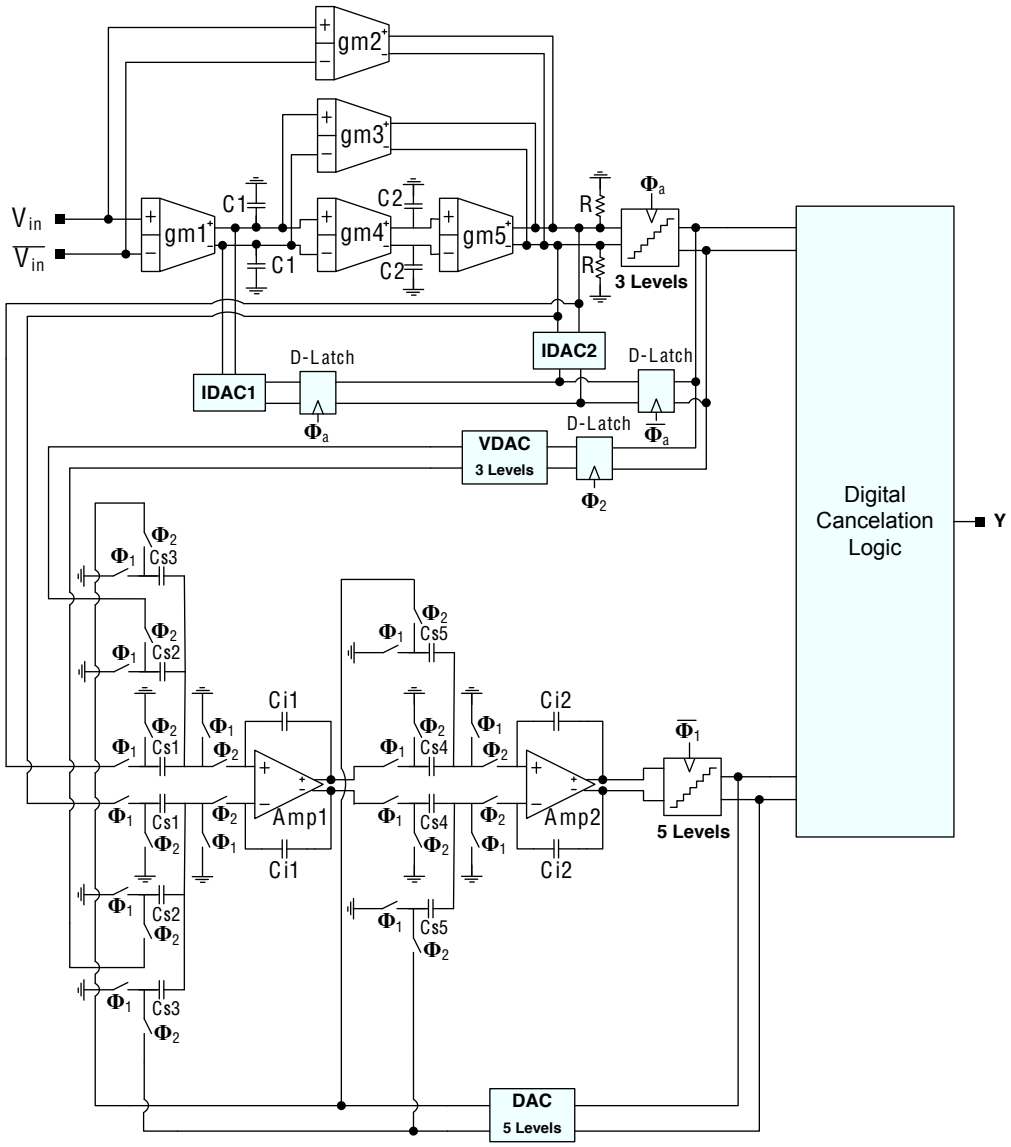
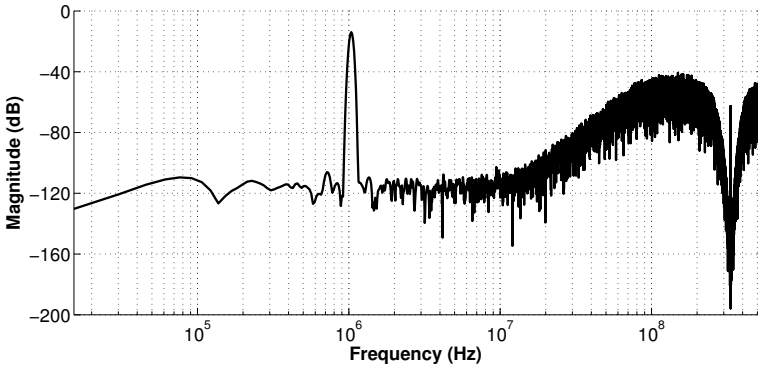


Figure 11: Conceptual Gm-C/SC schematic of the modulator in Fig. 3(c).

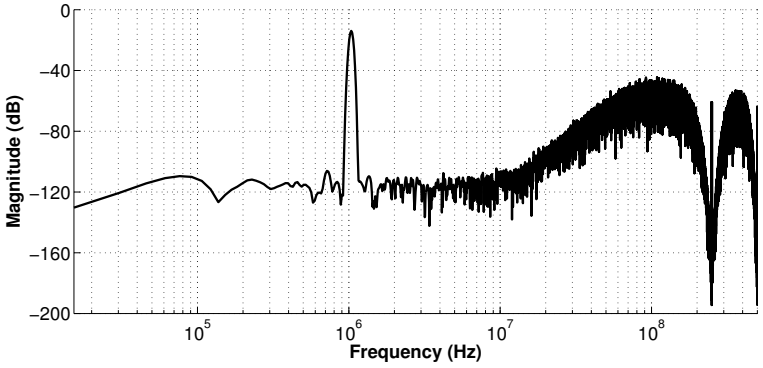
The Full-Scale (FS) reference voltage, V_{FS}, is 1V. Feedback DACs in the CT front-end stage are implemented as current steering NRZ 3-level DACs (named IDACs in Fig. 11) because of their potential high-speed operation and the convenience to inferface with the Gm-C loop filter. The output currents provided by both IDACs are also shown in Table 1. An additional voltage-mode 3-level DAC, named VDAC, is required in the inter-stage path. The digital cancellation logic is implemented as described in Section 2.

Fig. 12 shows the output spectra of the modulator in Fig. 11 for different values of p, considering a sampling frequency of the front-end stage of $f_{s1} =$ 1GHz and including thermal noise corresponding to $g_{mu} = 75\mu$A/V. Ideally, the modulator is able to digitize signals with B_w from 5MHz to 60MHz and an effective resolution ranging from 9 to 16 bits. According to (7), these specifications can be satisfied for $\text{OSR}_1 \in [8, 128]$ and $p = [2, 3, 4, 5, 6]$. This is illustrated in Fig. 13 that represents IBN vs. B_w (Fig. 13(a)) and IBN vs. OSR_1 (Fig. 13(b)) for different values of p. In this case, three values of f_{s1} are considered, $f_{s1} =$ 1GHz, 500MHz and 333MHz. The values of the Gm-C integration capacitors, $C_{1,2}$ are changed according to the expressions shown in Table 1, by using a switchable bank of three unit capacitances of value C_u=1.2pF. The sampling frequency of the SC back-end stage can be reconfigured through a programmable clock-phase generator, such that $f_{s2} = f_{s1}/p$. Both clock-phase generators are synthesized and controlled by a single master clock – generated by a digital PLL-based synthesizer whose reference frequency is f_{s1}. This is conceptually depicted in Fig. 14, where clock phases of both CT and SC stages are shown for different values of p.

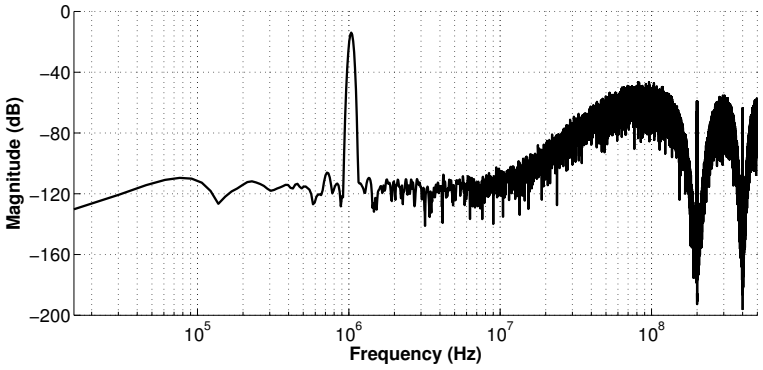
Fig. 17 illustrates the effect of circuit element tolerances in the CT part



(a)

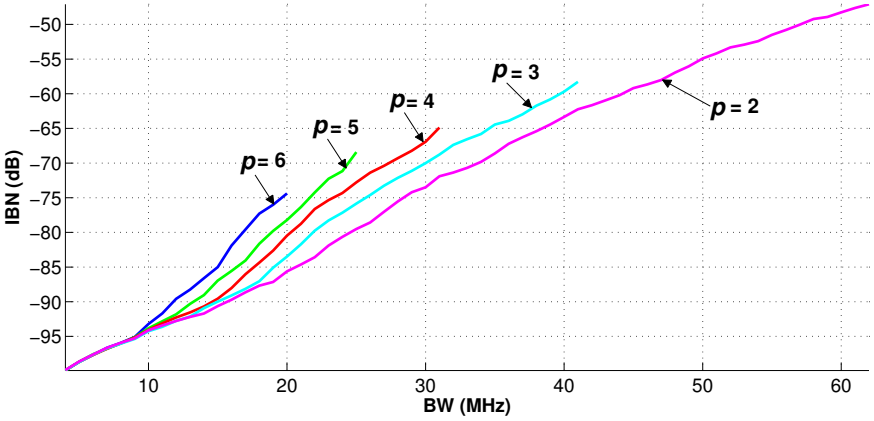


(b)

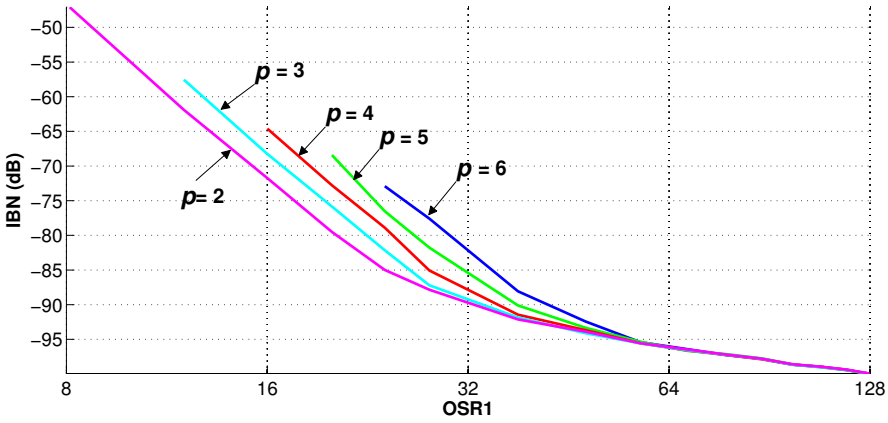


(c)

Figure 12: Output spectra for: (a) $p = 3$, (b) $p = 4$, (c) $p = 5$.



(a)



(b)

Figure 13: IBN for different values of p: (a) IBN vs. B_w. (b) IBN vs. OSR_1.

Table 1: Loop filter coefficient implementation of Fig.11

Transconductances	
$g_{m1} = 4g_{mu}$, $g_{m2} = g_{mu}$, $g_{m3} = 10g_{mu}$, $g_{m4} = 4g_{mu}$, $g_{m5} = 16g_{mu}$	
Capacitances	
Gm-C Integ.	$C_1 = g_{m1}/f_{s1}$, $C_2 = g_{m4}/f_{s1}$
SC Integ.	$C_{s1} = C_{s4} = 0.4$pF, $C_{s2} = C_{s3} = 0.1$pF, C_{s5} =0.2pF,$C_{i1} = C_{i2}$=0.4pF
Voltage-to-Current Converters and Feedback DACs	
$R = 1/g_{m1} = 3.3$kΩ, $I_{\mathrm{DAC1}} = 4g_{mu}V_{FS}$=300$\mu$A, $I_{\mathrm{DAC2}} = 2g_{mu}V_{FS}$=150$\mu$A	

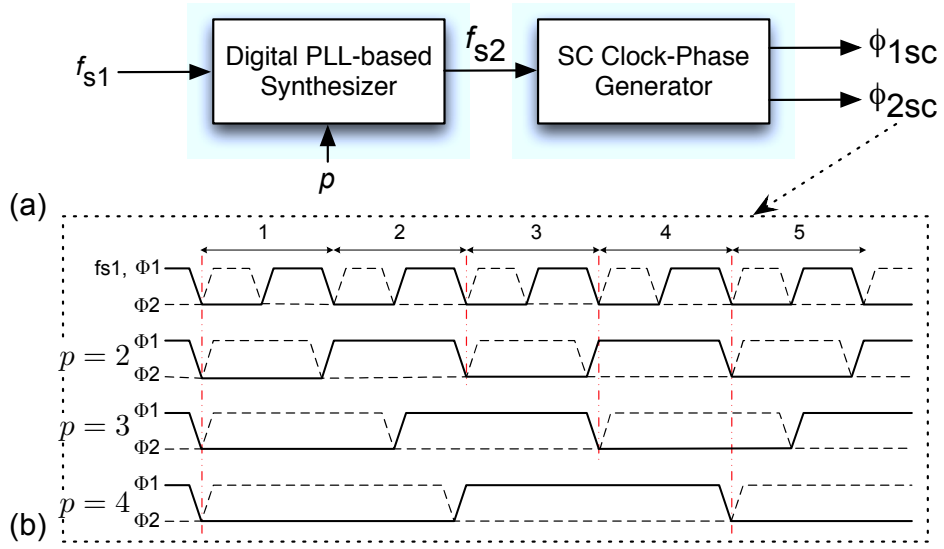
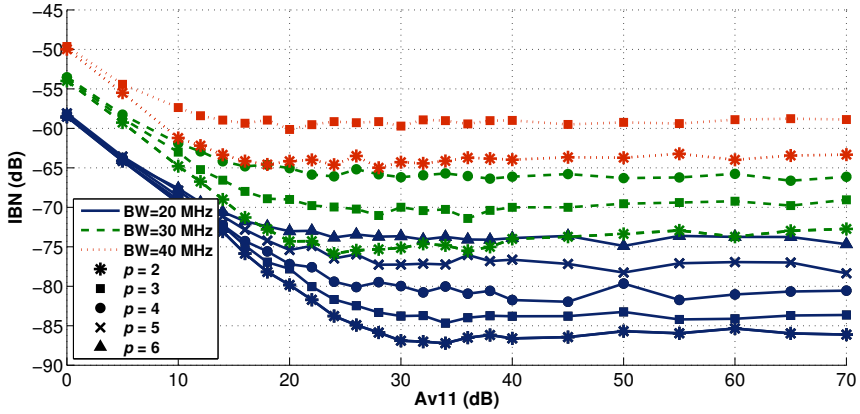
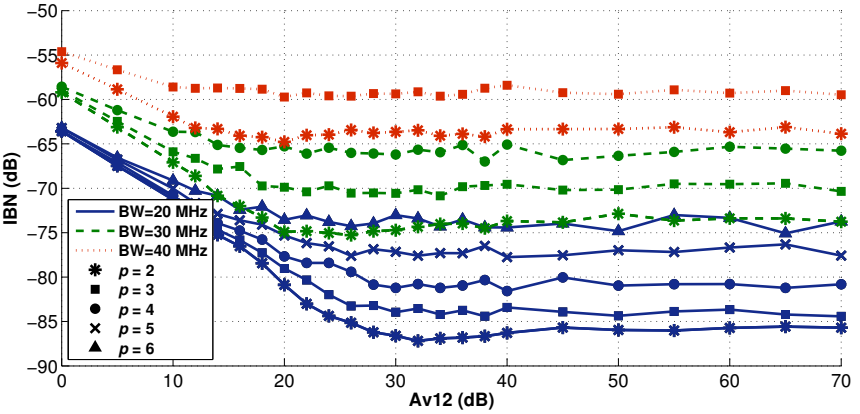


Figure 14: Clock phase generator. (a) Conceptual block diagram. (b) Clock phases for different values of the multi-rate ratio.



(a)



(b)

Figure 15: IBN degradation caused by finite OTA dc gain in (a) 1st and (b) 2nd Gm-C integrators.

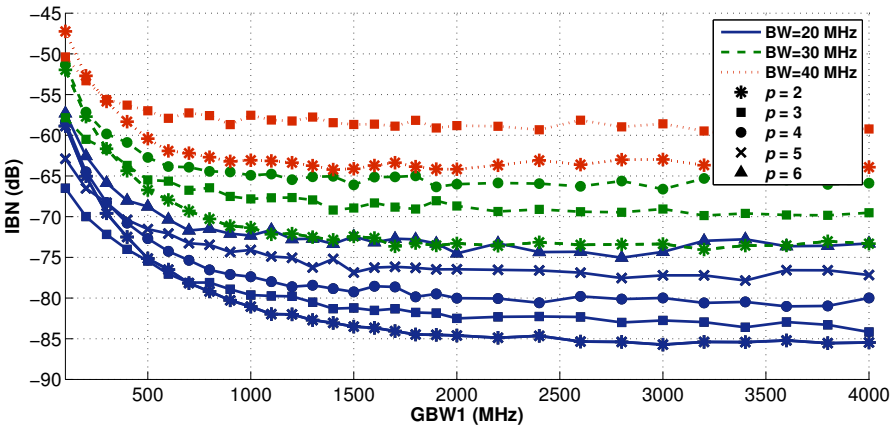


Figure 16: IBN degradation due to GBW of the front-end Gm-C integrator.

and capacitor mismatch in the DT part of the modulator, by showing an histogram of IBN for $B_w = 20$MHz and different values of p. In order to evaluate the impact of random circuit errors, a 250-sample Monte Carlo simulation was carried out, considering a standard deviation of 1% in the transconductances and 5% for the capacitors in the CT part of the circuit, while a 0.1% mismatch variation was considered for the SC stage. Note that the effective resolution degradation is similar to the one obtained in conventional cascade $\Sigma\Delta$Ms.

Table 2 sums up the modulator performance in terms of the maximum signal bandwidth, B_{wmax}, that can be handled for a given value of p, f_{s1} and the Signal-to-(Noise+Distortion) Ratio (SNDR). The table includes also the circuit-level performance metrics required to achieve this modulator performance, including both nonideal and nonlinear effects, such as the input-referred third-order intercept point (IIP3). In the case of SC integrators, folded cascode operational amplifiers were considered and their electrical per-

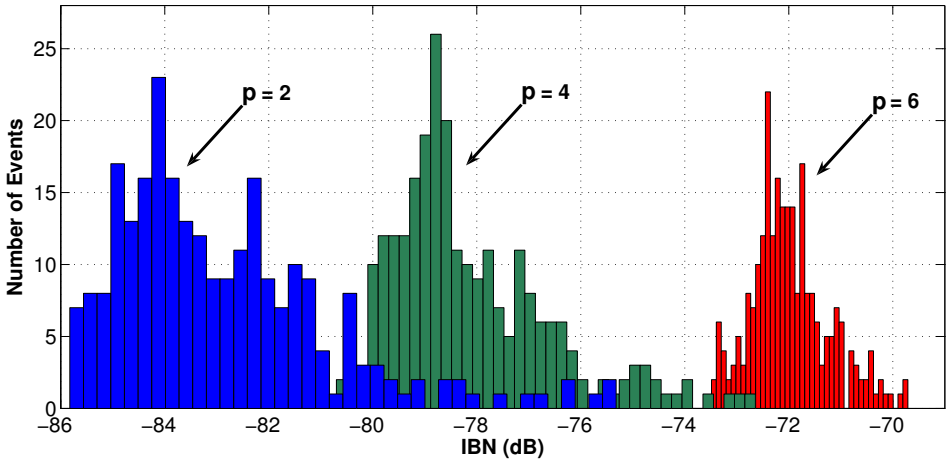


Figure 17: Monte Carlo simulation for $f_{s1} = 1$GHz and B_w =20MHz.

formance – extracted from transistor-level simulations carried out in Cadence Spectre – are also shown, considering a 1.2-V 90-nm CMOS technology.

The diverse range of specifications covered by the proposed modulator is illustrated in Fig. 18, that represents SNDR vs. input amplitude for f_{s1} =1GHz and considering different values of B_w and p, taking into account all circuit nonideal and nonlinear effects listed in Table 2. It can be noted that the modulator is able to cover a wide region in the resolution-vs-bandwidth plane.

Conclusions

The comparative study presented in this work has demonstrated that reducing the clock rate in the back-end stages of multi-rate cascade hybrid continuous-time/discrete-time $\Sigma\Delta$ modulators results in more efficient and robust data-converter architectures, compared to those based on conventional

Table 2: Modulator Performance Summary

Modulator									
p	2		3	4	5	6	(2,6)	2	
f_{s1}	1GHz						500MHz	333MHz	
B_{wmax} (MHz)	60	50	40	30	25	20	5	10	5
$SNDR$ (bits)	7	8.3	8.9	10	10.5	11.5	15	12.5	14.6
Clock Jitter (ps)	8.9	4	3	1.6	1.2	0.7	0.2	0.9	0.3
Front-End Gm-C Integrator									
DC Gain (dB)	20	20	20	25	25	30	40	35	40
GBW (GHz)	0.7	0.8	0.8	1	1.2	1.5	1.5	1.5	1.5
IIP3 (dBV)	10	13	15	18	20	25	35	30	35
Input Swing	500mV								
Output Swing	500mV								
Second Gm-C Integrator and Loop-filter Transconductances									
DC Gain (dB)	20	20	20	25	25	30	40	35	40
GBW (MHz)	200	250	250	300	350	400	500	450	500
IIP3 (dBV)	5	7	7	10	12	15	15	15	15
Input Swing	500mV								
Output Swing	500mV								
SC Integrators (Transistor-Level Performance)									
DC Gain (dB)	47								
g_m (mA/V)	4.4								
Phase Margin	73.4°								
Output Current (μA)	404								
Input Parasitic Cap. (pF)	0.2								
Out. Parasitic Cap. (pF)	0.1								
Output Swing (mV)	700								

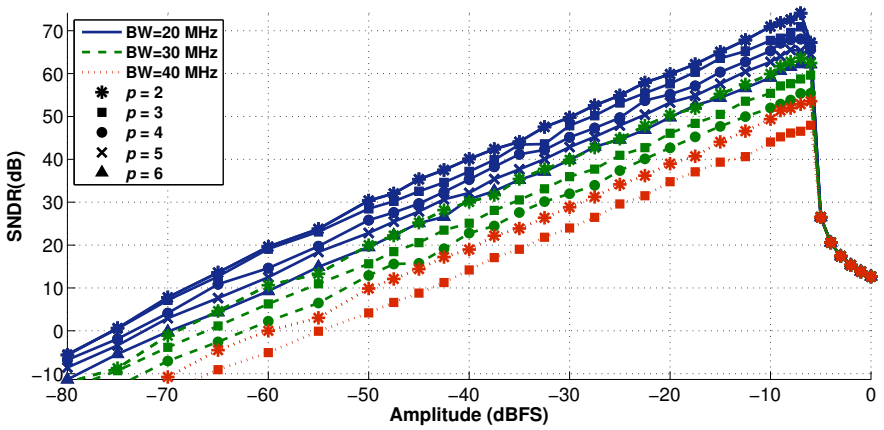


Figure 18: SNDR vs. amplitude for different values of B_w and p.

multi-rate (*upsampling*) topologies. The proposed *downsampling* multi-rate architectures are indeed less sensitive to the effect of the most critical error mechanisms that affect the performance of hybrid cascade $\Sigma\Delta$ modulators. The presented systematic methodology have resulted in the derivation of closed-form expressions that relate the main performance metrics of the modulators under study with their main circuit-error model parameters. The resulted expressions can be used for the design of either single-rate or multi-rate cascade hybrid $\Sigma\Delta$ modulators. This has been illustrated trough the high-level design of a multi-rate hybrid Gm-C/SC fourth-order cascade 2-2 $\Sigma\Delta$ modulator, intended to digitise signals with a 5-to-60MHz reconfigurable bandwidth, 7-to-15 bit scalable resolution and adaptive power consumption. The analytical procedures, as well as the architectural and circuital techniques presented in this work are being applied to the design of reconfigurable low-pass/band-pass $\Sigma\Delta$ RF-to-digital converters in software-defined-radio receivers integrated in nanometer CMOS technologies.

References

[1] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations.* Springer, 2006.

[2] P. Morrow *et al.*, "A 0.18μm 102dB-SNR Mixed CT SC Audio-band $\Delta\Sigma$ ADC," *IEEE ISSCC Digest of Technical Papers*, pp. 177–178, February 2005.

[3] K. Nguyen *et al.*, "A 106dB SNR Hybrid Oversampling ADC for Digital Audio," *IEEE ISSCC Digest of Technical Papers*, pp. 176–177, February 2005.

[4] B. Putter, "A 5th-Order CT/DT Multi-Mode $\Sigma\Delta$ Modulator," *IEEE ISSCC Digest of Technical Papers*, pp. 244–245, February 2007.

[5] S. Kulchycki *et al.*, "A 77-dB Dynamic Range, 7.5-MHz Hybrid Continuous-Time/Discrete-Time Cascade $\Sigma\Delta$ Modulator," *IEEE J. of Solid-State Circuits*, vol. 43, pp. 796–804, April 2008.

[6] M. Choi *et al.*, "A 101-dB SNR Hybrid Delta-Sigma Audio ADC Using Post Integration Time Control," *Proc. of the 2008 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 89–92, 2008.

[7] F. Colodro and A. Torralba., "Multirate $\Sigma\Delta$ Modulators ," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, pp. 170–176, March 2002.

[8] L. Bos *et al.*, "Multirate Cascaded Discrete-Time Low-Pass $\Delta\Sigma$ Modulator for GSM/Bluetooth/UMTS," *IEEE J. of Solid-State Circuits*, vol. 45, pp. 1198–1208, June 2010.

[9] M. Ortmanns *et al.*, "Multirate Cascaded Continuous-Time $\Sigma\Delta$ Modulators," *Proc. of the 2002 IEEE Int. Symp. on Circuits and Systems (ISCAS'02)*, pp. 4225–4228, May 2002.

[10] J. G. García-Sánchez and J. M. de la Rosa, "Multirate Downsampling Hybrid CT/DT Cascade Sigma-Delta Modulators," *IEEE Trans. on Circuits and Systems–I: Regular Papers*, vol. 59, pp. 285–294, 2 2012.

[11] R. del Río *et al.*, *CMOS Cascade $\Sigma\Delta$ Modulators for Sensors and Telecom: Error Analysis and Practical Design.* Springer, 2006.

[12] P. Benabes, "Accurate Time-Domain Simulation of Continuous-Time Sigma-Delta Modulators.," *IEEE Trans. on Circuits and Systems – I: Regular Papers*, vol. 56, pp. 2248–2258, October 2009.

[13] S. Pavan, "Systematic Design Centering of Continuous Time Oversampling Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, pp. 158–162, March 2010.

[14] H. Kwan *et al.*, "Design of Hybrid Continuous-Time Discrete-Time Delta-Sigma Modulators," *Proc. of the 2008 IEEE Int. Symp. on Circuits and Systems (ISCAS'08)*, pp. 1224–1227, May 2008.

[15] J. Ruiz-Amaya *et al.*, "High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time $\Sigma\Delta$ Modulators Using

SIMULINK-based Time-Domain Behavioral Models," *IEEE Trans. on Circuits and Systems – I: Regular Papers*, vol. 51, pp. 1795–1810, September 2005.